Winbond Electronics Corp.

STEPLESS CLOCK FOR VIA P4 CHIPSET

W83194BR-P4X

Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for .
2	n.a.	02/July	1.0	n.a	Change version and version on web site to 1.0
3	4,10	07/Aug	1.1	1.1	FS1 internal 120K pull up change to pull down. Register 3: bit 0,1 PCISTOPB read back & CPUSTOPB read back exchange. Change version and version on web site to 1.1
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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STEPLESS CLOCK FOR VIA P4 CHIPSET

1. GENERAL DESCRIPTION

The W83194BR-P4X is a Clock Synthesizer for VIA P4 chipset. W83194BR-P4X provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, AGP clocks setting. All clocks are externally selectable with smooth transitions.

The W83194BR-P4X provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% and +/-0.25% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

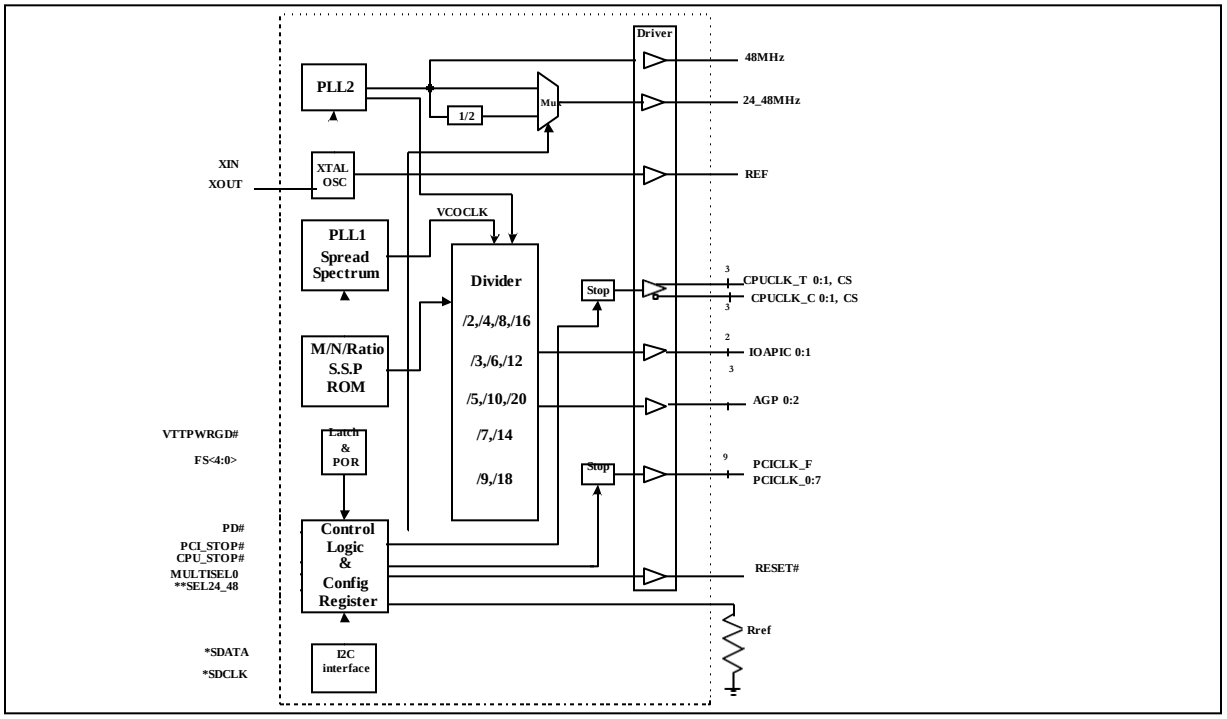
The W83194BR-P4X also has watch dog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-P4X accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. The fixed frequency outputs as REF and 48 MHz provide better than 0.5V /ns slew rate.

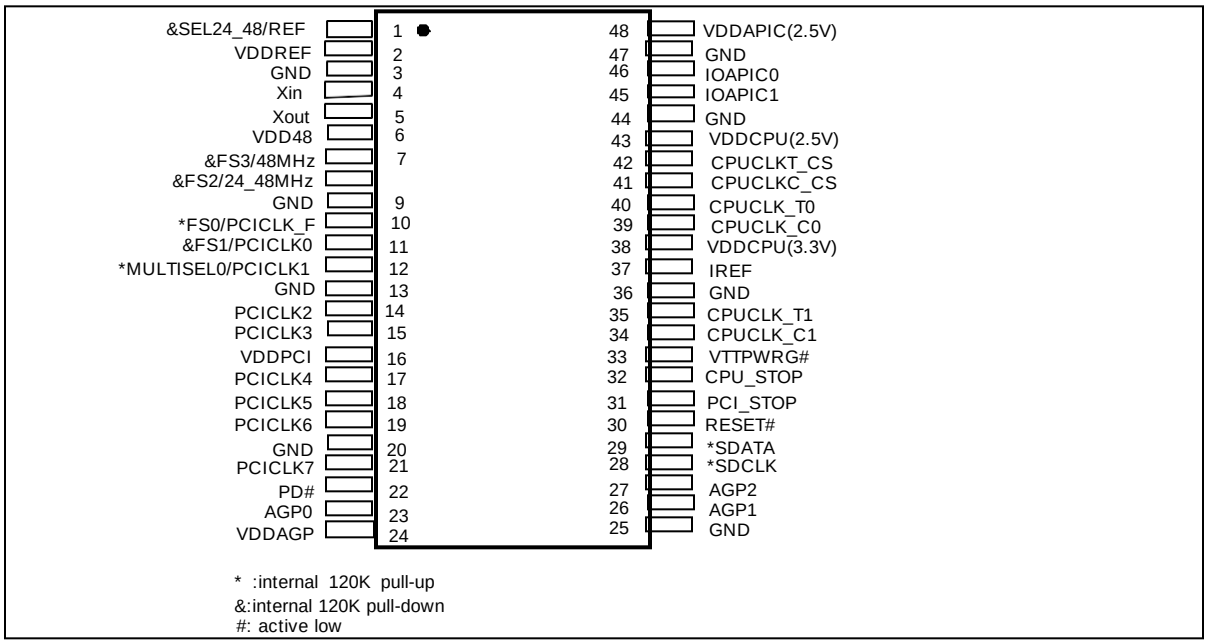
2. PRODUCT FEATURES

- 2 Differential pairs of CPU clock outputs
- 1 Differential pairs push pull of CPU_CS clock outputs
- 3 AGP clock outputs
- 9 PCI synchronous clocks
- 24_48Mhz clock output for super I/O.
- 48 MHz clock output for USB.
- 2 IOAPIC clock outputs.
- 1 REF clock output.
- Skew form CPU to PCI clock 1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200MHz
- Step-less frequency programming
- I^2C 2-Wire serial interface and support byte read/write and block read/write.
- -0.5% and +/- 0.25% center type spread spectrum
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PIN DESCRIPTION

IN – Input

IN_{tp120k} – Latched input at power up, internal 120kO pull up.

IN_{td120k} – Latched input at power up, internal 120kO pull down.

OUT – Output

OD – Open Drain

I/O - Bi-directional Pin

I/OD – Bi-directional Pin, Open Drain.

 # - Active Low

*** - Internal 120kΩ pull-up**

&- Internal 120 kΩ pull-down

5.1. Crystal I/O

PIN	SYMBOL	I/O	FUNCTION
4	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
5	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2. CPU, AGP, and PCI, IOAPIC Clock Outputs

PIN	SYMBOL	I/O	FUNCTION
34,35,39,40	CPUCLK_T [0:1] CPUCLK_C [0:1]	OUT	Low skew (< 250ps) differential clock outputs for host frequencies of CPU
41,42	CPUCLKT_CS CPUCLKC_CS	OUT	Low skew (< 250ps) differential push pull clock outputs for host frequencies of CHIPSET
23,26,27	AGP0: 2	OUT	3.3V AGP clock outputs.
10	PCICLK_F	OUT	3.3V free running PCI clock output.
	*FS0	IN_{tp120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency. This is internal 120K pull up.
11	PCICLK0	OUT	3.3V PCI clock output.
	*FS1	IN_{tp120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency, This is internal 120K pull down.
12	PCICLK1	OUT	3.3V PCI clock output.
	*MULTI_SEL0	IN_{tp120k}	Latched input for MULTSEL0 at initial power up, internal 120K pull up
14,15,17,18, 19,21	PCICLK [2:7]	OUT	Low skew (< 250ps) PCI clock outputs.
45,46	IOAPIC0: 1	OUT	2.5V PCI/2 clock outputs.