Description

The SPCA751A is a single chip signal processor optimized for MPEG audio decoding and voice recording. It is developed to achieve a better performance/cost ratio for MPEG audio players.

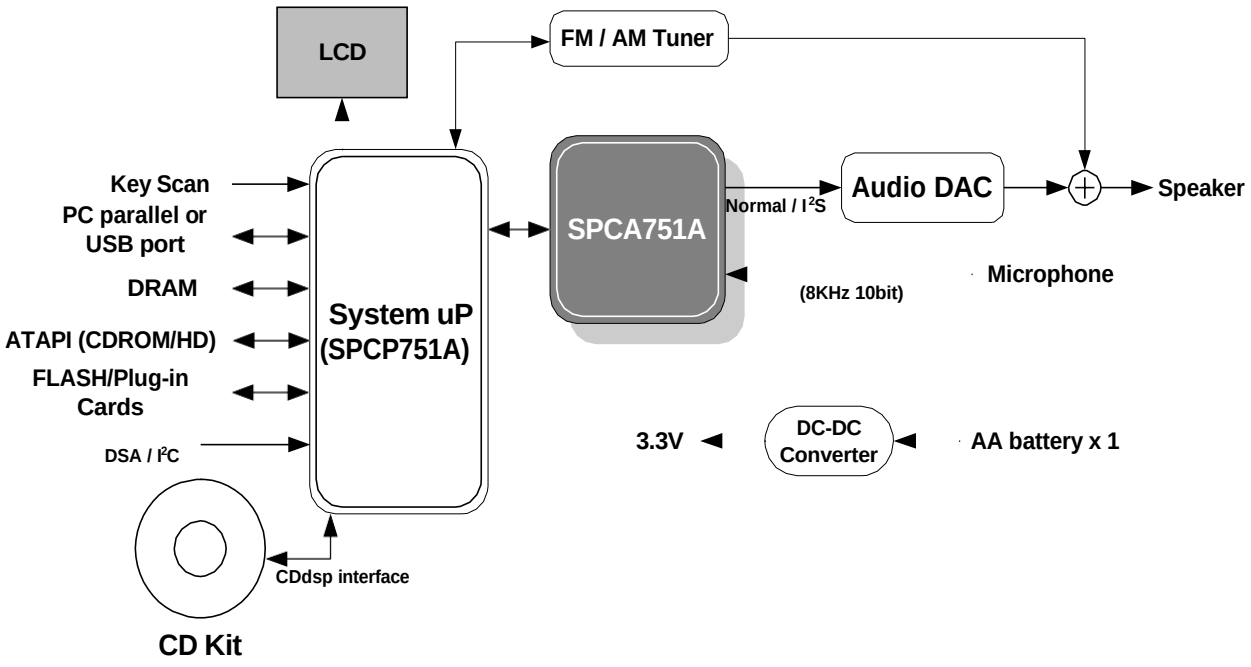
The SPCA751A is especially designed for standalone audio players, the system controller can easily carry out the MPEG audio decoding process by the use of a general serial IO/control interface for MPEG bit stream in/out and playback control.

Decoded audio PCM data are output to external DAC through a programmable normal/I^{2}S DAC interface, such that most of common audio DACs can be cooperated with SPCA751A to meet different customers' requirements.

A high quality 10-bit 8KHz sampling rate ADC is embedded for voice recording. Based on the algorithm of SACM_S480 or SACM_S3200, voice is compressed to a low data rates of 4.8Kbps and 32Kbps respectively, while retaining a good resolution of the original speech/audio.

The SPCA751A is designed for 3.3V applications, A built in PLL is able to synthesize the system clock from a 16.934MHz crystal oscillator source. The high performance SPCA751A signal processor can operate at 34MHz and dissipate low power, which makes the SPCA751A extremely suitable for portable systems.

A common implementation utilizing the SPCA751A is presented below:

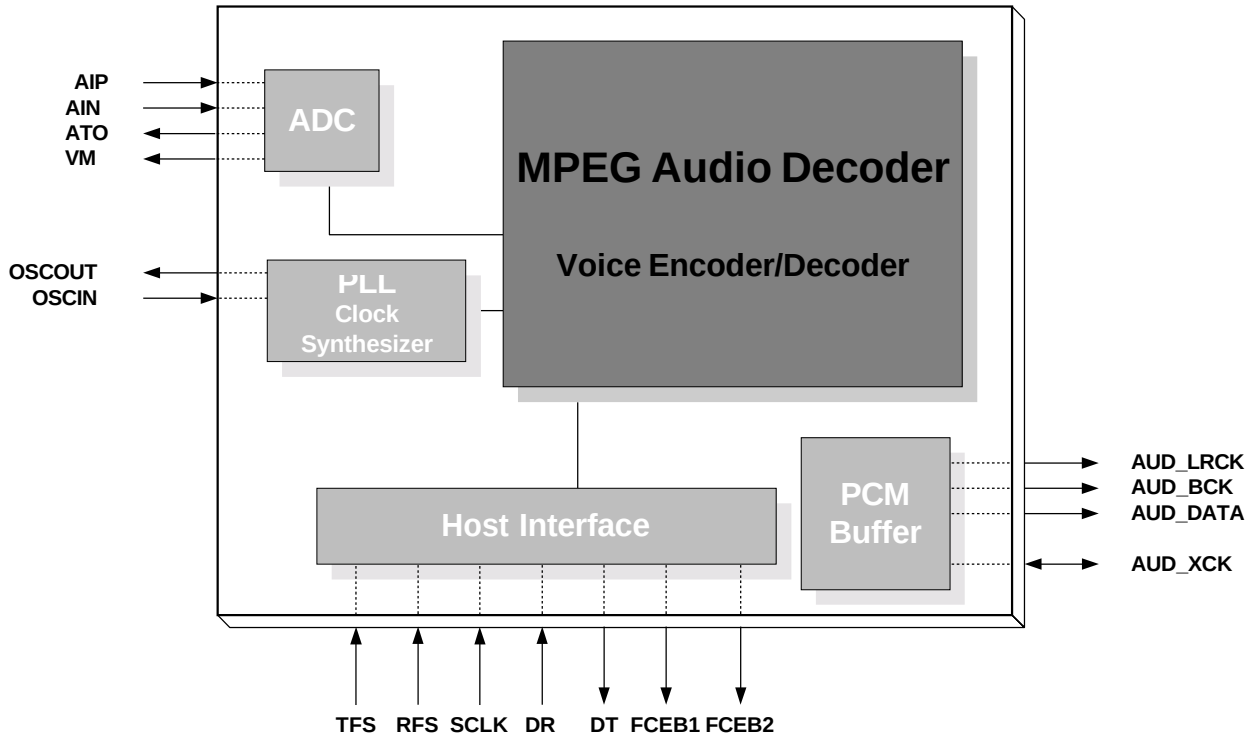


MPEG Audio Player System Block Diagram

Features

- Single chip MPEG audio decoder
  - Conforming to MPEG1/MPEG2 audio layer 2/3
  - Extension to MPEG lower sampling rates
- Digital sound control
  - Digital volume control
  - Stereo/Mono channel select
  - Digital sound equalizer
- Internal auto-generate audio clock
  - Sampling frequency from 8 kHz up to 48 kHz
- Programmable audio DAC interface
  - Support both normal and I^2S audio DAC formats
  - Audio clock polarity programmable
  - Internal auto-generated oversampling clock for DAC
  - Accept external audio clock for sampling rate control
- Serial data IO and control interface
  - Easy for the host processor to command
- Low power dissipation
- PLL embedded
  - Require only 16.934MHz crystal, resistors, and capacitors to supply the system clock
- Built-in Digital Recording option
  - Embedded 10-bit 8 kHz audio ADC
  - SACM_S480 recording with 4.8 kbit/sec
  - SACM_S3200 recording with 32 kbit/sec
- Device Parameter
  - Supply voltage : 3.0 ~ 3.6 volts
  - IO interface : 5 volts tolerance, TTL compatible
  - Package : 44-pin LQFP
  - Power consumption: less than 150 mW @ 3.6 volts

SPCA751A BLOCK DIAGRAM



Function Description

The SPCA751A is a single-chip CMOS microprocessor optimized for real-time MPEG audio decoding and speech/audio recording.

SPCA751A decodes the encoded MPEG audio data according to the commands passed through the ***Serial Control/Data I/O Interface*** by the host processor, the host processor can also check the status of decoding process by the use of this interface. Refer to *Programming Guide* for command definitions

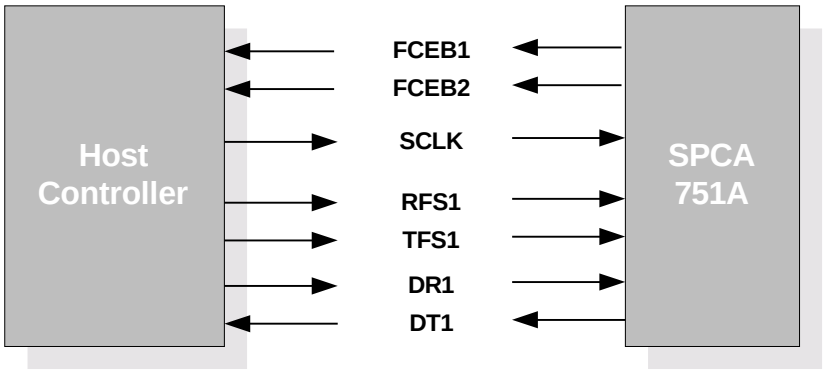
In the digital recorder mode, speech/Audio is sampled at 8Khz by the on-chip ***ADC*** into 10-bit digital words, after encoding, the datum is compressed into a data rate of 4.8Kbps or 32Kbps.

Decoded audio PCM data are output to external DAC through a programmable normal/I^2S ***PCM interface***, this interface is compliant to most of the common audio DACs.

The embedded ***PLL*** is capable of providing the 27 MHz system clock derived from a 16.934MHz clock source

■ *Serial Control/Data I/O Interface*

The host controller uses this interface to transfer MPEG bit-stream with the SPCA751A and to command the SPCA751A during the recording/decoding process. This interface consists of seven pins:



Pin	# 12	*FCEB2*	Frame Decoded Indicator generated by the SPCA751A
Pin	# 13	*FCEB1*	Data Request Flag generated by the SPCA751A
Pin	# 44	*SCLK1*	Bit Clock controlled by the host processor
Pin	# 1	*DT1*	Data from the SPCA751A to the host processor
Pin	# 2	*TFS1*	Transmit Frame Synchronization controlled by the host processor
Pin	# 3	*DR1*	Data from the host processor to the SPCA751A
Pin	# 4	*RFS1*	Receive Frame Synchronization controlled by the host processor

- ***FCEB1* - Data Request Flag**

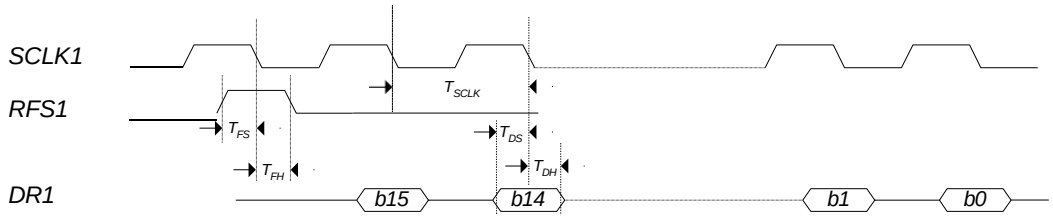
The *FCEB1* flag generated by the SPCA751A informs the status of the decoding/encoding process. When *FCEB1* is high, it indicates that the SPCA751A is ready to receive data/command or to transfer data, the host processor is allowed to start the communication; When *FCEB1* is low, the SPCA751A is busy processing internally and no I/O tasks could be taken, the commands sent by the host processor during low *FCEB1* are not accepted by the SPCA751A and may cause the SPCA751A run into an unknown state.

✂ *FCEB2* - Frame Decoded Indicator

Each time the SPCA751A has decoded one frame (512 bytes) of data, it changes the state of *FCEB2* (either high to low or low to high) and progresses to the next frame. By counting the number of state-changes, the host processor is able to know the time elapsed in decoding.

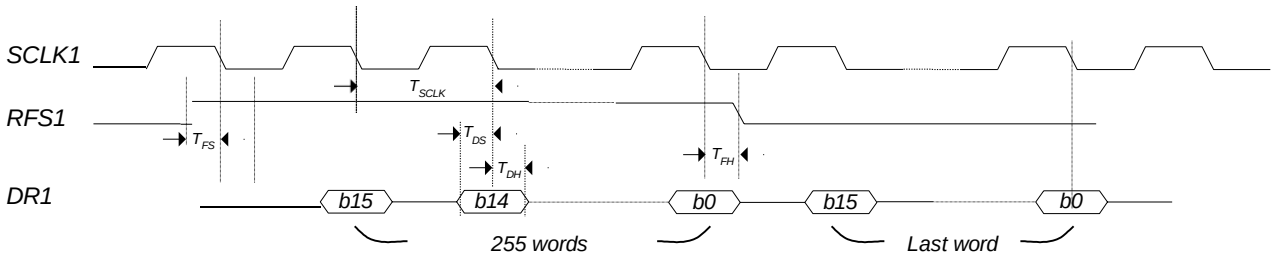
✂ Host Command

The host commands consist of 8-bit command and 8-bit ID, totally 16-bit long. (Refer to the SPCA751A Programming Guide for command definitions) At the falling edges of *SCLK1*, the SPCA751A checks whether the *RFS1* is high. Once it is high, the 16-bit long command is sampled at the following 16 consecutive falling edges of *SCLK1* with MSB first. After the LSB is sent, the host processor should send at least one more cycle of *SCLK*1 to the SPCA751A.



✂ Host processor writes 512 bytes to the SPCA751A

At the falling edges of *SCLK1*, the SPCA751A checks whether the *RFS1* is high. Once it is high, the 512-byte long data is sampled at the following 512x8 consecutive falling edges of *SCLK1*. *RFS1* should remain high before the MSB of the last word. After the LSB of the last word is sent, the host processor should send at least three more cycles of *SCLK*1 to the SPCA751A.



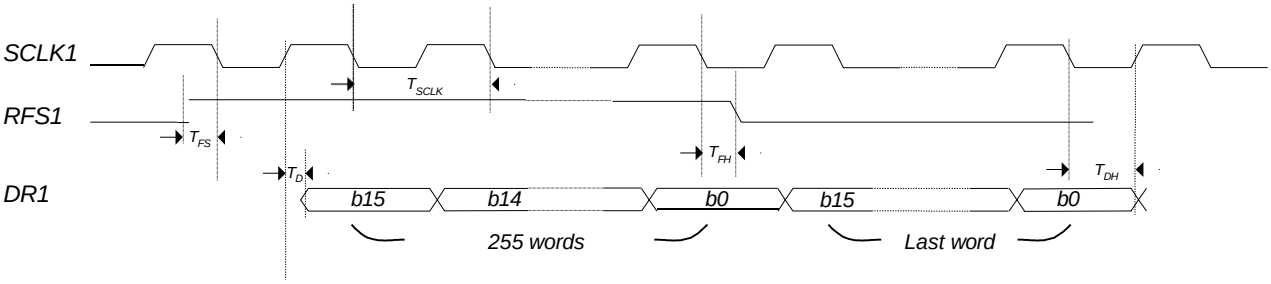
Timing Requirements

PARAMETER		*MIN.*	*MAX.*	*UNIT*
TFS	*RFS1* setup before *SCLK1* falls low	2		ns
TFH	*RFS1* hold after *SCLK1* falls low	2		ns
TDS	*DR1* setup before *SCLK1* falls low	3		ns
TDH	*DR1* hold after *SCLK1* falls low	3		ns
TSCLK	*SCLK1* period	16	*	ns

* The maximum period of *SCLK1* depends on the sampling rate of the decoded data, too long a *SCLK1* period makes the real-time decoding impossible.

✂ **Host processor reads 512 bytes from the SPCA751A**

To read data from the SPCA751A, the host processor first asserts the *TFS1* at the falling edges of *SCLK1*, then the 512-byte long data is sampled out from the SPCA751A at the following 512x8 consecutive rising edges of *SCLK1*. The host processor is supposed to latch-in the data at the falling edges of *SCLK1. TFS1* should remain high before the MSB of the last word. After the LSB of the last word is received, the host processor should send at least three more cycles of *SCLK*1 to the SPCA751A.



Timing Requirements

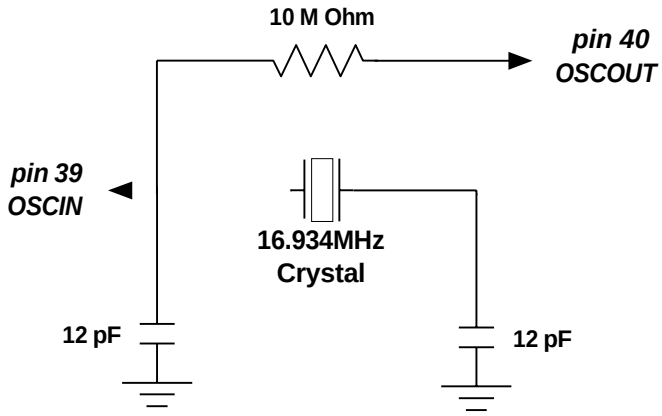
PARAMETER		*MIN.*	*MAX.*	*UNIT*
TFS	*TFS1* setup before *SCLK1* falls low	2		ns
TFH	*TFS1* hold after *SCLK1* falls low	2		ns
TSCLK	*SCLK1* period	16		ns

Switching Characteristics

PARAMETER		*MIN.*	*MAX.*	*UNIT*
TD	*DT1* access		5	ns
TDH	*DT1* hold after *SCLK1* falls low	TSCLK / 2		ns

✎ ***PLL***

An independent analog power is applied through *pin 41 VSSP* and *pin 42 VDDP* to supply the power for the internal *PLL*. An oscillation circuit is built externally on *pin 39 OSCIN* and *pin 40 OSCOUT*.



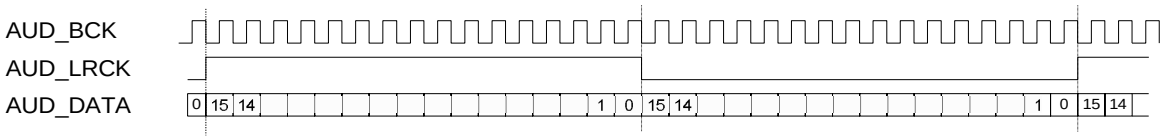
Oscillation Circuit

PCM Interface

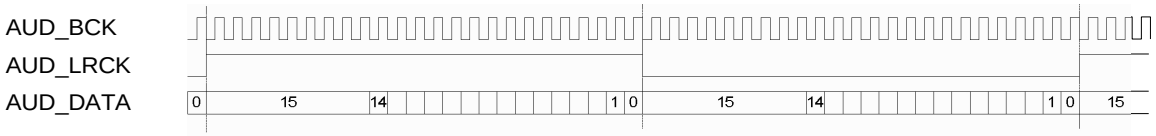
The PCM Interface is used to output decoded audio data to external audio DAC. There are 4 signals, AUD_XCK, AUD_LRCK, AUD_BCK and AUD_DATA. The signal format of PCM Interface is programmable with register 0x3fDE.

Register Name	Register #	Bits	Description	(Value set at initialization) (0x2103)
AUD_CONFIG	0x3FDE	14	Audio out configuration (RW) bit 0 = I²S control bit 1 = AUD_XCK select bit 2 = AUD_DATA LSB / MSB sent first bit 3 = AUD_BCK active edge bit 4 = AUD_XCK IO select bit 5 = LRCK polarity bit 12 = CD-DA pass through mode	 (0 = I²S, 1 = normal) (0 = 256×Fs, 1 = 384×FS) (0 = MSB first, 1 = LSB first) (0 = falling, 1 = rising) (0 = output, 1 = input) (0 = LRCK low is right, 1 = LRCK low is left) (0 = disable, 1 = enable)

Normal Mode:

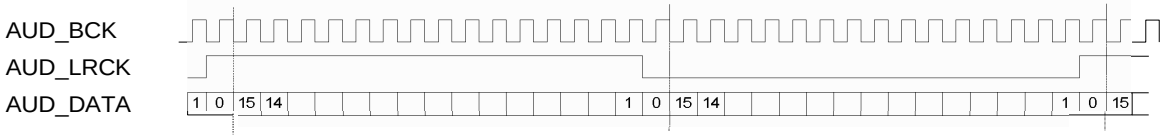


BCK = 32 x Fs

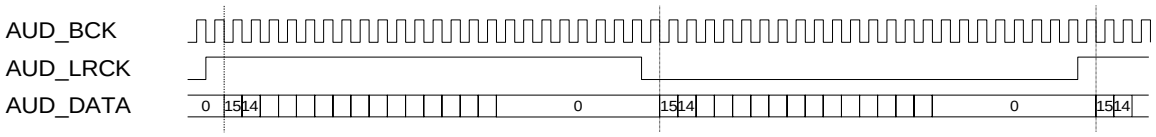


BCK = 48 x Fs

I²S Mode:



BCK = 32 x Fs



BCK = 48 x Fs

PCM Interface waveform

ADC

The SPCA751A has an audio-band sigma-delta analog-to-digital converter so as to meet the requirement of the digital recorder application. The circuit of converter consists of two main blocks: the analog- to-digital converter (ADC) and internal reference and bias voltage. For the latter, it is 15-bit format with 10-bit resolution.

The analog-to-digital conversion chain consists of a microphone amplifier (M.A.), a programmable gain amplifier (PGA), an analog oversampled modulator, and the decimation digital filter. The PGA has gain step from –12dB to 12dB (-12, -6, 0, 6, 12dB). The modulator is a sigma-delta feedback loop, which oversamples the signal at 1.024MHz and provides second-order noise shaping. It performs the conversion of the differential analog input signal to a pulse-density-modulated single-bit digital output. When a maximum positive differential input voltage is applied at the input of modulator, the resulting code at the output of the modulator is all ones. The decimation digital filter consists of a comb filter and a half-band filter. The comb filter is a third-order comb filter. Finally the encoder implements the half-band filter and data compression by software.

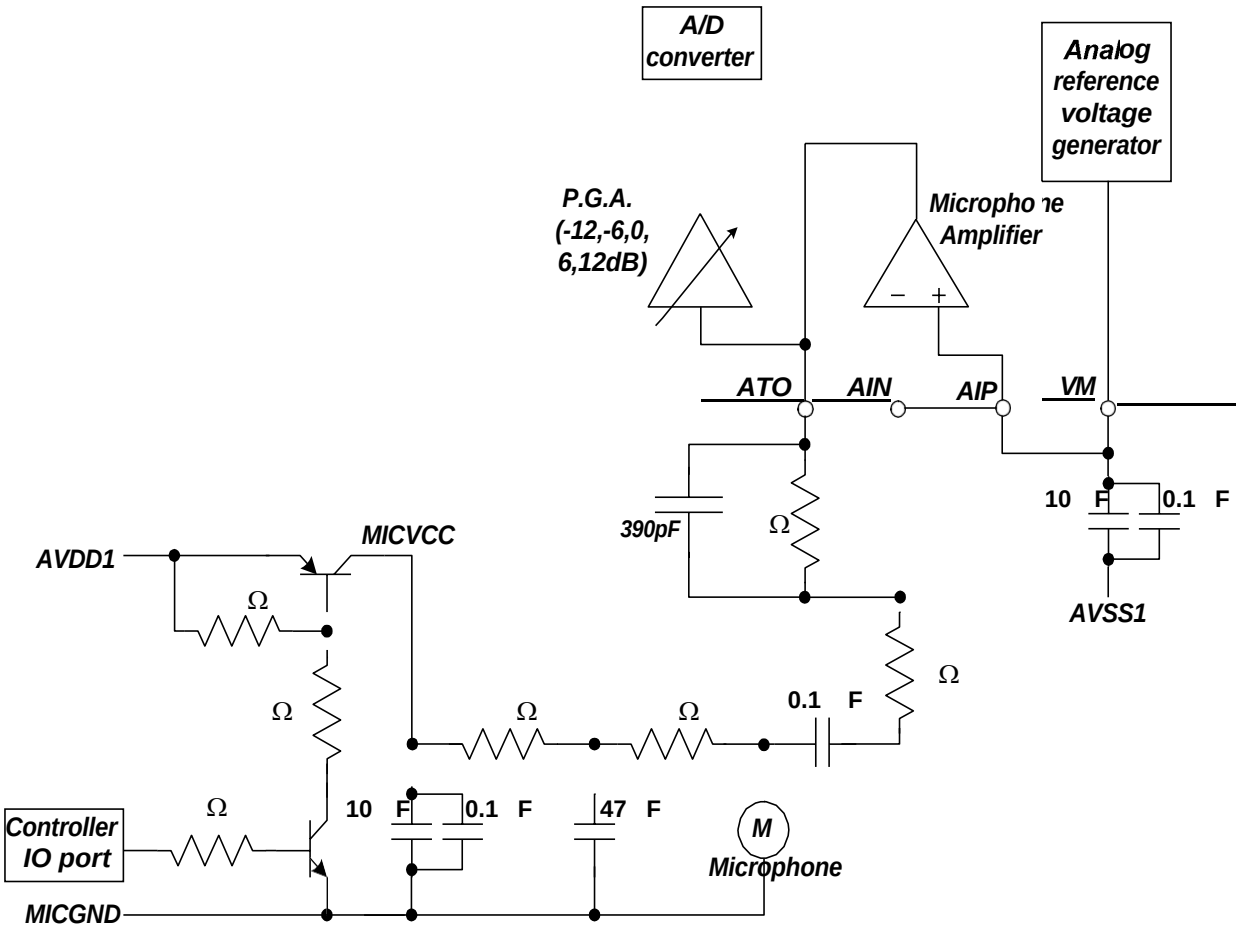
ADC & DAC ELECTRICAL CHARACTERISTICS (T_A = 25°C, VDD = 3.3 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
ATO:	MA gain = 0dB,				
Input Voltage	PGA gain = 6dB			0.25*VDD	Vpp
PGA:	Default: 6dB				
Gain Range		-12		12	dB
Step Size			6		dB
Step Variation			0.5		dB
Voltage Reference:					
Output Voltage		0.45VDD	0.5VDD	0.55VDD	Vpp

ADC PATH CHARACTERISTICS

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
ADC:	F_{IN} = 1kHz,				
Signal to noise ratio	PGA gain = 12dB		60		dB
	ATO is full swing				
	Without data compression				

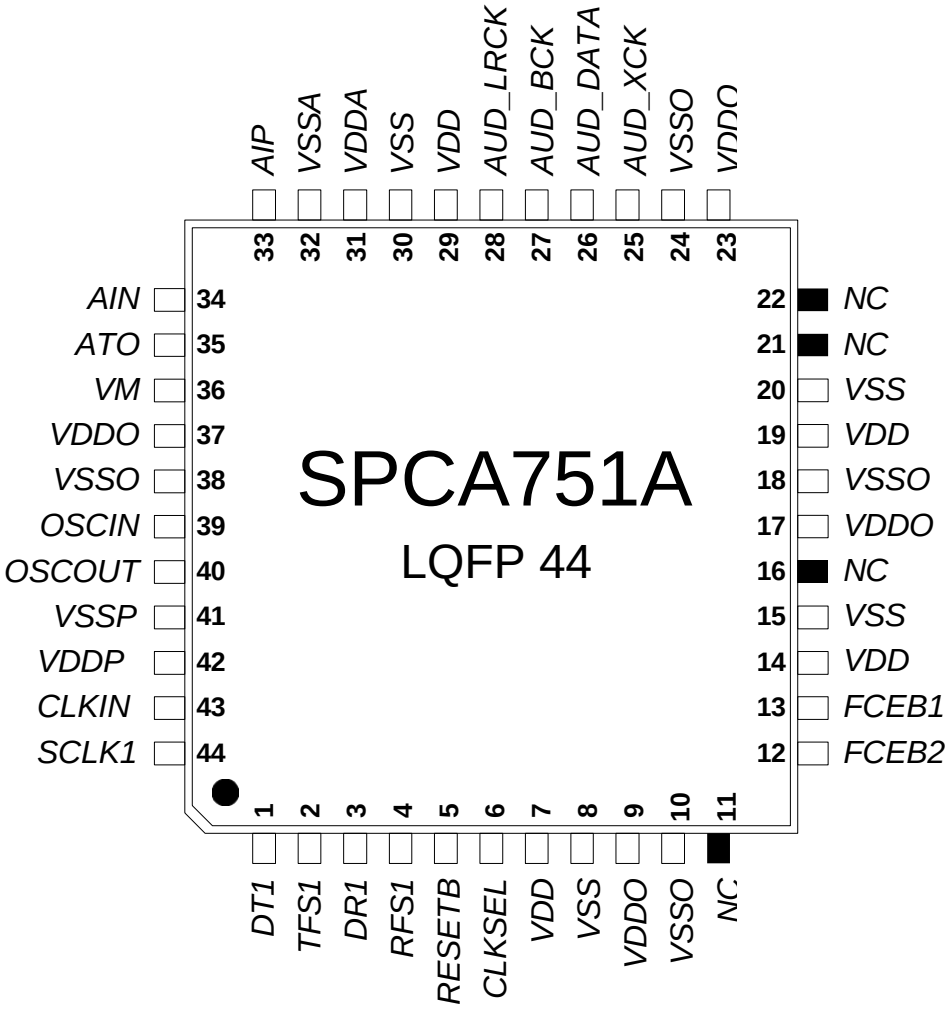
DIGITAL RECODER APPLICATION CIRCUIT



Pin Description

PIN No.	Mnemonic	Type	Description
1	DT1	O	Transmit Data of Serial Port
2	TFS1	I/O	Transmit Frame Synchronization of Serial Port
3	DR1	I	Receive Data of Serial Port
4	RFS1	I/O	Receive Frame Synchronization of Serial Port
5	$\overline{\text{RESET}}$	I	System Reset (Active Low)
6	$\overline{\text{CLKSEL}}$	I	System Clock Select (0: Internal PLL 1:External Oscillator)
7	VDD	I	Digital Power
8	VSS	I	Digital Ground
9	VDDO	I	Digital Power
10	VSSO	I	Digital Ground
11	N.C.		No Connection
12	FCEB2	O	Frame Decoded Indicator
13	FCEB1	O	Data Request Flag
14	VDD	I	Digital Power
15	VSS	I	Digital Ground
16	N.C.		No Connection
17	VDDO	I	Digital Power
18	VSSO	I	Digital Ground
19	VDD	I	Digital Power
20	VSS	I	Digital Ground
21	N.C.		No Connection
22	N.C.		No Connection
23	VDDO	I	Digital Power
24	VSSO	I	Digital Ground
25	AUD_XCK	I/O	Oversampling Clock to external Audio DAC / from external source
26	AUD_DATA	O	Serial Data Output to Stereo Audio DAC
27	AUD_BCK	O	Bit Clock Output to Stereo Audio DAC
28	AUD_LRCK	O	Sample Rate Clock Output to Stereo Audio DAC
29	VDD	I	Digital Power
30	VSS	I	Digital Ground
31	VDDA	I	Analog Power for Audio ADC
32	VSSA	I	Analog Ground for Audio ADC
33	AIP	I	Positive Input of the Audio ADC transmit input amplifier
34	AIN	I	Negative Input of the Audio ADC transmit input amplifier
35	ATO	O	Output of the Audio ADC transmit input amplifier
36	VM	O	1/2 AVDD for the bias of the Audio ADC transmit input amplifier
37	VDDO	I	Digital Power
38	VSSO	I	Digital Ground
39	OSCIN	I	16.934MHz Oscillator Input
40	OSCOUT	O	16.934MHz Oscillator Output
41	VSSP	I	Analog Ground for PLL
42	VDDP	I	Analog Power for PLL
43	CLKIN	I	External System Clock (Connect to VSS if internal PLL is used (pin 82 CLKSEL == 0))
44	SCLK1	I/O	Bit Clock of Serial Port

PIN Map


SPCA751A
LQFP 44
1 DT1
2 TFS1
3 DR1
4 RFS1
5 RESETB
6 CLKSEL
7 VDD
8 VSS
9 VDDO
10 VSSO
11 NC
12 FCEB2
13 FCEB1
14 VDD
15 VSS
16 NC
17 VDDO
18 VSSO
19 VDD
20 VSS
21 NC
22 NC
23 VDDO
24 VSSO
25 AUD_XCK
26 AUD_DATA
27 AUD_BCK
28 AUD_LRCK
29 VDD
30 VSS
31 VDDA
32 VSSA
33 AIP
34 AIN
35 ATO
36 VM
37 VDDO
38 VSSO
39 OSCIN
40 OSCOUT
41 VSSP
42 VDDP
43 CLKIN
44 SCLK1