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Advanced PWM and Triple Linear Power Controller for Gateway Applications

The ISL6440A provides the power control and protection for four output voltages required by microprocessors used in high-performance, graphics-intensive gateway applications. The IC integrates a voltage-mode PWM controller and three linear controllers, as well as the monitoring and protection functions into a 28 lead SOIC package.

The synchronous rectified buck converter includes an Intel®-compatible, TTL five-input, digital-to-analog converter (DAC) that adjusts the core PWM output voltage from 1.3V_{DC} to 2.05V_{DC} in 0.05V steps and from 2.1V_{DC} to 3.5V_{DC} in 0.1V increments. The precision reference and voltage-mode control provide ±1% static regulation. A TTL-compatible signal applied to the SELECT pin dictates which method of control is used for the AGP bus power. A low state results in linear control of the AGP bus to 1.5V, while a high state transitions the output through a linearly controlled soft-start to 3.3V, followed by full enhancement of the external MOSFET to pass the input voltage. The other two linear regulators provide fixed output voltages of 1.5V GTL bus power and 1.8V power for the north/south bridge core and/or cache memory. These levels are user-adjustable by means of an external resistor divider and pulling the FIX pin low. All linear controllers can employ either N-Channel MOSFETs or bipolar NPNs for the pass transistor.

The ISL6440A monitors all the output voltages. A single power good signal is issued when the core is within ±10% of the DAC setting and all other outputs are above their under-voltage levels. Additional built-in overvoltage protection for the core output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM controller's overcurrent function monitors the output current by using the voltage drop across the upper MOSFET's $r_{DS(ON)}$.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ISL6440ACB	0 to 70	28 Ld SOIC	M28.3

Features

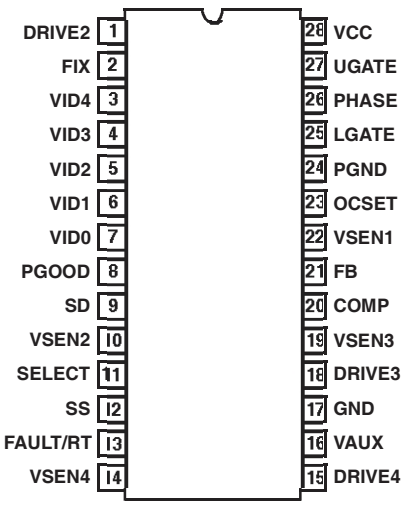
- Provides four regulated voltages
  - Microprocessor core, AGP bus, memory, and GTL bus power
- Drives N-Channel MOSFETs
- Linear regulator drives compatible with both MOSFET and bipolar series pass transistors
- Fixed or externally resistor-adjustable linear outputs
- Simple single-loop control design
  - Voltage-mode PWM control
- Fast PWM converter transient response
  - High-bandwidth error amplifier
  - Full 0–100% duty ratio
- Excellent output voltage regulation
  - Core PWM output: ±1% over temperature
  - Other outputs: ±3% over temperature
- TTL-compatible 5-bit DAC core output voltage selection
  - Shutdown feature removed when all inputs high
  - Wide range 1.3V_{DC} to 3.5V_{DC}
- Power-good output voltage monitor
- Overvoltage and overcurrent fault monitors
  - Switching regulator does not require extra current Sensing element, uses upper MOSFET's $r_{DS(ON)}$
- Small converter size
  - Constant frequency operation
  - 200kHz free-running oscillator; programmable from 50kHz to over 1MHz
  - Small external component count

Applications

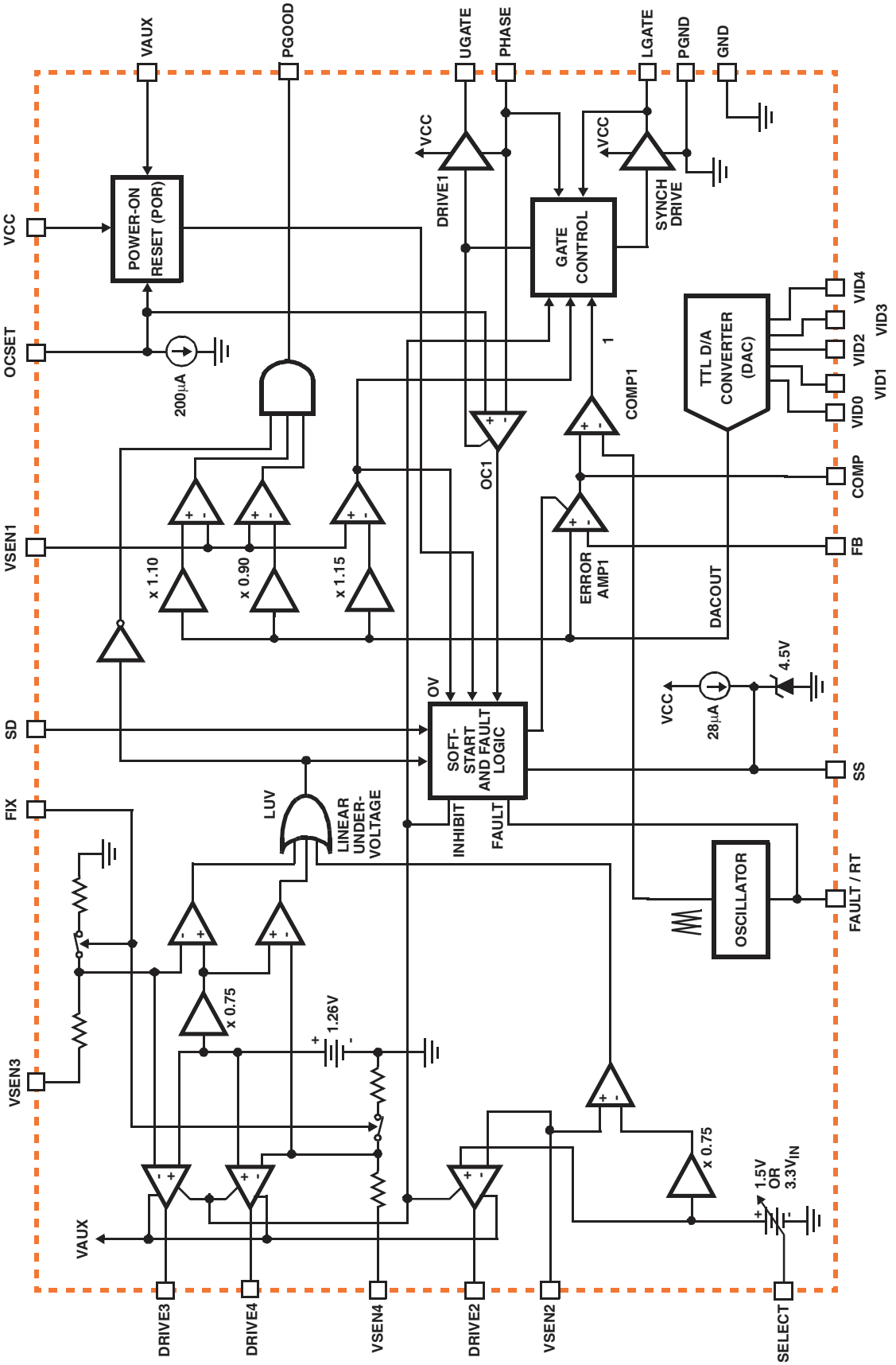
- Power regulation for gateway processors

Pinout

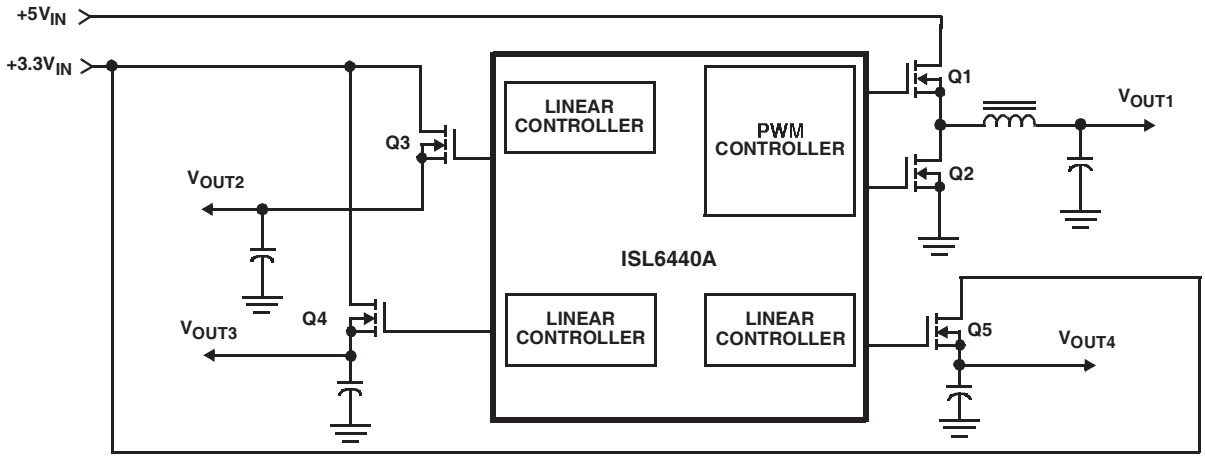
ISL6440A (SOIC)
TOP VIEW



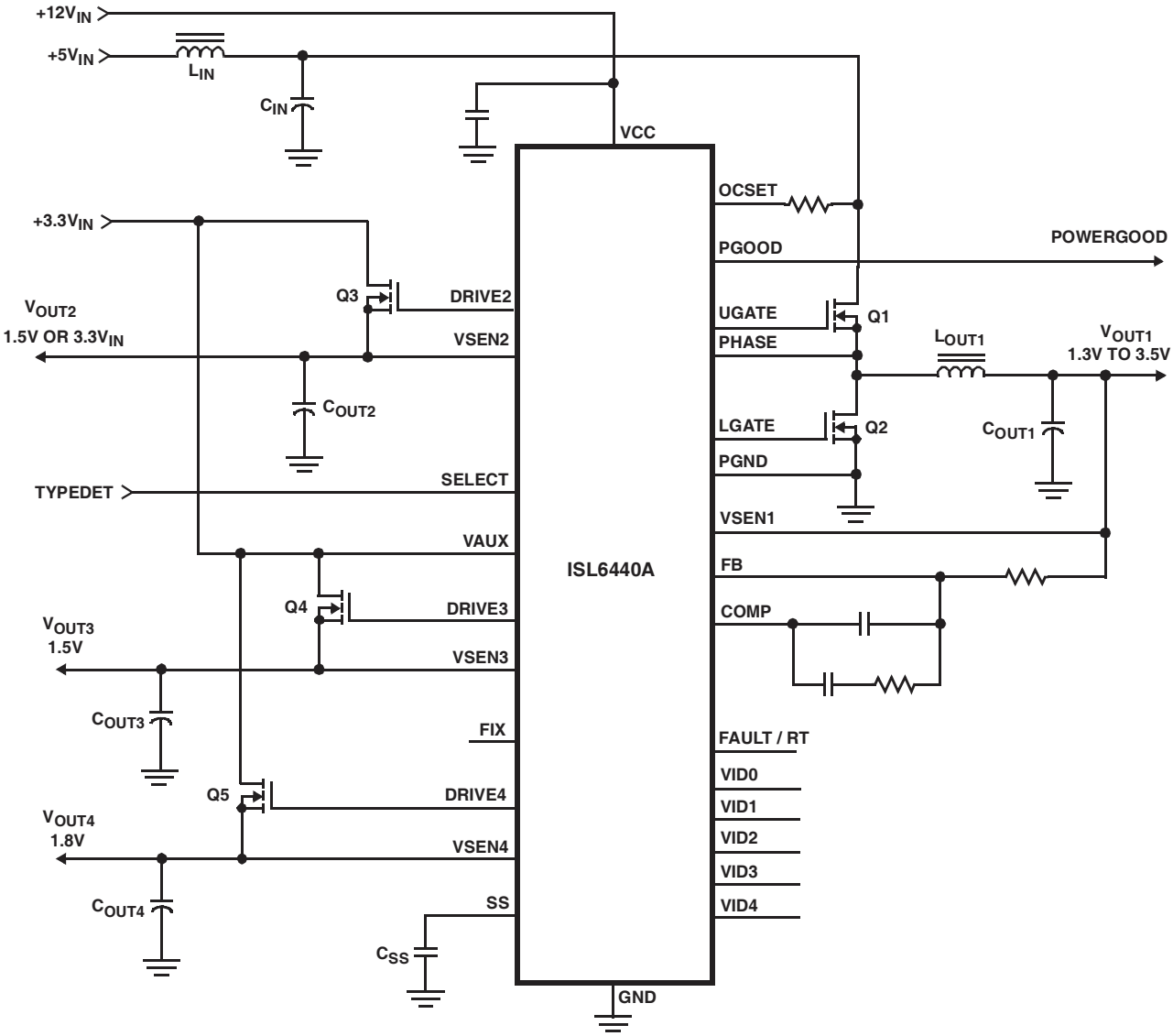
Block Diagram



Simplified Power System Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +15V
PGOOD, RT/FAULT, DRIVE, PHASE,
and GATE Voltage . . . . . GND -0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage . . . . . GND -0.3V to 7V
ESD Classification . . . . . Class 1

Operating Conditions

Supply Voltage, V_{CC} . . . . . +12V ±10%
Ambient Temperature Range . . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package 45
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications — Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{CC}	UGATE, LGATE, DRIVE2, DRIVE3, and DRIVE4 Open	-	9	-	mA
POWER-ON RESET						
Rising VCC Threshold		V_{OCSET} = 4.5V	-	-	10.4	V
Falling VCC Threshold		V_{OCSET} = 4.5V	8.2	-	-	V
Rising VAUX Threshold		V_{OCSET} = 4.5V	-	2.5	-	V
VAUX Threshold Hysteresis		V_{OCSET} = 4.5V	-	0.5	-	V
Rising V_{OCSET} Threshold			-	1.26	-	V
OSCILLATOR						
Free Running Frequency	F_{OSC}	RT = OPEN	185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ	-15	-	+15	%
Ramp Amplitude	ΔV_{OSC}	RT = Open	-	1.9	-	V_{P-P}
DAC AND BANDGAP REFERENCE						
DAC(VID0-VID4) Input Low Voltage			-	-	0.8	V
DAC(VID0-VID4) Input High Voltage			2.0	-	-	V
DACOUT Voltage Accuracy			-1.0	-	+1.0	%
Bandgap Reference Voltage	V_{BG}		-	1.265	-	V
Bandgap Reference Tolerance			-2.5	-	+2.5	%
LINEAR REGULATORS (OUT2, OUT3, AND OUT4)						
Regulation (All Linears)		Except OUT2 when SELECT > 2.0V	-	3	-	%
VSEN2 Regulation Voltage	$VREG_2$	SELECT < 0.8V	-	1.5	-	V
VSEN3 Regulation Voltage	$VREG_3$		-	1.5	-	V
VSEN4 Regulation Voltage	$VREG_4$		-	1.8	-	V
Undervoltage Level (VSEN/VREG)	$VSEN_{UV}$	VSEN Rising	-	75	-	%
Undervoltage Hysteresis (VSEN/VREG)		VSEN Falling	-	7	-	%
Output Drive Current (All Linears)		VAUX-V_{DRIVE} > 0.6V	20	40	-	mA
SYNCHRONOUS PWM CONTROLLER ERROR AMPLIFIER						

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Gain			-	88	-	dB
Gain-Bandwidth Product	GBWP		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	V/μs
PWM CONTROLLER GATE DRIVER						
UGATE Source	I_{UGATE}	VCC = 12V, V_{UGATE} = 6V	-	1	-	A
UGATE Sink	R_{UGATE}	$V_{GATE-PHASE}$ = 1V	-	1.7	3.5	Ω
LGATE Source	I_{LGATE}	VCC = 12V, V_{LGATE} = 1V	-	1	-	A
LGATE Sink	R_{LGATE}	V_{LGATE} = 1V	-	1.4	3.0	Ω
PROTECTION						
VSEN1 Overvoltage (VSEN1/DACOUT)		VSEN1 Rising	-	115	120	%
FAULT Sourcing Current	I_{OVP}	$V_{FAULT/RT}$ = 2.0V	-	8.5	-	mA
OCSET1 Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	μA
Soft-Start Current	I_{SS}		-	28	-	μA
POWER GOOD						
VSEN1 Upper Threshold (VSEN1/DACOUT)		VSEN1 Rising	108	-	110	%
VSEN1 Undervoltage (VSEN1/DACOUT)		VSEN1 Rising	92	-	94	%
VSEN1 Hysteresis (VSEN1/DACOUT)		Upper/Lower Threshold	-	2	-	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	-	0.8	V

Typical Performance Curve

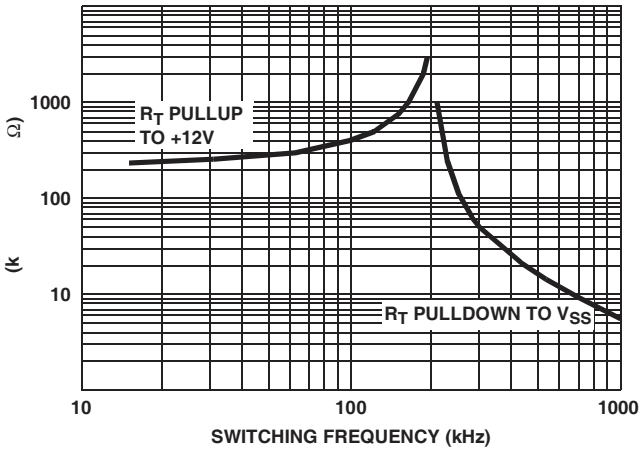


FIGURE 1. R_T RESISTANCE vs FREQUENCY

Functional Pin Descriptions

VCC (Pin 28)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for power-on reset (POR) purposes.

GND (Pin 17)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

PGND (Pin 24)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

VAUX (Pin 16)

This pin provides boost current for the linear regulators' output drives in the event bipolar NPN transistors (instead of N-Channel MOSFETs) are employed as pass elements. The voltage at this pin is monitored for POR purposes.

SS (Pin 12)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28µA current source, sets the soft-start interval of the converter.

FAULT / RT (Pin 13)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$Fs \approx 200kHz + \frac{5 \times 10^6}{R_T(k\Omega)} \quad (R_T \text{ to GND})$$

Conversely, connecting a resistor from this pin to VCC reduces the switching frequency according to the following equation:

$$Fs \approx 200kHz - \frac{4 \times 10^7}{R_T(k\Omega)} \quad (R_T \text{ to 12V})$$

Nominally, the voltage at this pin is 1.26V. In the event of an overvoltage or overcurrent condition, this pin is internally pulled to VCC.

PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within ±10% of the DACOUT reference voltage or when any of the other outputs are below their undervoltage thresholds.

The PGOOD output is open for '11111' VID code.

SD (Pin 9)

This pin shuts down all the outputs. A TTL-compatible, logic level high signal applied at this pin immediately discharges the soft-start capacitor, disabling all the outputs. Dedicated internal circuitry insures the core output voltage does not go negative during this process. When re-enabled, the IC undergoes a new soft-start cycle. Left open, this pin is pulled low by an internal pull-down resistor, enabling operation.

FIX (Pin 2)

Grounding this pin bypasses the internal resistor dividers that set the output voltage of the 1.5V and 1.8V linear regulators. This way, the output voltage of the two regulators can be adjusted from 1.26V up to the input voltage (+3.3V or +5V) by way of an external resistor divider connected at the corresponding VSEN pin. The new output voltage set by the external resistor divider can be determined using the following formula:

$$V_{OUT} = 1.265V \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

where R_{OUT} is the resistor connected from VSEN to the output of the regulator, and R_{GND} is the resistor connected from VSEN to ground. Left open, the FIX pin is pulled high, enabling fixed output voltage operation.

VID0, VID1, VID2, VID3, VID4 (Pins 7, 6, 5, 4 and 3)

VID0-4 are the TTL-compatible input pins to the 5-bit DAC. The logic states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the microprocessor core converter output voltage, as well as the corresponding PGOOD and OVP thresholds.

OCSET (Pin 23)

Connect a resistor from this pin to the drain of the respective upper MOSFET. This resistor, an internal 200µA current source, and the upper MOSFET's on-resistance set the converter overcurrent trip point. An overcurrent trip cycles the soft-start function.

The voltage at this pin is monitored for POR purposes and pulling this pin low with an open drain device will shutdown the IC.

PHASE (Pin 26)

Connect the PHASE pin to the PWM converter's upper MOSFET source. This pin represents the gate drive return current path and is used to monitor the voltage drop across the upper MOSFET for overcurrent protection.

UGATE (Pin 27)

Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

LGATE (Pin 25)

Connect LGATE to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

COMP and FB (Pin 20 and 21)

COMP and FB are the available external pins of the PWM converter error amplifier. The FB pin is the inverting input of the