2.1 Applications

The UCC2891 is suited for use in isolated telecom 48-V input systems requiring high-efficiency and high-power density for very low-output voltage, high-current converter applications, including:

- Server Systems
- Datacom
- Telecom
- DSP's, ASIC's, FPGA's

2.2 Features

The UCC2891EVM features include:

- ZVS transformer reset using active clamp technique in forward converter
- All surface mount components, double sided half brick (2.2 × 2.28 × 0.5) inches
- Complementary auxilliary drive for active clamp with programmable dead time for ZVS
- Current mode control with synchronization function
- Internal PWM slope compensation
- Start-up directly from telecom input voltage
- Synchronous rectifier output stage allows high-efficiency operation
- Programmable soft-start
- Up to 30-A dc output current
- Regulation to zero load current
- Non-latching, output overcurrent and short circuit protection
- Non-latching, Input undervoltage protection
- 1500-V isolation primary to secondary

3 UCC2891EVM Electrical Performance Specifications

The UCC2891EVM electrical performance specifications are listed in Table 1.

Table 1. UCC2891EVM Performance Summary

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Input voltage range		36	48	72	V
No load intput current	V_{IN} = 36 V, I_{OUT} = 0 A		75	100	mA
Maximum input current	V_{IN} = 36 V, I_{OUT} = 30 A		3.00	3.25	A
Input voltage ripple	V_{IN} = 72 V, I_{OUT} = 30 A		1.50	1.75	V_{P-P}
Input voltage ripple					
Output voltage	36 V ≤ V_{IN} ≤ 72 V, 0 A ≤ I_{OUT} ≤ 30 A	3.25	3.30	3.35	V
Output voltage regulation	Line regulation (36 V ≤ V_{IN} ≤ 72 V, I_{OUT} = 0 A)		0.003%		
	Load regulation (0 A ≤ I_{OUT} ≤ 30 A, V_{IN} = 48 V)		0.060%		
Output voltage ripple	V_{IN} = 48 V, I_{OUT} = 30 A		30	35	mV_{P-P}
Output load current	V_{IN} = 48 V, I_{OUT} = 30 A	0		30	A
Output current limit	36 V ≤ V_{IN}≤ 72 V			32	
Output current limit					
Switching frequency		275		325	kHz
Control loop bandwidth	36 V ≤ V_{IN} ≤ 72 V, I_{OUT} = 10 A	5		8	
Control loop bandwidth	36 V ≤ V_{IN} ≤ 72 V, 2 A ≤ I_{OUT} ≤ 30 A	30		50	°C
Peak efficiency			92%		
Full load efficiency	V_{IN} = 48 V, I_{OUT} = 30 A		89%		

4 Schematic

A schematic of the UCC2891EVM is shown in Figure 1. Terminal block J1 is the 48-V input voltage source connector and J8 is the output and return for the 3.3-V output voltage.

On the primary side, U1 is the UCC2891 shown with the necessary discrete circuitry for configuring the controller to operate at 300 kHz with the maximum duty clamp set for 0.65. The EVM is programmed to start at VIN=36 V, as determined by R11 and R12. To minimize power dissipation in the current sense, a current sense transformer, T1 is used, as opposed to simply using a sense resistor between the source of Q2 and power ground. Q2 is the primary switching MOSFET and is selected based upon VDS and low RDS(on). Q1 is the AUX (active reset) MOSFET and is selected based upon preferred package only, with only minor consideration given for $R_{DS(on)}$ and Qg. Since the active clamp used in this design is low-side referenced, Q1 must be a P-channel type MOSFET. The reason for this is further explained in application note SLUA299[2]. C9 is the clamp capacitor used to maintain a constant dc voltage. The input voltage is subtracted from the clamp voltage to allow transformer reset during the active clamp period.

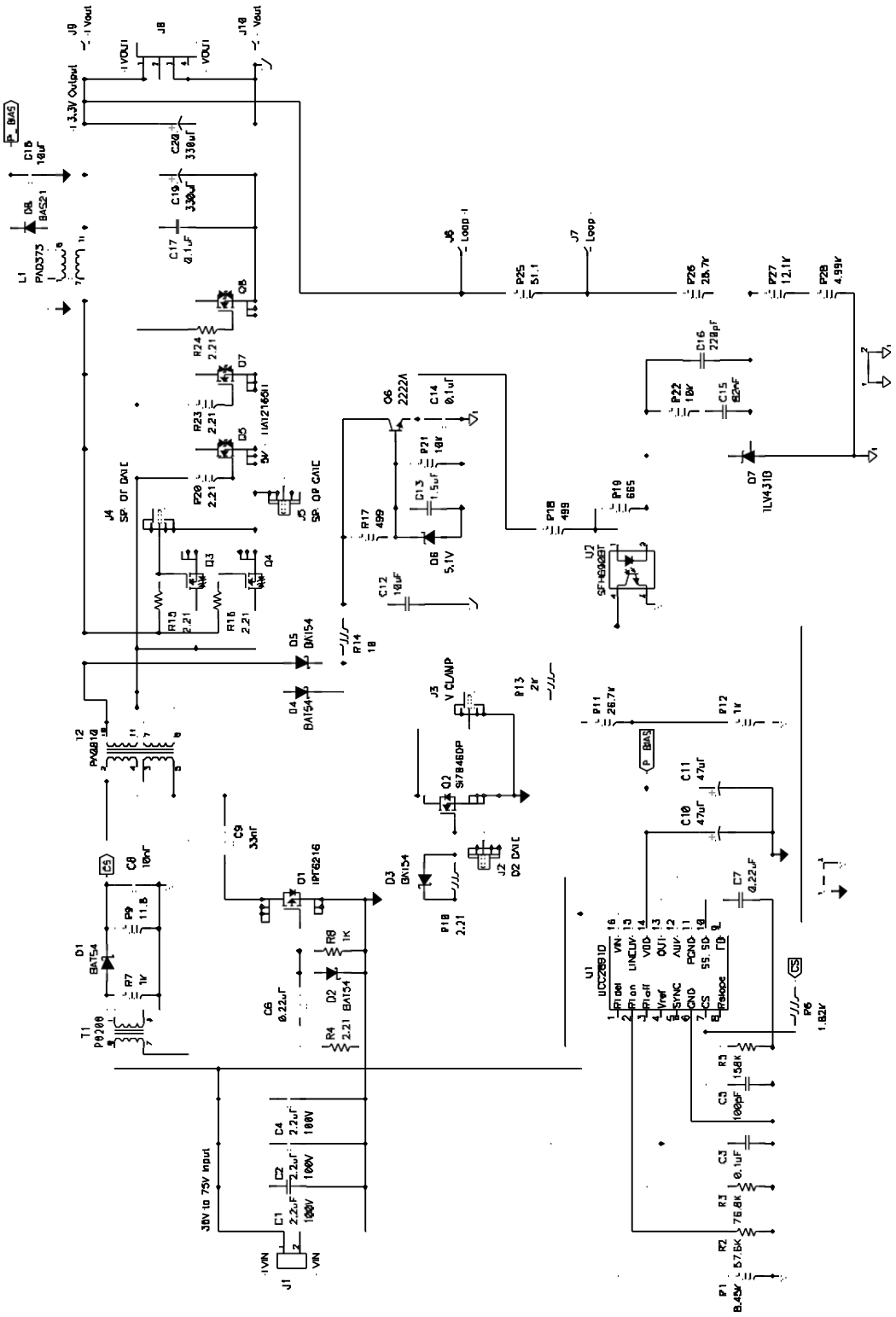


Figure 1. UCC2891EVM Schematic

High efficiency is achieved using self-driven synchronous rectification on the secondary side. Q3 and Q4 are placed in parallel and make up the forward synchronous rectifier (SR), while the reverse SR is made up of the parallel combination of Q5, Q7 and Q8. If the duty cycle were limited to 50% then the reverse SR could be reduced to only two parallel MOSFETs, but since these devices are operating near 60% duty cycle during the freewheel mode, they carry a higher average current than seen by Q3 and Q4. The output inductor L1 has a coupled secondary, referenced to the primary side, used to provide bootstrapping voltage to U1. A stable bias for the optocoupler, U2 is provided by the series pass regulator made up of D6, Q6 and some associated filtering.

Scope jacks J2 and J3 allow the user to measure the gate-to-source and drain-to-source signals for Q2, the primary MOSFET. J4 and J5 allow convenient access to the gate drive signals of each SR on the secondary side. J6 and J7 are available allowing the option of using a network analyzer to non-invasively measure the control to output loop gain and phase.

5 EVM Test Setup

Figure 2 shows the basic test set up recommended to evaluate the UCC2891EVM.

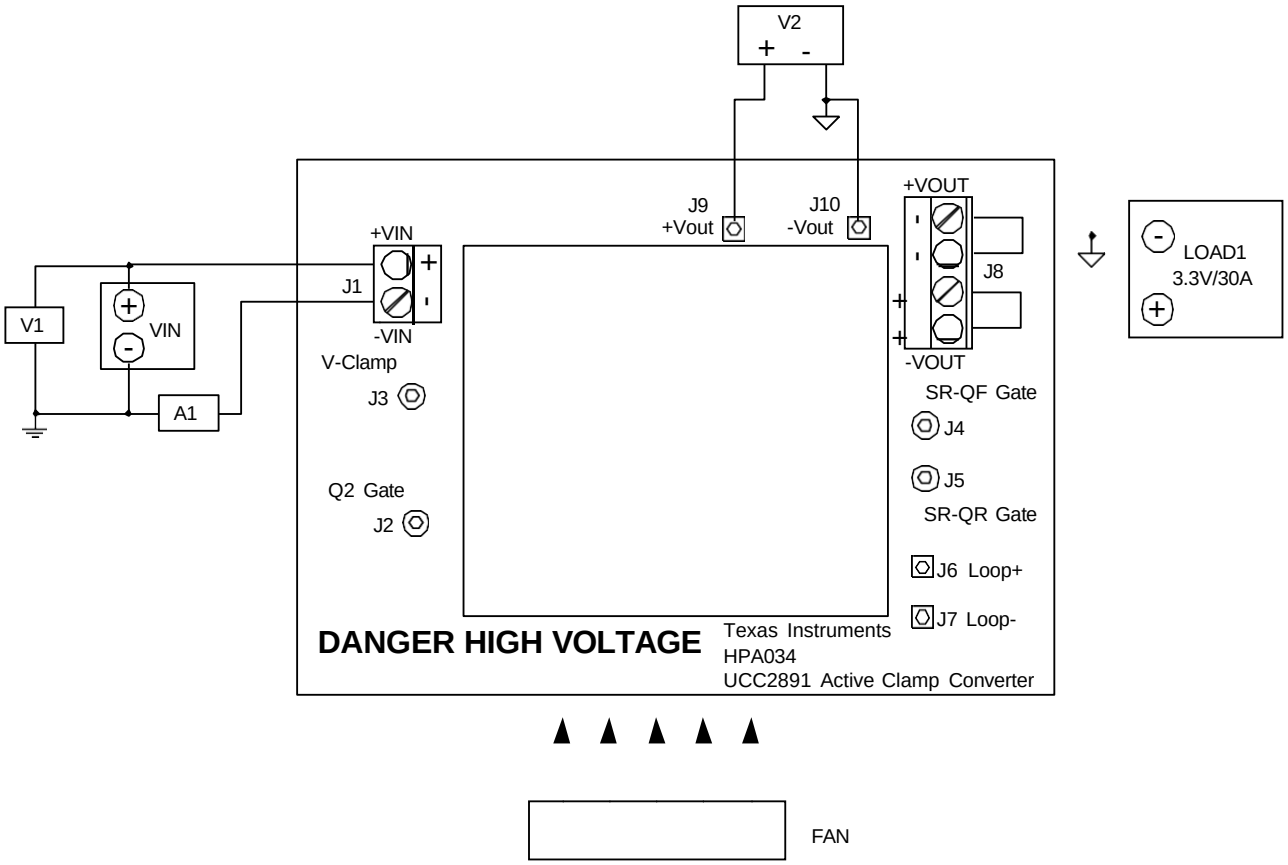


Figure 2. Recommended EVM Test Configuration

以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：https://d.book118.com/048022063117006045