

6ED003L06-F Gate Drive-IC for three-phase converters

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1 Short Description

The 6ED003L06-F is a high voltage gate drive IC for three-phase converters up to a maximum blocking voltage of 600V. The converters can be used for example in drives applications which are basing on induction machines (IM) or brushless DC motors. The 6ED003L06-F is designed in silicon-on-insulator-technology (SOI). This technology provides a high ruggedness against negative voltage spikes and noise.

This application note gives an overview of the technological characteristics. It also describes the most important sections in terms of the application and gives design recommendations for a proper operation of the device in the application.

6ED003L06-F is similar to use as IR2136 and its derivates. It is compatible to the same footprint, but not compatible in terms of the internal thresholds, which may concern the external circuitry. Please refer here to the product specifications of 6ED003L06-F.

2 Technology Characteristics

SOI is the abbreviation of **Silicon-On-Insulator** and is an advanced technique for MOS/CMOS fabrications. It differs from the conventional bulk process by placing the active transistor layer on the top of an insulator, as shown in **Figure 1**.

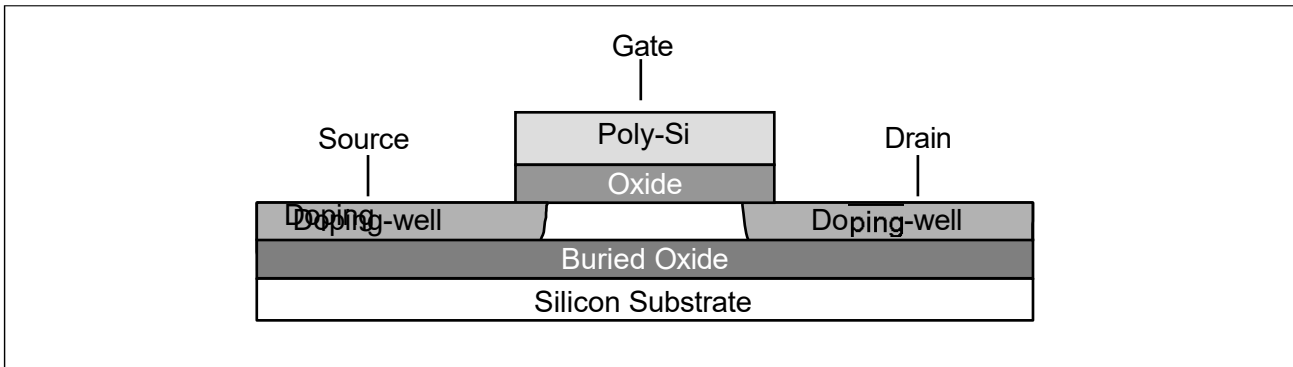


Figure 1 Cross section of a FET in SOI-technology

The silicon is separated by a buried silicon oxide layer to one layer on the top and the other on the bottom. The one on the top, which is the silicon film, is used to produce the transistor and the one on the bottom is used as the silicon substrate. The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate and hence reduces the parasitic capacitance tremendously. Moreover, this insulation barrier disables leakage or latch-up currents between adjacent devices.

A major technological advantage of the Thin-Film-SOI technology is the easy way of lateral insulation of elements inside the silicon film. The thin film technology allows each device to be separated from all other devices by a simple local oxidation (LOCOS) process. Thus, there is no need for CMOS-wells for preventing the "latch-up" effect and reducing the chip size.

The small size of PN-junctions inside the thin silicon film leads to higher switching speed, lower leakage currents and consequently higher temperature stability. In order to obtain a proper body contact for the thin SOI-MOS transistor the channel doping is extended and connected to a common source contact (split source contact). Hence the thin-film SOI-MOS transistor exhibits an anti-paralleled diode that safeguards the device in case of polarity reversal.

In spite of the thin drift regions inside the silicon films, reasonable low on-resistance per area is achieved. This allows a cost effective layout of the output driver transistors.

The SOI technology is also implemented for the 600 V level-shift transistors and high-voltage diodes. The 600V-NMOSFET is based on the low-voltage SOI-NMOSFET structure in conjunction with a very long Drain-extension. The buried oxide insulation barrier cuts off parasitic current paths between substrate and silicon film. This prevents the latch-up effect even in case of high dv/dt switching under elevated temperature and hence provides improved robustness.

Besides these improvements, the thin-film SOI-technology provides additional benefits like lower power consumption and higher immunity to radioactive radiation or cosmic rays.

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