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Contents

1. LVDS SERDES Transmitter/Receiver IP Cores User Guide

The low-voltage differential signaling serializer or deserializer (LVDS SERDES) IP cores (ALTLVDS_TX and ALTLVDS_RX) implement the LVDS SERDES interfaces to transmit and receive high-speed differential data. You can configure the features of these IP cores using the IP Catalog and parameter editor.

Related Information

- LVDS SERDES Transmitter/Receiver IP Cores User Guide Archives on page 53
  Provides a list of user guides for previous versions of the ALTLVDS_TX and ALTLVDS_RX IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.
- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.

1.1. Features

Table 1. ALTLVDS_TX and ALTLVDS_RX Features

This table lists the features of the ALTLVDS_TX and ALTLVDS_RX IP cores.

Note: The ALTLVDS_TX and ALTLVDS_RX IP cores are not available for the Intel® Stratix® 10, Intel Arria® 10, and Intel Cyclone® 10 GX device families. For Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices, use the Intel FPGA LVDS SERDES core.

IP Core	Features	Supported devices
ALTLVDS_TX and ALTLVDS_RX	Parameterizable data channel widths	All Stratix, Arria, and Cyclone series devices.
	Parameterizable serializer/deserializer (SERDES) factors	
	Registered input and output ports	
	Support for external phase-locked loops (PLL)	
	PLLs sharing between transmitters and receivers	
	PLL control signals	
ALTLVDS_RX Only	Dynamic phase alignment (DPA) mode support(1)	All Stratix and Arria series devices.
	Soft clock data recovery (CDR) mode support(2)	
	DPA PLL calibration support(1)	All Stratix series devices.

Note: Intel recommends implementing the Bus LVDS (BLVDS) I/O with user logic, instead of the ALTLVDS_TX and ALTLVDS_RX IP cores.

Related Information

- Altera LVDS SERDES IP Core User Guide
- AN 522: Implementing Bus LVDS Interface in Supported Altera Device Families

1.1.1. Resource Utilization and Performance

The Intel Quartus® Prime software configures the PLL according to the settings you apply in the ALTLVDS_RX and ALTLVDS_TX parameter editor. All supported devices provide the option to use an external PLL, which requires you to enter the appropriate PLL parameters.

When the ALTLVDS_TX and ALTLVDS_RX IP cores are instantiated without the external PLL option, they use one PLL per instance. During compilation, if directed to do so, the compiler tries to merge PLLs whenever possible to minimize resource usage.

The Arria, Cyclone, Hardcopy, and Stratix series support the **Use Shared PLL(s) for Receiver and Transmitter** option to allow both the ALTLVDS_TX and ALTLVDS_RX IP cores to share a PLL. The Intel Quartus Prime software lets the transmitter and receiver share the same PLL when both use identical input clock sources, identical `pll_areset` sources, identical deserialization factors, and identical output settings. For example, the Intel Quartus Prime software displays the following message when the PLL merges successfully:

```
Info: Receiver fast PLL <lvds_rx PLL name>
                and transmitter fast PLL <lvds_tx PLL name> are merged
                together
```

The Intel Quartus Prime software displays the following message when it cannot merge the PLLs for the LVDS transmitter and receiver pair in the design:

```
Warning: Can't merge transmitter-only fast PLL
                <lvds_tx PLL name> and receiver-only fast PLL <lvds_rx PLL
                name>
```

Note: One cause for the warning message is that PLLs that are driven by different clocks cannot be merged. For PLL merging to happen, the input clocks and the settings on the outputs must be identical.

Note: To use the LVDS I/O standard in the I/O Bank 1 of Cyclone III, Cyclone IV E, and Intel Cyclone 10 LP devices, ensure that you set the **Configuration device I/O voltage** to 2.5 V, or Auto in the **Device and Pin Options** dialog box of the Intel Quartus Prime software.

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(1) DPA is available starting from Stratix GX onwards. The first generation Stratix device family does not support DPA.

(2) CDR is not available in the first generation Stratix device family and the Stratix II device family. However, soft-CDR is available in all other Stratix series including Stratix GX and Stratix II GX..

For the Stratix series, the side I/O banks contain dedicated SERDES circuitry, which includes the PLLs, serial shift registers, and parallel registers. The transmit and receive functions use varying numbers of LEs depending on the number of channels, serialization, and deserialization factors. For best performance, manually place these LEs in columns as close as possible to the SERDES circuitry and LVDS pins. By default, the Intel Quartus Prime software places these LEs automatically during placement and routing.

Note: When dedicated SERDES is implemented in LVDS transmitter, the SERDES is directly connected to the LVDS transmitter; therefore, the output of the transmitter cannot be assigned to single-ended I/O standards.

Note: The Intel Quartus Prime software reports the number of LEs used per ALTLVDS block in the **Fitter Resource Utilization by Entity** section in the **Resource** section of the **Compilation Report**.

The Cyclone series uses DDIO registers as part of the SERDES interface. Because data is clocked on both the rising edge and falling edge, the clock frequency must be half the data rate; therefore, the PLL runs at half the frequency of the data rate. The core clock frequency for the transmitter is data rate divided by serialization factor (J). For the odd serialization factors, depending on the output clock-divide factor (B) and device family, an optional core clock frequency of data rate divided by two times the serialization factor (J) is also available.

Use the following tables to determine the clock and data rate relationships.

Table 2. Cyclone Series ALTLVDS Transmitter Clock Relationships

Clock Type	J = Even	J = Odd
Fast Clock	Data Rate / 2	Data Rate / 2
Slow Clock (outclock)	Data Rate / 2 * B	Data Rate / 2 * B
Core Clock	Data Rate / J	Data Rate / J

Table 3. Cyclone Series ALTLVDS Receiver Clock Relationships

Clock Type	J = Even	J = Odd
Fast Clock	Data Rate / 2	Data Rate / 2
Slow Clock (outclock)	Data Rate / J	Data Rate / J

Related Information

- ALTPLL (Phase-Locked Loop) IP Core User Guide
- Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide

1.2. Parameter Settings

You can parameterize IP cores using the IP Catalog and parameter editor.

Related Information

Command Line Interface Parameters on page 17

1.2.1. ALTLVDS_TX Parameter Settings

On the **General** page (page 3) of the parameter editor, depending on the device you selected, you can configure the following options:

- Implement the SERDES circuitry in LEs (logic cells) or dedicated (hard) SERDES block
- Use internal PLL or external PLL

The selections you make on the **General** page determine the features available on the remaining pages of the parameter editor.

The options on pages 1 and 2a of the parameter editor are the same for all supported device families.

The following table lists the parameter settings for the ALTLVDS_TX IP core.

Table 4. ALTLVDS_TX Parameter Settings

Option	Description
General (page 3)	
Implement Deserializer circuitry in logic cells	Turn on this option to implement the SERDES circuitry in logic cells. The transmitter starts its operation on the first fast clock edge after the PLL is locked. This option is intended for slow speeds. The byte alignment might be different from the dedicated SERDES implementation. Turn off this option to use the dedicated SERDES circuitry in the device. When you implement the dedicated SERDES in the LVDS transmitter, the SERDES connects to the LVDS transmitter; therefore, the output of the transmitter cannot be assigned to single-ended I/O standards. This feature is supported in Arria GX, Arria II GX, Arria II GZ, HardCopy® II, HardCopy III, HardCopy IV, Stratix, Stratix GX, Stratix II, Stratix II GX, Stratix III, and Stratix IV devices. In Cyclone series, except Cyclone V devices, the SERDES is always implemented in logic cells. Cyclone V devices contain dedicated SERDES circuitry. If you turn on this option, there is additional delay for the `tx_outlock` signal to be stable after the `tx_locked` signal is asserted. Perform gate-level simulation to determine the time for the `tx_outclock` signal to stabilize.
What is the number of Channels?	Number of output channels available for the LVDS transmitter. If the required number of channels is not available in the list, type the desired number. For example, if the number of channels is **44**, the port created is `tx_out[43..0]`. The legal values depend on the pins available in the device. For the legal values for your device, refer to the relevant device handbook.
What is the deserialization factor?	Determines the number of parallel bits from the core that the transmitter serializes and sends out. For example, if the deserialization factor is **10** and the number of output channels is **1**, the transmitter serializes every 10 parallel bits into a single output channel. If the deserialization factor is **10** and the number of channels is **44**, the port created is `tx_in[439..0]`. For the valid deserialization factors for your device, refer to the relevant device handbook.

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Option	Description
	When the `divide_by_factor` port shown in the parameter editor is identical to the deserialization factor, the parameter editor disables the 50/50 duty cycle for x5, x7, and x9 modes.
Use External PLL	Turn on this option to use an external PLL to clock the SERDES transmitter. When you turn on this option, the options on the **Frequency/PLL** settings page are disabled. You must use a separate PLL to provide the clocking source and make the necessary connections. You must ensure your circuit has the correct input and functionality to generate an appropriate clock frequency and is correctly connected to the LVDS transmitter. When you have a deserialization factor of two, the IP core bypasses SERDES and implements the SERDES functionality in DDR registers. Your design requires a deserialization factor of at least four to turn on the external PLL option. If you turn off this option, the IP core automatically implements an internal PLL to clock the ALTLVDS_TX block. For Stratix and Stratix GX devices, if you implement SERDES for your LVDS transmitter using a dedicated SERDES block, you do not have the option to use an external PLL.
Use 'tx_data_reset' input port	This option is available when you implement the LVDS in logic cells. When you turn on this option, it adds an input port in the IP core, which when asserted asynchronously resets all the logic in the ALTLVDS_TX IP core excluding the PLL.
Frequency/ PLL Settings (page 4) The options on this page are available only when you are using internal PLL	
What is the output data rate?	Specifies the data rate for the output channel of the transmitter, in Megabits per second (Mbps). For data rate ranges, refer to the Device Data Sheet chapter in the relevant device handbook. This option determines the legal value of the input clock rate.
Specify input clock rate by	Specifies the clock frequency (`tx_inclock` port) or the clock (`inclock_period` parameter) going into the internal PLL. The legal values depend on the output data rate selected.
What is the phase alignment of 'tx_in' with respect to the rising edge of 'tx_inclock'? (in degrees)	Determines the phase alignment of the data transmitted by the core logic array with respect to the `tx_inclock` clock. The available values are **0.00**, **22.50**, **45.00**, **67.50**, **90.00**, **112.50**, **135.00**, **157.50**, **180.00**, **202.50**, **225.00**, **247.50**, **270.00**, **292.50**, **315.00**, and **337.50**. The values for this option are device dependent.
Use 'tx_pll_enable' input port	Turn on to control the enable port of the fast PLL that the IP core uses with this function. If the transmitter shares the PLL with other ALTLVDS blocks, and uses the `tx_pll_enable` port, you must use this port in all the IP core instances and tie the signals together in the design file. If you use a PLL-enabled port in one IP core instance and not another, the PLLs are not shared, and a warning appears during compilation.
Use 'pll_areset' input port	Turn on to control the asynchronous reset port of the PLL that the IP core uses with this function. When the transmitter shares the PLL with other ALTLVDS blocks and uses the `pll_areset` port, you must use this port in all the IP core instances and tie the signals together

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Option	Description
	in the design file. If you use the `pll_areset` port in one IP core instance only, the PLLs are not shared and a warning appears during compilation. The PLL must be reset to set the output clock phase relationships correctly when the PLL loses lock, or if the PLL input reference clock is not stable when the device completes the configuration process.
Align clock to center of data window	Turn on this option to add a phase shift of 90° to the clock, which center-aligns the clock in the data. Turn on this option for PLL merging if you also turn on this option for the receiver. This option is available only for Arria GX, Stratix II, Stratix II GX, and HardCopy II devices when you implement the SERDES in logic cells, and for Cyclone II devices.
Enable self-reset on lost lock in PLL	Turn on this option to reset the PLL automatically whenever the PLL loses lock. This option is available only for Arria II GX, Arria II GZ, HardCopy III, HardCopy IV, Stratix III, and Stratix IV devices when SERDES is implemented in logic cells, and for Cyclone lll, Cyclone IV, and Intel Cyclone 10 LP devices.
Use shared PLL(s) for receivers and transmitters	Turn on this option for your LVDS receivers and transmitters to share the same PLL. Turn on this option if the LVDS receivers and transmitters use the same input clock frequency, deserialization factor, and data rates.
Register 'tx_in' input port using	Turn on this option to specify whether input registers are clocked by the `tx_inclock` signal or `tx_coreclock` signal. When the PLLs are shared, connect the `tx_inclock` signal to the same reference clock as the receiver function. For example, if the `tx_inclock` signal is connected to a 500-MHz input reference clock, and the parallel data rate is not 500 MHz, register the parallel data using the `tx_coreclock` signal that runs at the output serial data rate divided by the deserialization factor. This frequency matches the parallel data rate from the FPGA core. If you turn off this option, a warning message appears that directs you to pre-register the inputs in the logic that feeds the transmitter. When you use the Cyclone series with the ALTLVDS_TX and ALTLVDS_RX IP cores, the interface always sends the most significant bit (MSB) of your parallel data first. When you use the ALTLVDS_TX IP core, you might get setup timing violations when you use the `tx_inclock` signal to register the data that feeds the SERDES blocks. The ALTLVDS_TX IP core gives you the choice to register the `tx_in[]` data with either the `tx_inclock` or `tx_coreclock` signal. The default setting is `tx_coreclock`. Using the `tx_coreclock` signal to register the data before it feeds the SERDES is the better choice, because it has the optimal phase position to register the data with respect to the high-speed clock that drives the SERDES. Your setup timing violations are eliminated when you use the `tx_coreclock` signal instead of the `tx_inclock` signal to register the data in the ALTLVDS_TX IP core. Additionally, you get better timing margins when you use the `tx_coreclock` signal instead of the `tx_inclock` signal, even if you do not have timing violations.
Transmitter Settings (page 5)	

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Option	Description
Use 'tx_outclock' output port	The `tx_outclock` signal is associated with the serial transmit data stream. Every `tx_outclock` signal goes through the shift register logic, excluding the following parameter configurations: • When the `outclock_divide_by` signal equals to `1`, or • When the `outclock_divide_by` signal equals to `deserialization_factor` signal (for odd factors only) and the `outclock_duty_cycle` signal is **50**.
What is the outclock divide factor (B)?	Specifies the frequency of the `tx_outclock` signal as the transmitter output data rate divided by the outclock divide factor (B). For the legal values, refer to the relevant device handbook. For a SERDES factor of **5** and **9**, the outclock divide factors available are **1**, **5**, and **9**. The divide factor of **2** is not available. For Cyclone II devices and later, when the `implement_in_les` parameter is `ON`, the `outclock_duty_cycle` of **50** is not supported in the following parameter configurations: • deserialization_factor signal is **5**, **7**, or **9** • `outclock_divide_by` signal equals to `deserialization_factor` • `outclock_multiply_by` is **2**
Specify phase alignment of 'tx_outclock' with respect to 'tx_out'	Specifies the phase alignment of `tx_outclock` signal with respect to the `tx_out` signal. This option is available only if you use the `tx_outclock` signal.
What is the phase alignment of 'tx_outclock' with respect to 'tx_out'?	The available values are **0.00**, **22.50**, **45.00**, **67.50**, **90.00**, **112.50**, **135.00**, **157.50**, **180.00**, **202.50**, **225.00**, **247.50**, **270.00**, **292.50**, **315.00**, and **337.50**. The values for this option are device dependent. This option is available only when you implement the SERDES in logic cells and uses the `tx_outclock` signal.
What is the outclock duty cycle?	The default value is **50**. The `outclock_duty_cycle` of **50** is not supported when: • `deserialization_factor` signal is **5**, **7**, or **9** • `outclock_divide_by` signal equals to `deserialization_factor` • `outclock_multiply_by` is **2**
Use 'tx_locked' output port	Allows you to monitor the lock status of the PLL. The status of the lock port is identical for the transmitter and receiver when the IP core uses shared PLLs.
Use 'tx_coreclock' output port	Turn on this option to show the core clock frequency during simulation. Enables the transmitter core clock signal to the registers of all the logic that feeds the LVDS transmitter function. If any other clock feeds the transmit function, your design must implement the clock domain transfer circuitry. You must add a false path constraint from the `slow_clock` signal to the `fast_clock` signal in the ALTLVDS_TX IP core whenever the faster `core_clock` signal implementation is used for odd deserialization factors.
What is the clock resource used for 'tx_coreclock'?	Specifies the clock resource type fed to the `tx_coreclock` signal. Allowed values are **Auto selection** (the Compiler determines the type), **Global clock**, and **Regional clock**. The default value is **Auto selection**.

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