VESA®

VSIS™ Standard

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Video Signal Standard (VSIS)

Version 1, Rev. 2

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Purpose

To establish the standard analog video signal characteristics for today's graphics cards and display monitors.

Summary

To date, the graphics controller output signals that drive the display monitor have not been well defined. H and V sync signals are defined only as TTL. The display side has the same problem, as each design may have been optimized to correct for certain signal deficiencies from particular graphics controllers. This document will lay the groundwork that both graphics controller and monitor designers can use to achieve compatible designs.

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Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product that incorporates the Video Signal Standard, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with clarification. All comments or reported errors should be submitted in writing to VESA using one of the following methods:

- Fax: direct this note to Technical Support at VESA
- Email: support@vesa.org
- Mail to: Technical Support
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Revision History

Version 1.0 -- September 1999

Initial release of the standard

Version 1, Rev. 1 -- March 2000

Document revised throughout, for was condition see previous release.

Version 1, Rev. 2 – December 2002

Revised copyright date, redefined Sync signal testing Section 2.4, replaced Figure 1 to improve clarity. Revised Table 2, Changed Max Luminance Voltage tolerance to +0.070 / -0.035; to Table 3, added Note 1. Revised Acknowledgement List to recognize input from other sources. Added Appendix B referencing tests from FPDM2.

Acknowledgments

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Joe Goodart, Workgroup Leader	Dell Computer Corp.	Michael H. Brill	NIDL
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significant time and effort.

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1. Introduction

Display graphics controller technology has leapt forward in the last 10 years at a break-neck pace. Displays have gone from VGA to 1600 x 1200@85Hz and beyond. Graphics controllers have increased performance up to fast 3D imagery with 32-bit pixel depth. However, the signal path between the graphics controller and display monitor has remained the same for more than 10 years. With new graphics ASICs running at 2.5 volts, there is no longer any margin left in the TTL synchronization circuits. With current high bandwidth designs, display signals have little margin left, resulting in monitor jitter and poor front of screen definition. Consequently, there have often been last minute patches by both display vendors and graphics card companies just to get products to work.

This document will give monitor/graphics vendors a starting point from which to address these issues. By using these specifications as a guideline, industry designers will be able to master the art of good signal integrity. This will benefit the industry as a whole, as well as the end user.

1.1 Compliance with standard

If a supplier does not wish to specify compliance with the standard at the minimum pixel clock period, then the supplier may alternatively specify a longer pixel clock period.

1.2 Related VESA documents

VESA Display Specifications and Test Procedures (DSTP) Version 1.0 Rev 1.0 - Oct. 3, 1996
VESA Display Data Channel Standard (DDC) Version 3 - Dec.15, 1997
VESA Enhanced Display Data Channel Standard (E-DDC) Version 1.0 - Sept. 2, 1999
VESA Flat Panel Display Measurements Standard, Version 2.0 – June 1, 2001