F-Tile Serial Lite IV Intel® FPGA IP Design Example User Guide

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1. About the F-Tile Serial Lite IV Intel® FPGA IP Design Example User Guide

This document provides features, usage guidelines, and functional description of the F-Tile Serial Lite IV Intel® FPGA IP design examples using F-tile transceivers in Agilex™ 7 devices.

Intended Audience

This document is intended for the following users:

- Design architects to make IP selection during system level design planning phase.
- Hardware designers when integrating the IP into their system level design.
- Validation engineers during system level simulation and hardware validation phase.

Acronyms and Glossary

Table 1. Acronym List

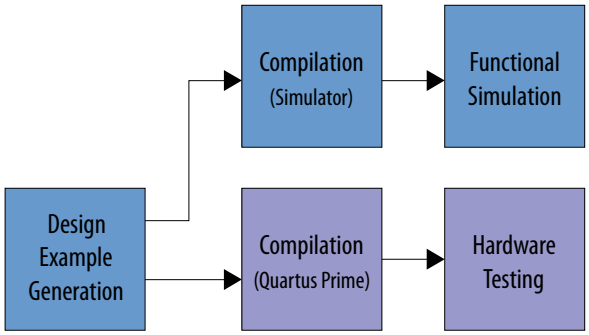
Acronym	Expansion
CW	Control Word
RS-FEC	Reed-Solomon Forward Error Correction
PMA	Physical Medium Attachment
TX	Transmitter
RX	Receiver
PAM4	Pulse-Amplitude Modulation 4-Level
NRZ	Non-return-to-zero
PCS	Physical Coding Sublayer
MII	Media Independent Interface
XGMII	10 Gigabit Media Independent Interface
DL	Deterministic Latency
DLW	Deterministic Latency Word
DLCW	Deterministic Latency Control Word
RBD	Release Buffer Delay

2. Quick Start Guide

The F-Tile Serial Lite IV Intel FPGA IP provides the ability to generate design examples for selected configurations.

The F-Tile Serial Lite IV Intel FPGA IP design example for Agilex 7 devices features a simulation testbench and a hardware design that supports compilation and hardware testing. The design example demonstrates loopback mode designs in basic or full mode for duplex configurations.

Figure 1. Development Stages for the Design Example



2.1. Design Example Block Diagram

Figure 2. High-Level Block Diagram for Agilex 7 Design Examples

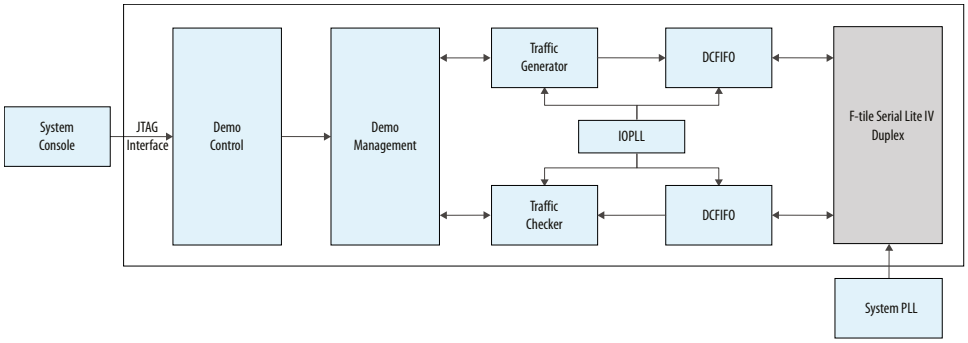


Table 3. Design Example Components

Component	Description
F-Tile Serial Lite IV Intel FPGA IP	The F-Tile Serial Lite IV Intel FPGA IP in this design example supports streaming or packet transfer mode with the following features: • For FHT transceiver type: — 48 Gbps to 58 Gbps and 96 Gbps to 116 Gbps per lane with a maximum of four PAM4 lanes. — 24 Gbps to 29 Gbps and 48 Gbps to 58 Gbps per lane with a maximum of four NRZ lanes. • For FGT transceiver type: — 20 Gbps to 58 Gbps per lane with a maximum of 12 PAM4 lanes. — 1 Gbps to 32 Gbps per lane with a maximum of 16 NRZ lanes for duplex and simplex designs. The F-Tile Serial Lite IV Intel FPGA IP accepts data from the traffic generator and formats the data for transmission. The F-Tile Serial Lite IV Intel FPGA IP also receives data from the link, strips the headers, and sends it to the traffic checker for analysis. You generate the IP using the parameter editor in the Quartus® Prime Pro Edition software.
System Console	The System Console is an Quartus Prime tool that provides a user-friendly interface for you to do first-level debugging and monitor the status of the IP, and the traffic generator, and checker.
Demo control	The demo control module consists of Avalon® memory-mapped pipeline bridges connected to the transceiver reconfiguration and the demo management interfaces. The design also instantiates the JTAG master, parallel input/output (PIO), and ISSP (In-system Source and Probe) modules for System Console debugging purposes.
Demo management	The demo management module implements control and status registers (CSRs) to control, monitor the design operation, and log errors that occur during the operation.
User clock—IOPLL	For Agilex 7 F-tile devices, the design example uses an IOPLL to generate a user clock to transmit data to the F-Tile Serial Lite IV IP. The design uses the `iopll_ref_clk` clock signal as an IOPLL reference clock to connect to the clock generator. *Important:* The `iopll_ref_clk` should have the same frequency as the `pll_refclk` and come from the same clock module.
Traffic generator	The traffic generator generates traffic in a deterministic format to verify that the link transmits data correctly.
Traffic checker	The traffic checker performs inspections to verify that the received data is in the expected format.
Dual-clock FIFO (DCFIFO)	The DCFIFO blocks handle data streaming and control signals for clock crossing between different clock domains.
System PLL	The system PLL drives the F-Tile Serial Lite IV Duplex and Simplex module and is driven to the same frequency as the `iopll_ref_clk` clock signal.

Related Information

- Traffic Generator on page 15
- Traffic Checker on page 16
- DCFIFO on page 17

2.2. Hardware and Software Requirements

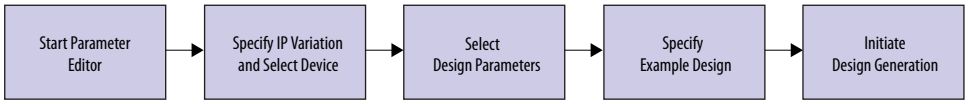
Intel uses the following software and hardware to test the design examples in a Linux system:

- Quartus Prime Pro Edition software version 24.1
- VCS*, VCS MX, Xcelium*, Riviera-PRO*, ModelSim*, or QuestaSim* simulators
- Agilex 7 I-Series Transceiver-SoC Development Kit for hardware testing

2.3. Generating the Design

You can use the IP parameter editor in the Quartus Prime Pro Edition software to generate the design example.

Figure 3. Generating the Design Flow



To generate the design example from the IP parameter editor:

1. In the **Tools ➤ IP Catalog**, locate and select **F-Tile Serial Lite IV Intel FPGA IP**. The IP parameter editor appears.
2. Specify the parameters for your design.
3. Click the **Generate Example Design** button.

The software generates all design files in the sub-directories. You need these files to run simulation, compilation, and hardware testing.

Related Information

Directory Structure on page 8

2.3.1. Design Example Parameters

The F-Tile Serial Lite IV Intel FPGA IP parameter editor includes an *Example Design* tab for you to specify parameters before generating the design example.

Figure 4. Example Design Tab

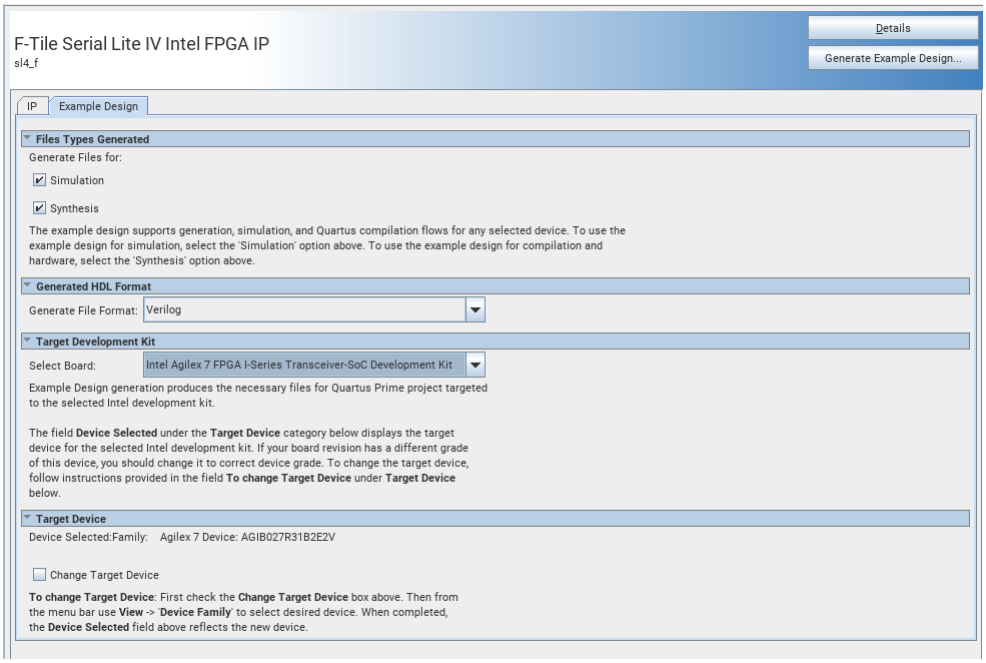


Table 4. Parameters in the Example Design Tab

Parameter	Description
Generate Files for	The IP generates the necessary design example files for simulation and compilation. Simulation—select this option to generate the necessary design simulation files. Synthesis—select this option to generate the necessary design synthesis files. Use these files to compile the design in the Quartus Prime Pro Edition software for hardware testing.
Generate File Format	The format of the RTL files for simulation—Verilog or VHDL.
Select Board	Supported hardware for design implementation. When you select an Intel FPGA development board, the **Target Device** is the one that matches the device on the Development Kit. If this menu is grayed out, there is no supported board for the options that you select. **Agilex 7 I-Series Transceiver-SoC Development Kit**: This option allows you to test the design example on the selected Agilex 7 I-Series Transceiver-SoC development kit. *Note:* This option is only available when your target device is: • AGIB027R31B1E2V for FHT • AGIB027R31B2E2V for FGT **No Development Kit**: This option excludes the hardware aspects for the design example.
Change Target Device	Select a different device grade for Intel FPGA IP development kit. For device-specific details, refer to the device datasheet on the Intel FPGA website.

2.3.2. Directory Structure

The Quartus Prime Pro Edition software generates the design example files in the following folders:

- `<user_defined_design_example_directory>/ed_sim`
- `<user_defined_design_example_directory>/ed_synth`
- `<user_defined_design_example_directory>/ed_hwtest`

The following diagrams show the directories that contain the generated files for the design example.