First Edition
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LCD Module Technical Specification

Final Revision
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Type No. **T-51756D121J-FW-A-AA**

Approved by (Quality Assurance Division)

Checked by (ACI Engineering Division)

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No.	Item	Page
--	CONTENTS	1
1	OVERVIEW	2
2	ABSOLUTE MAXIMUM RATINGS	3
3	ELECTRICAL CHARACTERISTICS	3
4	INTERFACE PIN CONNECTION	6
5	INTERFACE TIMING	7
6	BLOCK DIAGRAM	11
7	MECHANICAL SPECIFICATION	12
8	OPTICAL CHARACTERISTICS	14
9	RELIABILITY TEST CONDITION	16
10	INSPECTION STANDARDS	17
11	HANDLING PRECAUTIONS FOR TFT-LCD MODULE	18
--	PACKAGING SPECIFICATION	21
--	PRODUCT NUMBER LABELING FORMS	25
--	LAMP UNIT FOR 12.1" XGA	27

1. OVERVIEW

T-51756D121J-FW-A-AA is 12.1" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs, control circuit, and backlight unit.
By applying 6 bit digital data, 1024 × 768, 260 K-color images are displayed on the 12.1" diagonal screen. Input power voltage is single 3.3V for LCD driving.

Inverter for backlight is not included in this module. General specifications are summarized in the following table:

ITEM	SPECIFICATION
Display Area (mm)	245.76 × 184.32 (12.106-inch diagonal)
Number of Dots	1024 × 3 (H) × 768 (V)
Pixel Pitch (mm)	0.240 (H) × 0.240 (V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	normally white
Number of Color	260 K
Optimum Viewing Angle(Contrast ratio)	6 o'clock
Brightness (cd/m^2)	300
Module Size (mm)	280.0 (W) × 210.0 (H) × 12.0 (D)
Module Mass (g)	720
Backlight Unit	CCFL, 2-tubes, edge-light, replaceable
Surface Treatment	Antiglare and hard-coating 3H

Sign "( )"represents preliminary value. Characteristic value without any note is typical value.
The LCD product described in this specification is designed and manufactured for the standard use in OA equipment and consumer products, such as computers, communication equipment, industrial robots, AV equipment and so on.
Do not use the LCD product for the equipment that require the extreme high level of reliability, such as aerospace applications, submarine cables, nuclear power control systems and medical or other equipment for life support.
OPTREX assumes no responsibility for any damage resulting from the use of the LCD product in disregard of the conditions and handling precautions in this specification.
If customers intend to use the LCD product for the above items or other no standard items, please contact our sales persons in advance.

2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX	UNIT
Power Supply Voltage for LCD	VCC	0	6.0	V
Lamp Voltage	VL	0	2000	Vrms
Lamp Current	IL	0	18	mArms
Lamp Frequency	FL	---	80	kHz
Operation Temperature Note 1,2)	T_{op}	0	60	°C
Storage Temperature Note 2)	T_{stg}	-20	70	°C

[Note]

1) Display panel surface

2) Top,Tstg ≤ 40°C : 90%RH max. without condensation

Top,Tstg > 40°C : Absolute humidity shall be less than the value of 90%RH at 40°C without condensation.

3. ELECTRICAL CHARACTERISTICS

(1) TFT-LCD

Ambient temperature: Ta = 25°C

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remarks
Power Supply Voltages for LCD *)	VCC	3.0	3.3	3.6	V	Note A) (See: Page 5)
Power Supply Currents for LCD	ICC	--	470	770	mA	Note B) (See: Page 6)
Permissive input ripple Voltage	VRP	--	--	100	mVp-p	VCC=+3.3V

*) at the Input connector

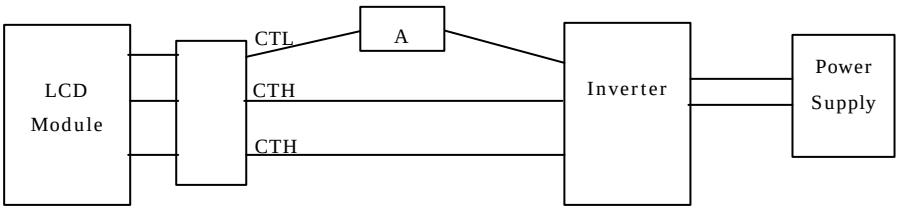
(2) Backlight

Ta = 25°C

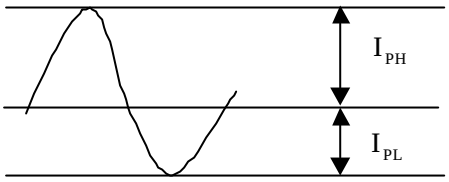
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remarks
Lamp Voltage	VL	--	540	--	Vrms	IL = 12.0 mArms
Lamp Current	IL	6.0	12.0	13.0	mArms	Note 1),5)
Lamp Frequency	FL	30	--	60	kHz	Note 2)
Starting Lamp Voltage	VS	1000	--	--	Vrms	Ta = 25°C Note 3)
		1200	--	--		Ta = 0°C Note 3)
Lamp Life Time	LT	50,000	--	--	h	IL = 12.0 mArms, Continuous operation Note 3),4)

[Note]

1) Lamp Current measurement method (The current meter is inserted in low voltage line.)



2) Lamp frequency of inverter may produce interference with horizontal synchronous frequency, and this may cause horizontal beat on the display. Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.
3) Lamp life time is defined as the time either when the brightness becomes 50% of the initial value, or when the starting lamp voltage does not meet the value specified in this table.
4) The life time of the backlight depends on the ambient temperature. The life time will decrease under low/high temperature.
5) Please use the inverter which has symmetrical current wave form as follows,
   The degree of unbalance: less than 10%
   The ratio of wave height: less than $\sqrt{2} \pm 10\%$



I_{PH}: High side peak

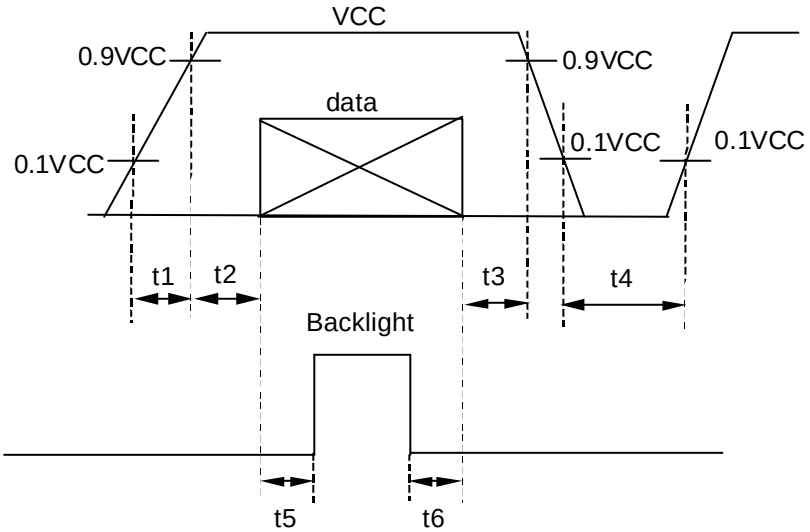
I_{PL}: Low side peak

The degree of unbalance = $| I_{PH} - I_{PL} |$ / Irms × 100(%)
The ratio of wave height = I_{PH}(or I_{PL}) / Irms

CURRENT WAVE FORM

A) Power and signals sequence:

t1 ≤ 10 ms	400ms ≤ t4
0 < t2 ≤ 50 ms	200 ms ≤ t5
0 < t3 ≤ 50 ms	0 ≤ t6



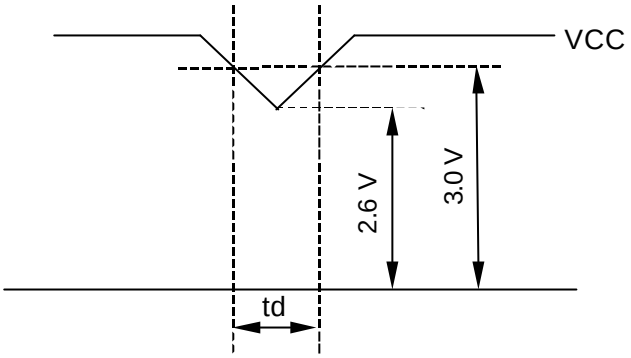
data: RGB DATA, DCLK, HD, VD, DENA

VCC-dip conditions:

1) When 2.6 V ≤ VCC < 3.0 V, td ≤ 10 ms

2) When VCC < 2.6 V

VCC-dip conditions should also follow the power and signals sequence.



B) Typical current condition:

64-gray-bar pattern

768 line mode

VCC = +3.3 V, , f_H = 48.4 kHz, f_V = 60 Hz, f_{CLK} = 65 MHz

4. INTERFACE PIN CONNECTION

CN 1(INTERFACE SIGNAL)

Used connector: FI-SE20P-HF(JAE)

Corresponding connector: FI-S20S[for discrete wire] , FI-SE20M[for SMT]

Pin No.	Symbol	Function
1	VCC	+3.3V Power supply
2	VCC	+3.3V Power supply
3	GND	
4	GND	
5	Link 0-	R0, R1, R2, R3, R4, R5, G0 *)
6	Link 0+	R0, R1, R2, R3, R4, R5, G0 *)
7	GND	
8	Link 1-	G1, G2, G3, G4, G5, B0, B1 *)
9	Link 1+	G1, G2, G3, G4, G5, B0, B1 *)
10	GND	
11	Link 2-	B2, B3, B4, B5, HD, VD, DENA *)
12	Link 2+	B2, B3, B4, B5, HD, VD, DENA *)
13	GND	
14	CLKIN-	Clock-
15	CLKIN+	Clock+
16	GND	
17	N.C.	This pin should be open.
18	TEST	This pin should be open. Test signal output for only internal test use.
19	TEST	This pin should be open. Test signal output for only internal test use.
20	SC	High:Reverse Scan , Low:Normal Scan

*) See; Timing Chart(P9) and LVDS Data Mapping(P10)

CN 2(BACKLIGHT)

Backlight-side connector: BHR-04VS-1 (JST)

Inverter-side connector: SM04(4.0)B-BHS-1(JST)

Pin No.	Symbol	Function
1, 2	CTH	VBLH (High voltage)
4	CTL	VBLL (Low voltage)

VBLH - VBLL = VL

5. INTERFACE TIMING

(1) Timing Specifications

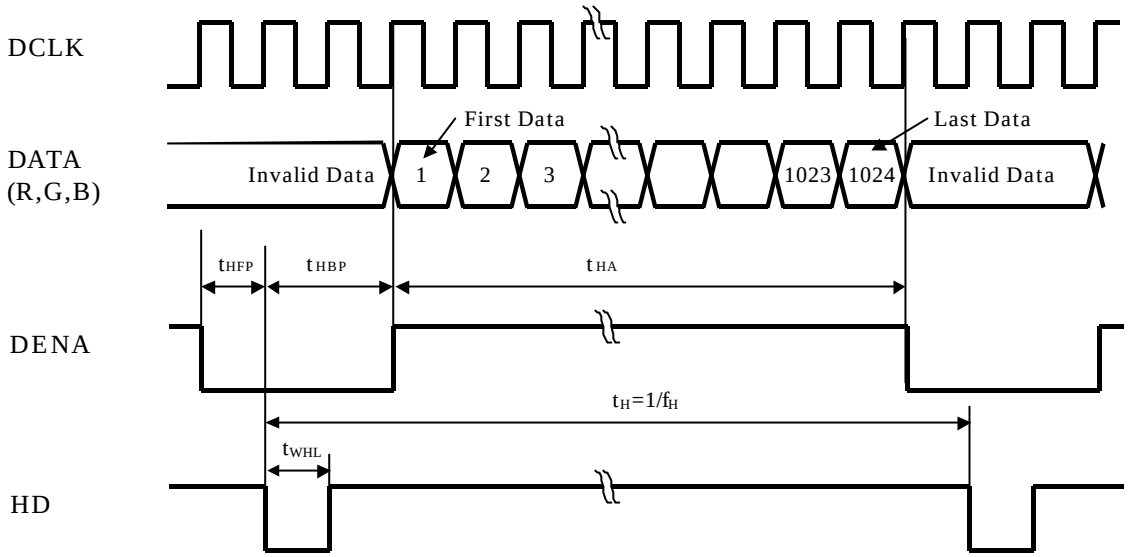
ITEM			SYMBOL	MIN.	TYP.	MAX.	UNIT
LCD Timing LVDS Transmitter Input	DCLK	Frequency	f_{CLK}	43.6	65	66.6	MHz
		Period	t_{CLK}	15	15.4	22.9	ns
	DENA	Horizontal Active Time	t_{HA}	1024	1024	1024	t_{CLK}
		Horizontal Front Porch	t_{HFP}	0	24	--	t_{CLK}
		Horizontal Back Porch	t_{HBP}	4	296	--	t_{CLK}
		Vertical Active Time	t_{VA}	768	768	768	t_H
		Vertical Front Porch	t_{VFP}	2	3	--	t_H
		Vertical Back Porch	t_{VBP}	1	35	--	t_H
	HD	Frequency	f_H	42.4	48.4	60	kHz
		Period	t_H	16.6	20.7	23.6	μs
		Low Width	t_{WHL}	1	136	--	t_{CLK}
	VD	Frequency	f_V	55	60	75	Hz
		Period	t_V	13.3	16.7	18.2	ms
		Low Width	t_{WVL}	1	6	--	t_H

[Note]

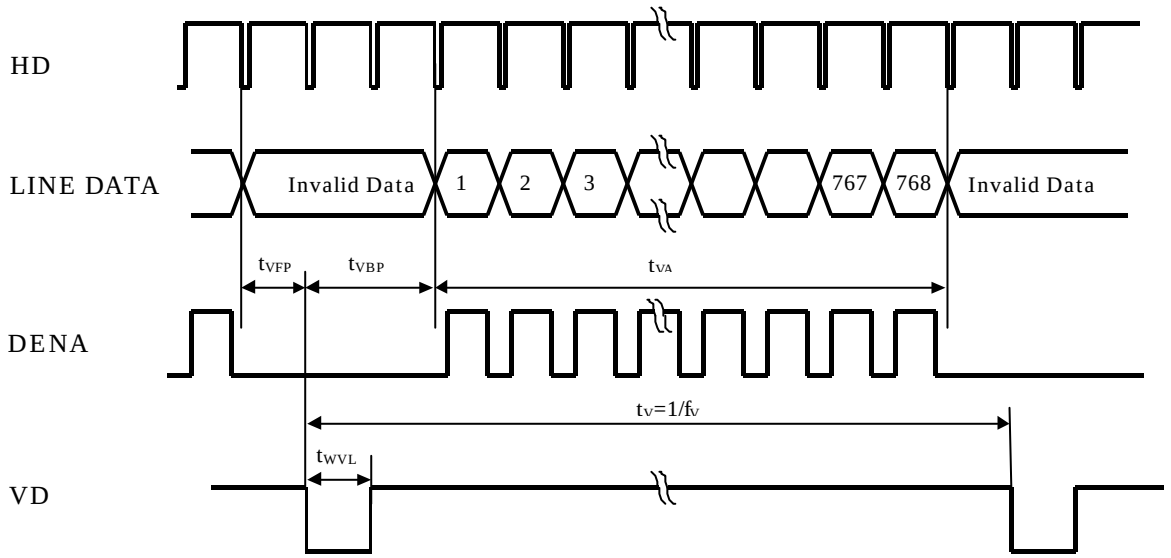
1) Polarities of HD and VD are negative in this specification.
2) DENA (Data Enable) shall always be positive polarity as shown in the timing specification.
3) DCLK shall appear during all invalid period, and HD shall appear during invalid period of frame cycle.
4) LVDS timing follows the timing specifications of LVDS receiver IC: THC63LVDF84A(Thine).

(2) Timing Chart

a. Horizontal Timing Chart



b. Vertical Timing Chart



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