

摘 要

本篇论文主要讲述了一款 JTAG 接口电路的设计。在日新月异的科技发展中，台积电（TSMC）公司发明空间折叠工艺，使得摩尔定义继续延续，让工艺进入 5nm 时代，随着电路的规模越来越大，电路的工艺越来越小，测试的难度呈几何倍数提升，成本越来越高和覆盖率的问题一直困扰着测试人员，普通物理测试因为工艺原因已经不能被作为主要的测试手段，在这种环境下 JTAG（Jiont Test Action Group）联合测试小组被提出，作为一种可以在设计 FPGA 里的可编程模块，可以配置和测试芯片，在不影响芯片正常逻辑运行的情况下，让电路的测试人员可以观测，甚至修改电路，而且覆盖率极高。本款 JTAG 接口电路设计兼容 IEEE1149.1 协议，指令长度为 10bit，数据长度为 32bit。在 JTAG 模块甚至 FPGA 领域国内外总体还是有一定差距，所以研究 JTAG 电路模块具有重大意义。

关键字: FPGA； JTAG 电路； 电路观测； IEEE1149.1 协议；

Abstract

This paper mainly describes the design of a JTAG interface circuit. In the ever-changing technological development, TSMC invented the space folding process, which made Moore's definition continue and let the process enter the 5nm era. As the scale of the circuit becomes larger and larger, the process of the circuit becomes smaller and smaller. The geometric multiple has increased, the cost is getting higher and higher, and the problems of coverage have been plaguing testers. Ordinary physical testing can no longer be used as the main test method due to process reasons. Under this environment, JTAG (Joint Test Action Group) joint testing The group was proposed as a programmable module that can be designed in FPGA, which can configure and test the chip, so that circuit testers can observe and even modify the circuit without affecting the normal logic operation of the chip, and the coverage is extremely high. This JTAG interface circuit design is compatible with IEEE1149.1 protocol, the command length is 10bit, and the data length is 32bit. There is still a certain gap in the field of JTAG modules and even FPGAs at home and abroad, so it is of great significance to study JTAG circuit modules.

Keywords: FPGA; JTAG circuit; circuit observation; IEEE1149.1 ;

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