Intel Agilex® 7 FPGA F-Series Development Kit User Guide

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1. Overview

Intel Agilex® 7 FPGA F-Series Development Kit is a complete design environment that includes both hardware and software you need to develop Intel Agilex 7 FPGA designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Intel Agilex 7 FPGA F-Series designs.

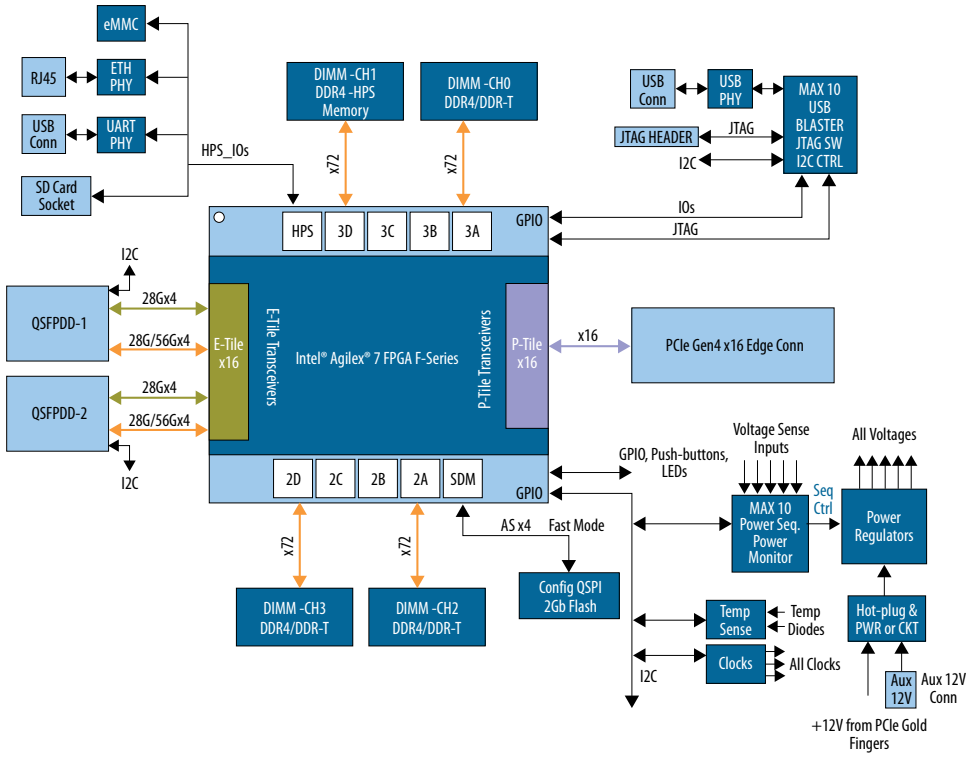
Table 1. Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Intel Agilex 7 FPGA F-Series Development Kit (ES -3V)	DK-DEV-AGF014E3ES	AGFB014R24A2E3VR0	Under 20000
Intel Agilex 7 FPGA F-Series Development Kit (ES -2V)	DK-DEV-AGF014E2ES	AGFB014R24A2E2VR0	Above 20000
Intel Agilex 7 FPGA F-Series Development Kit (Production 1 P-Tile & E-Tile) Power Solution 1	DK-DEV-AGF014EA	AGFB014R24B2E2V	Above 20220
Intel Agilex 7 FPGA F-Series Development Kit (Production 2 P-Tile & E-Tile) Power Solution 2	DK-DEV-AGF014EB	AGFB014R24B2E2V	Above 20500

Note: The -3V and -2V versions of the Intel Agilex 7 FPGA F-Series Development Kit use different power solutions for VCC core. Refer to the power tree diagrams in Power on page 40 for additional information.

1.1. Block Diagram

Figure 1. Intel Agilex 7 FPGA F-Series Development Kit Block Diagram



Feature Summary

- Intel Agilex 7 FPGA F-Series, 1400 KLE, 2486- (R24A and R24B) packages
- 2x Standard QSFPDD supports both optical and electrical cable interfaces connected to E-Tile transceivers
- PCIe x16 Gen 4 golden finger connected to P-Tile transceivers, supports x1/x4/x8/x16 modes
- 3x 288-Pin DDR4 DIMMs sockets to support 72 bits DDR4/DDR-T module in FPGA Fabric interface
- 1x 288-Pin DDR4 DIMM socket to support 72 bits DDR4 module for HPS memory interface
- 2 Gb QSPI Flash for active serial FPGA configuration (ASx4 mode)
- Programmable clock resource for XCVR, memory and FPGA fabric
- HPS interface supporting: ETH, UART, SD card socket, eMMC and Mictor connector

Note: Golden Software Reference Design for HPS (GSRD) is not currently available for this development kit.

1.2. Box Contents

Intel Agilex 7 FPGA F-Series development board, DDR4 DIMM module, USB2.0 Micro cable, Ethernet cable, 240W power adapter and NA/EU/JP/UK cords, ATX power convert cable - 24 pin to 6 pin.

Note: Only one DIMM module is provided with each development kit.

1.3. Operating Conditions

Table 2. Recommended Operating Conditions

Operating Condition	Range
Ambient operating temperature range	0°C to 45°C
ICC load current	100 A
ICC load transient percentage	200 A/µs
FPGA maximum power supported by active heatsink/fan	150 W

Handling Precautions

When handling the board, it is important to observe static discharge precautions.

Note: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Note: This development kit should not be operated in a vibration environment.

2. Getting Started

2.1. Software and Driver Installation

Intel® Quartus® Prime design software is a multi-platform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs. Intel Quartus Prime Pro Edition software is optimized to support the advanced features in next-generation FPGAs and SoCs with the Intel Agilex 7, Intel Stratix® 10, Intel Arria® 10, and Intel Cyclone® 10 GX device families.

Intel Agilex 7 FPGA F-Series Development Kit includes on-board Intel FPGA Download Cable circuits for FPGA and system Intel MAX® 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer. Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.

The Intel SoC EDS is a comprehensive software tool suite for embedded software development on Intel SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

Note: Use Intel Quartus Prime 19.4 Pro Edition or later for this development kit test and debug.

For more information and steps to install the Intel SoC EDS Tool Suite, refer to the links below.

Related Information

- Quick-Start for Intel Quartus Prime Pro Edition Software
- Intel Quartus Prime Pro Edition User Guide: Getting Started
- Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide
- Intel Agilex 7 FPGAs and SoCs Device Overview
- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series

2.2. Design Examples

Unzip the install package which includes board design files, documents, and examples directories. The following table lists the file directory names and a description of their contents.

Table 3. Installed Development Kit Directory Structure

Directory Name	Description of Directory Contents
board_design_files	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
documents	Contains the development kit documentation – quick start guides and user guide
examples	Contains: • Board Test System: BTS GUI, Power GUI and Clock GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, GPIO and PCIe Gen4
power_max10	Contains the instructions on how to program the power monitoring function in the Intel MAX 10 board controller (refer to Control on-board power regulator through Power Monitor GUI on page 28).
ubii_max10	Contains the instructions on how to program UBII Intel MAX 10

3. Powering Up the Development Kit

The instructions in this chapter explain how to setup the Intel Agilex 7 FPGA F-Series Development Kit for specific use cases.

3.1. Default Settings

The Intel Agilex 7 FPGA F-Series Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch settings table given below to return the board to its factory settings before proceeding forward.

Note: X refers to Don't Care in the table below.

Table 4. Factory Default Switch Settings

Switch	Default Position	Function
SW1 [1:3]	OFF/ON/ON	Configuration mode setting bits By default, AS -> FAST mode
SW2 [1:4]	OFF/OFF/OFF/OFF	Select the resource of the System Intel MAX 10 JTAG from USB PHY Enable Si5341's outputs Power up Si52202 Enable UART interface
SW3 [1:4]	OFF/OFF/OFF/OFF	Enable all the I^2C level shifter.
SW4 [1:4]	OFF/ON/ON/OFF	Select on-board Intel FPGA Download Cable as JTAG master when external JTAG header is absent Bypass PWR Intel MAX 10 in JTAG chain; Bypass FPGA HPS in JTAG chain Enable FPGA in JTAG chain
SW5	SW5.5 to SW5.6	Power off the board
SW6 [1:4]	ON/OFF/OFF/OFF	PCIe x16 mode is selected
SW7.1	ON	Select local clock as PCIe reference clock

3.2. Power Up

Board runs as a standalone work bench

Use the provided 240 W power adapter to supply power through **J16**. After power adapter is plugged into **J16** and **SW5** is set to the ON position, one blue LED (**D8**) illuminates, indicating that the board powered up successfully.