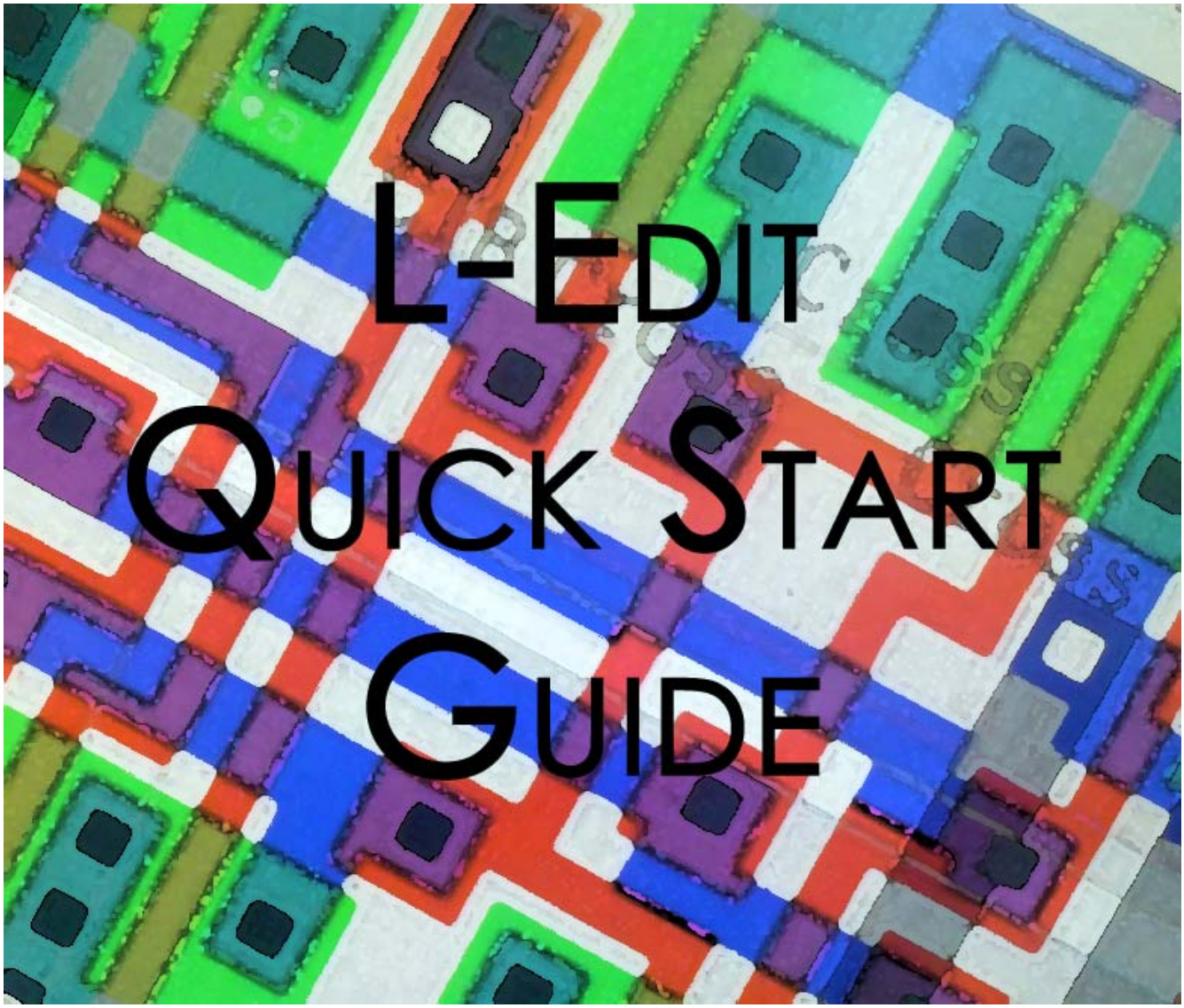

Nathan Kupp
Princeton University
PRISM REU Program 2006

1. Introduction

This guide is intended to supply the L-Edit user with a tutorial and reference for quickly gaining proficiency with the L-Edit software layout tool. By reading this guide and doing the provided tutorials in L-Edit, the user should be able to become relatively familiar with the program within a few hours time. This guide does not provide an exhaustive reference to all the features of L-Edit, as a complete documentation of these features is provided in the L-Edit User's Guide. The L-Edit User's Guide is provided in Adobe PDF form, accessible from the Help menu within the L-Edit program.

2. User Interface

The user interface provided by L-Edit is similar to that of many other CAD and layout design software packages. There are three important sections of the L-Edit User Interface:

- Toolbars
- Sidebar
- Drawing Area

The collection of toolbars on the top of the screen allows the user to select what type of objects to draw, as well as manipulate previously created objects. Figure 1 displays the toolbar and sidebar with the most frequently used buttons labeled. Most of the buttons here are self-explanatory.

L-Edit also has a sidebar which contains the layers specified under "Setup → Layers...". A default collection of most commonly used layers is provided by the **`Generic_025um.tdb`** file, provided in the root L-Edit directory. Since this file provides all of the common layers such as N-well, Active, N-select, P-select, Metal1, etc. it will not likely be necessary to modify the default layers for this tutorial.

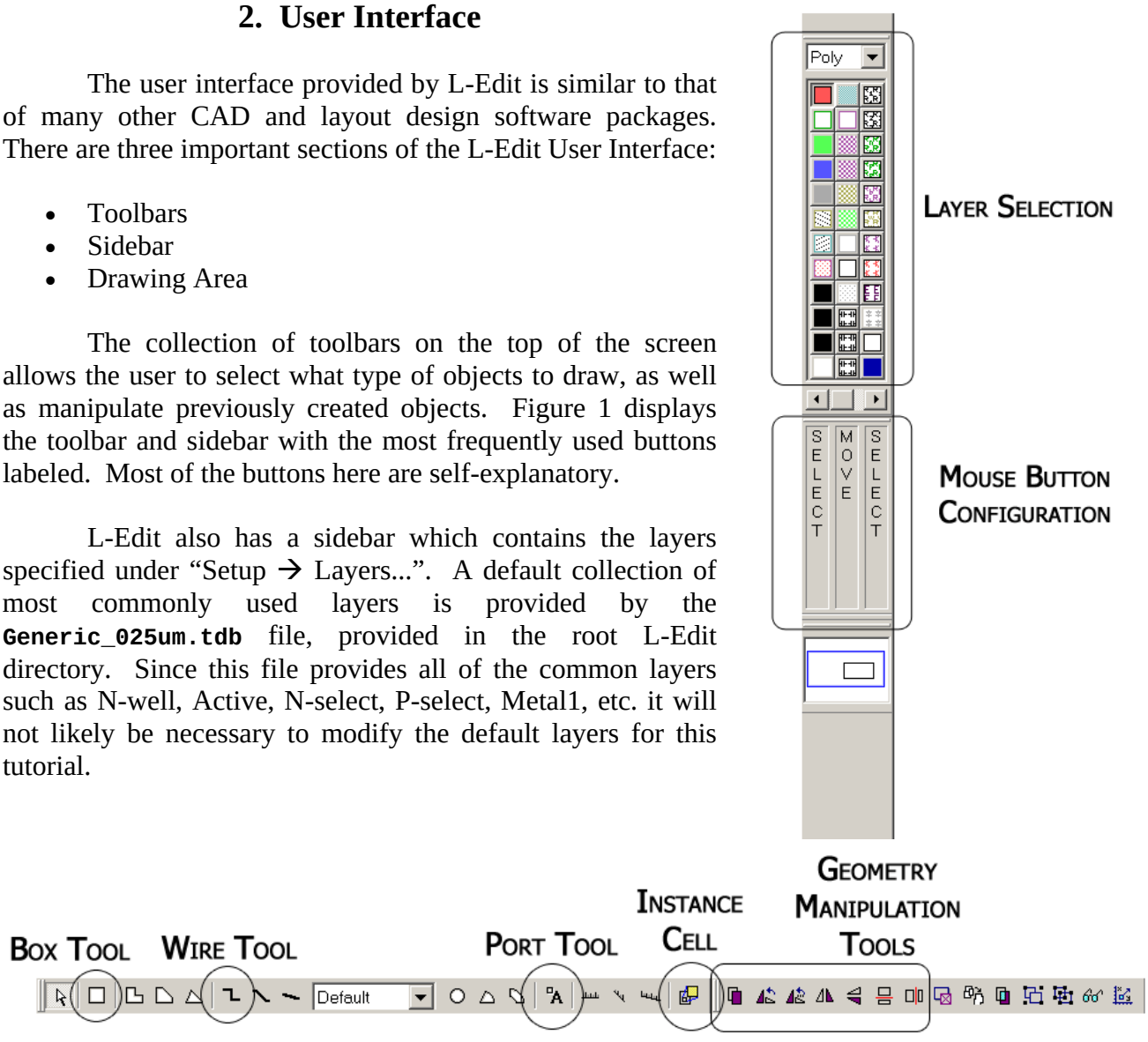

Figure 1. L-Edit Toolbar/ Sidebar

For custom layers, a blank setup can be used without any default layers, as described in Tutorial #1: NMOS Design & Layout. Layers can be selected on the sidebar with either their representative icon or from the list above the icons. Note that the names of layers are functionally irrelevant, and serve only to clarify the design – in reality, all layers are simply translated to geometry and the layer names discarded when the file is exported to GDSII.

With the creation of a new file, the user is presented with a layout area entitled Cell0, representing the first "cell" within his or her design (Cells will be explained in further detail in section 4). Figure 2 shows the layout area of this Cell0. The layout area is where all of the design takes place – the user selects appropriate geometry from the toolbar, such as a rectangle; a layer, from the sidebar, and draws it on the layout area. As the object is drawn, the status bar at the bottom left of the screen will display the drawn width and height, and area of the object. The drawn object can subsequently be resized by left-clicking on the object to select it, and then clicking down with the mouse scroll wheel on the corner of the object and dragging it. The status bar will update to reflect the change in size. The object can be repositioned by clicking near its center with the mouse scroll wheel and dragging it with the mouse. Finer movement can be achieved with the Draw → Nudge dialog, which allows movement in any direction with three decimal places.

Use the arrow keys to display different parts of the design in the viewing window. Also, the view can be zoomed in/out by clicking anywhere outside the drawing with the left mouse button, and then rotating the scroll wheel on the mouse while holding Ctrl on the keyboard. The display of the grid can be toggled within this viewing window by selecting Setup → Design and selecting the Grid tab. Note that under the Technology tab there are settings for the units used in the design. The settings under Grid control the distance between grid points as well as whether the mouse snaps to this grid. If the Suppress major/minor grid is set too large in this dialog, the grid will likely not appear unless the view is zoomed fully in (again to scroll, use the middle mouse button). Finally, note that the origin (x,y = 0) appears as a cross symbol on the drawing area (see figure below).

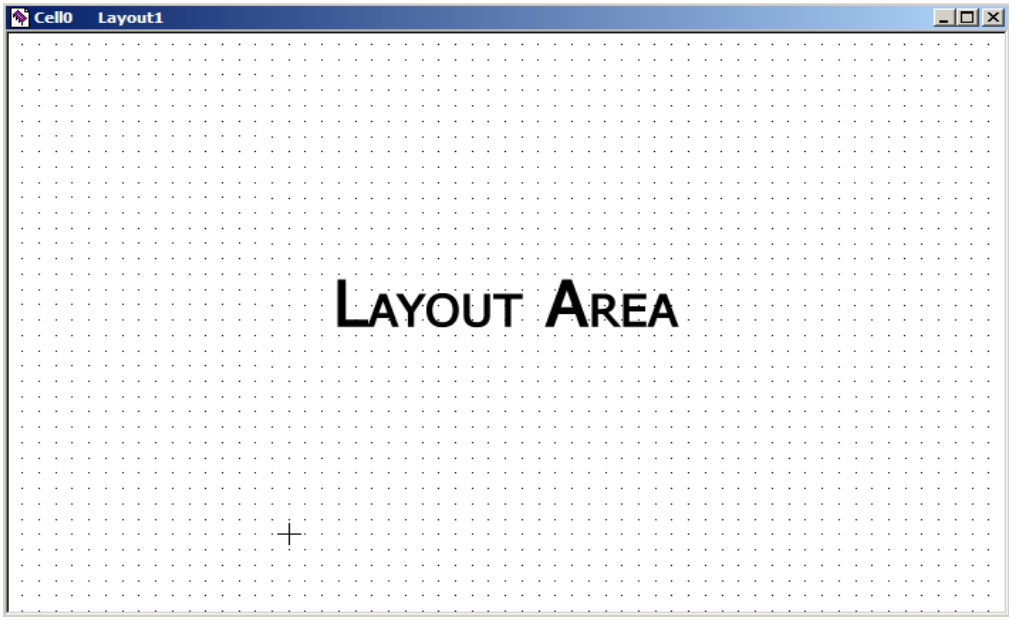

Figure 2. Cell0 Window

What's Important:

- ***Toolbar: Select, Rectangle, Wire, Port, Instance, and Rotate/Mirror icons***
- ***Layers icons in Sidebar***
- ***Layout Area***

3. Tutorial #1: NMOS Design & Layout

In the first tutorial, the design of an n-type MOSFET on a p-type substrate is presented. An NMOS transistor consists of an n-type source and drain regions, a gate terminal, and a substrate terminal. Remember, a MOSFET is a four terminal device, requiring not only connections to the Source, Drain, and Gate, but the Substrate as well.

Process:

1. Select File → New to create a new layout. A dialog will appear asking for a layout name as well as a location to copy a TDB setup from. The file you choose for the TDB setup governs the layer setup in the new design – therefore, if you wish to create a design with entirely customized layers, you can select **<empty>** and a layout will appear with an empty Layers toolbar. Copy the TDB setup from the file C:\Tanner\LEdit102\Samples\tech\Generic0_25um\Generic_025.tdb. Since the transistor is NMOS, the source and drain are n-doped and thus must be formed directly on a p-type material (in this case, the substrate).

2. Draw two Active regions in the design. The Active layer denotes an opening in the field oxide through which n-type and p-type depositions can be made – we need an area for the source and drain of the transistor, as well as a connection for the substrate.

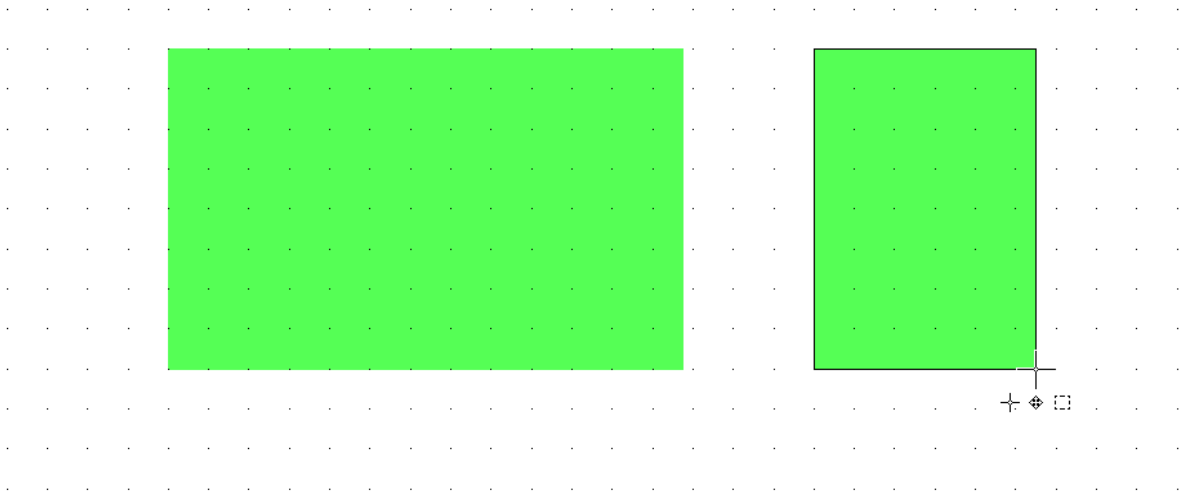

Figure 3. Active Area Layer

Suggestion: *The purpose of this tutorial is to teach you how to use L-Edit. To save time, you do not need to understand the names and functions of different layers. Just draw objects the way you see them in this tutorial.*

3. Draw N-select/P-select regions over the source/drain and substrate Active areas, respectively. The substrate can never be directly connected to metal layers, so we need to create doped select layers where we want to make connections. These layers denote areas that will be implanted with n/p-type material. Note that the N-select can be drawn right across the polysilicon gate, as this gate will prevent n-type deposition directly beneath the gate when the chip is bombarded with n-type atoms.

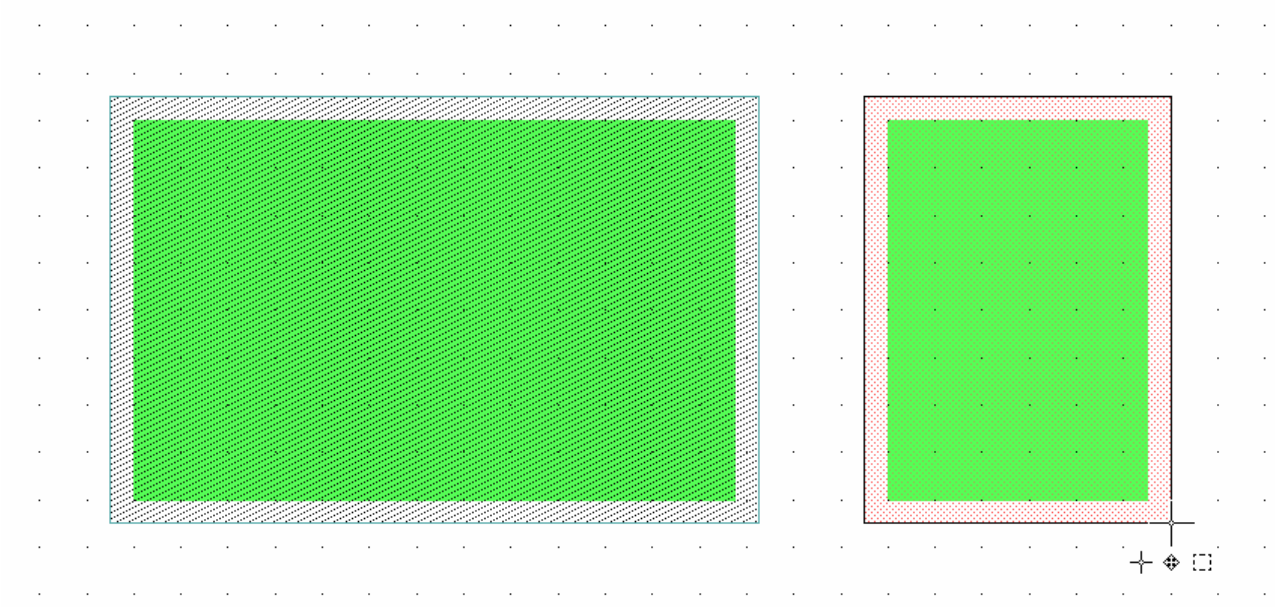

Figure 4. N-Select and P-Select Layers

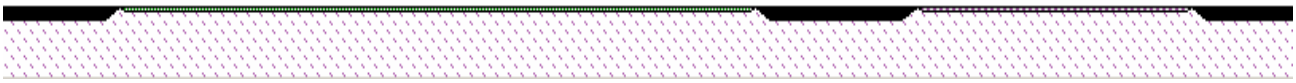

Figure 5. N-Select and P-Select Cross-Sectional View

4. Draw Poly layer. The gate of a MOSFET is typically created out of polysilicon, represented by the Poly layer. To create a gate for our NMOS transistor, we need to draw a Poly layer rectangle over the active region of the source/drain. Note that in the cross-sectional view, the large polysilicon pad is not shown, because the cross-section was taken across the transistor itself. The Poly gate shown below can be generated by drawing two separate, overlapping rectangles. These rectangles can then be merged into a single object by selecting Draw → Merge.

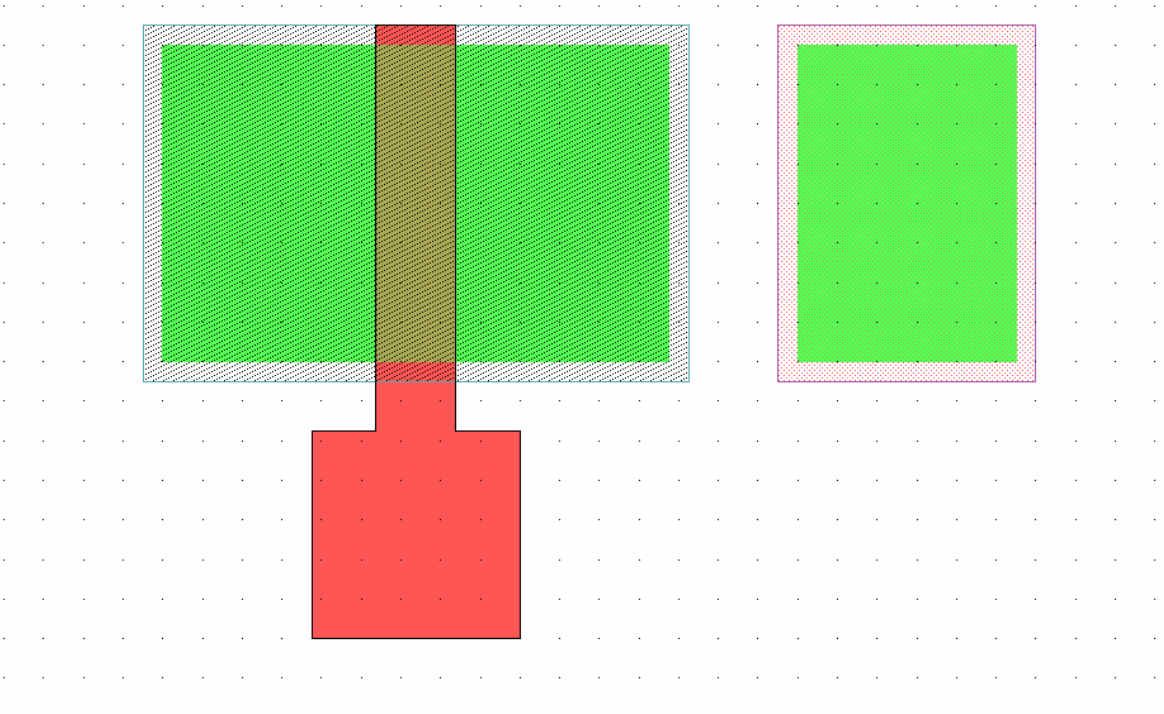

Figure 6. Poly Layer

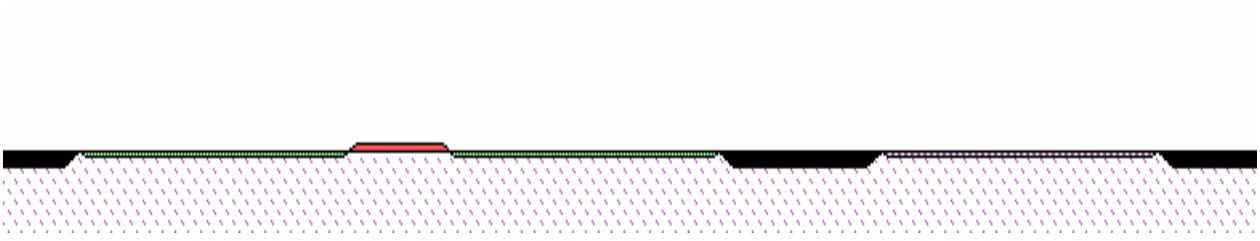

Figure 7. Poly Layer Cross-Sectional View

5. Draw Active contacts at the source drain and substrate, and a Poly contact on the gate. We now need to create an opening in the gate oxide to wire up our transistor. This is denoted by the Active Contact layer and the Poly Contact layer – the Active Contact layer makes connections to the Active layer, and the Poly Contact layer makes connections to the Poly layer. Again note that in the cross-sectional view, the Poly contact is not visible because the cross-section was taken across the transistor itself.

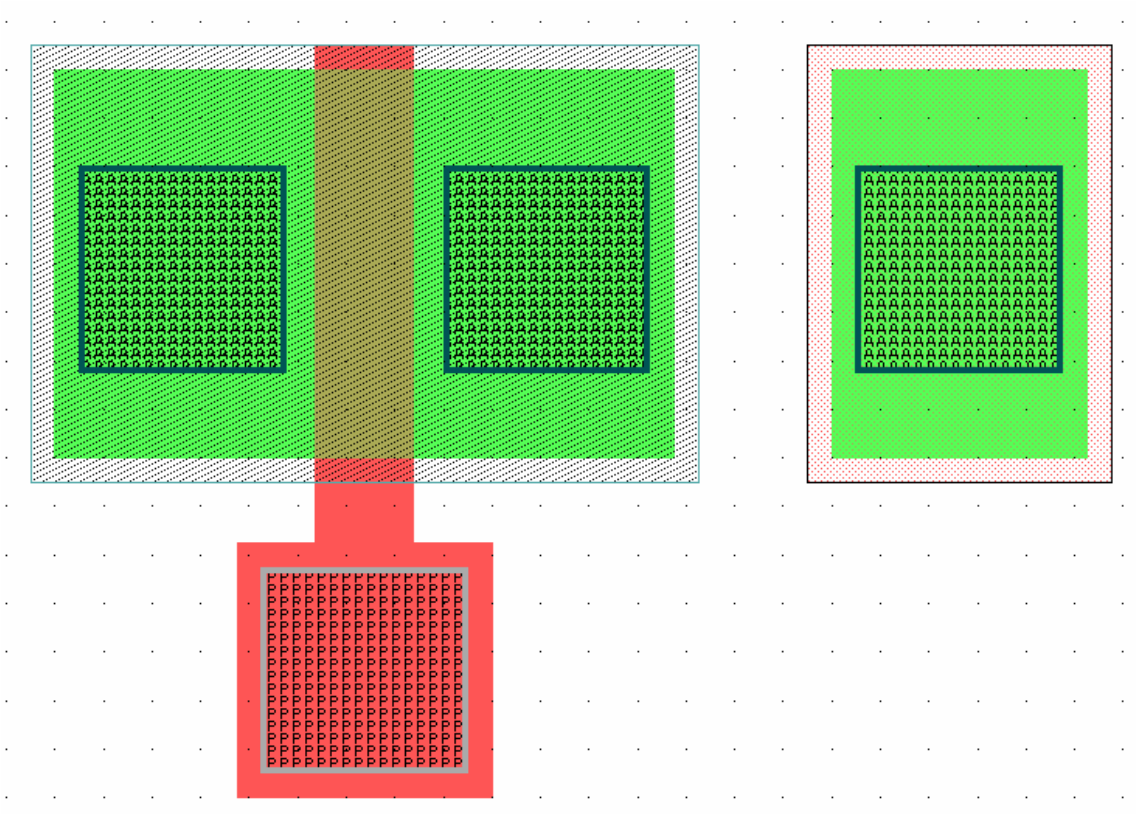

Figure 8. Active and Poly Contact Layers

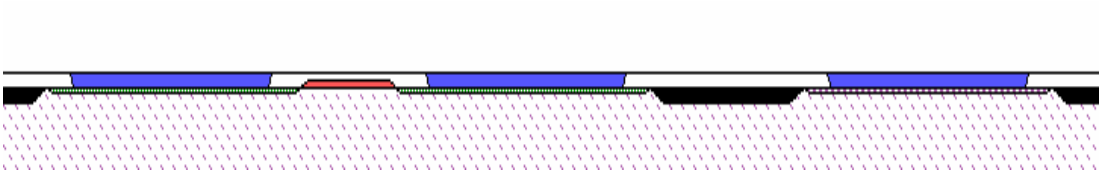

Figure 9. Active and Poly Contact Layers Cross-Sectional View

6. We now need wires for the transistor to be useful. Draw Metal1 layer connections to each of the four contact points. These can be created by either selecting the wire tool and drawing a wire, or using the rectangle tool to create a rectangular wire segment. Again, we cannot see the Metal1 wire on the gate in the cross-sectional view because of the location of the cross-section. Note that it is common to connect one terminal of the N-type MOSFET to the substrate and then to ground.

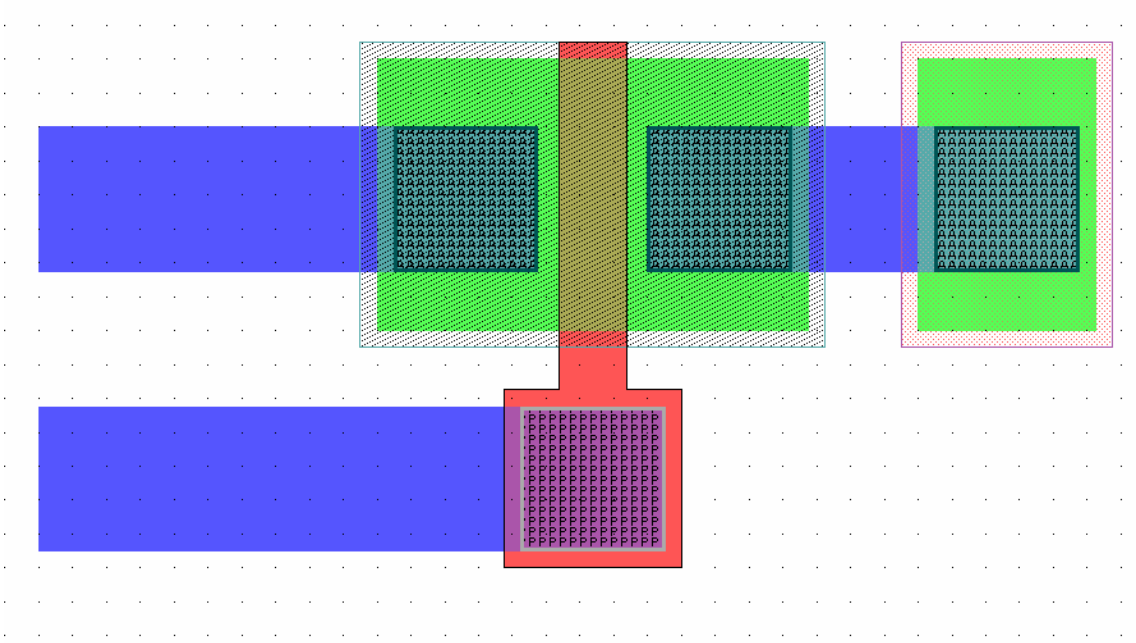

Figure 10. Metal1 Layer

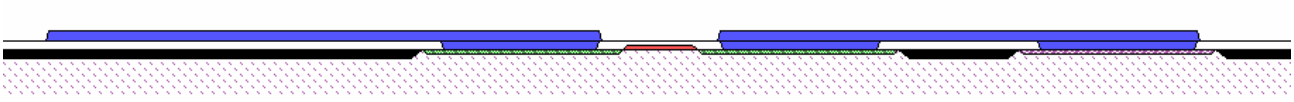

Figure 11. Metal1 Layer Cross-Sectional View

7. Now we have a working NMOS transistor! Do a Cell → Rename… to name this cell "**NMOS**" and a File → Save As... to save this file as tutorial.tdb. You can now create a PMOS device as well by simply forming it entirely within an n-well, with the substrate connection now being to an N-Select layer within the n-well. Remember, the substrate connection of a PMOS device is connected to VDD, not GND, producing a reverse biased pn-junction at the substrate connection. Similarly our NMOS device had a substrate connection to ground, also producing a reverse biased pn-junction between the substrate and the more positively charged transistor source and draing. A layout and cross sectional view of the PMOS transistor is shown below. Create a new cell (Cell → New...), and name it "**PMOS**". Draw this transistor, and then click File → Save.

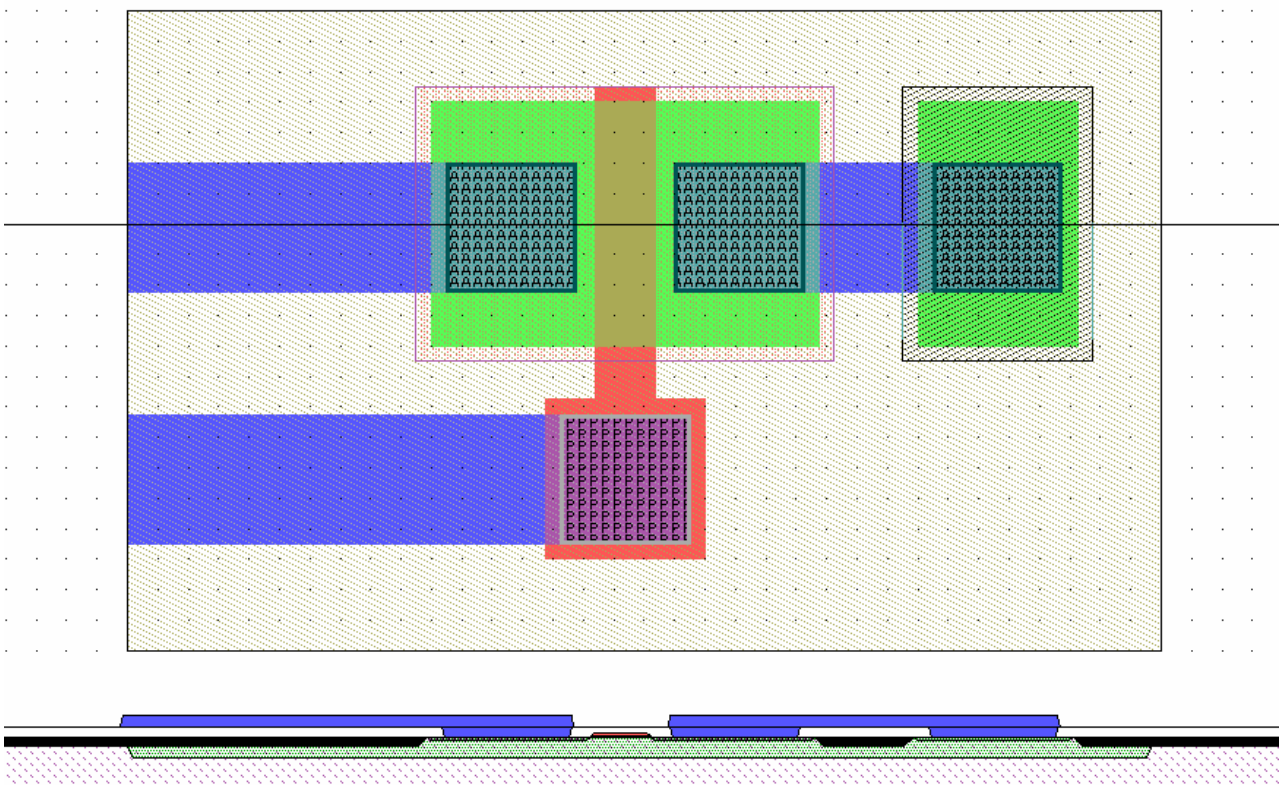

Figure 12. PMOS

Cross-Sectional View Note: *The cross sectional views used in this tutorial can be created using L-Edit's built in Cross-Sectional View Generator. This is accessed from* **Tools → Cross-Section...** *as shown below in Figure 13. Use the settings as shown in Figure 14, and select a vertical coordinate using* **Pick**. *Place the horizontal black line across the design, and then click* **OK**. *The cross-sectional view will be generated as shown in Figure 15. Note that these cross-sections represent an oversimplification of the fabrication process, and are merely intended to provide the user with an understanding of the interconnections between the layers drawn.*

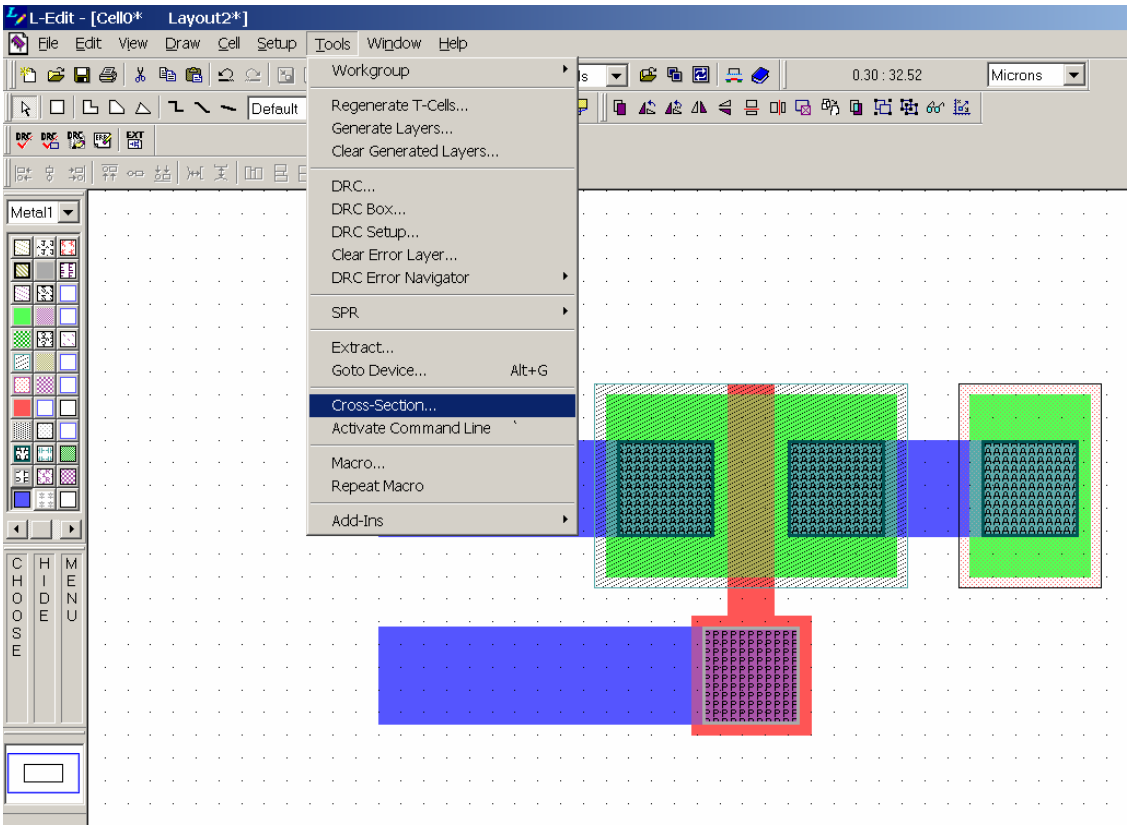

Figure 13. Cross-Sectional View Creation

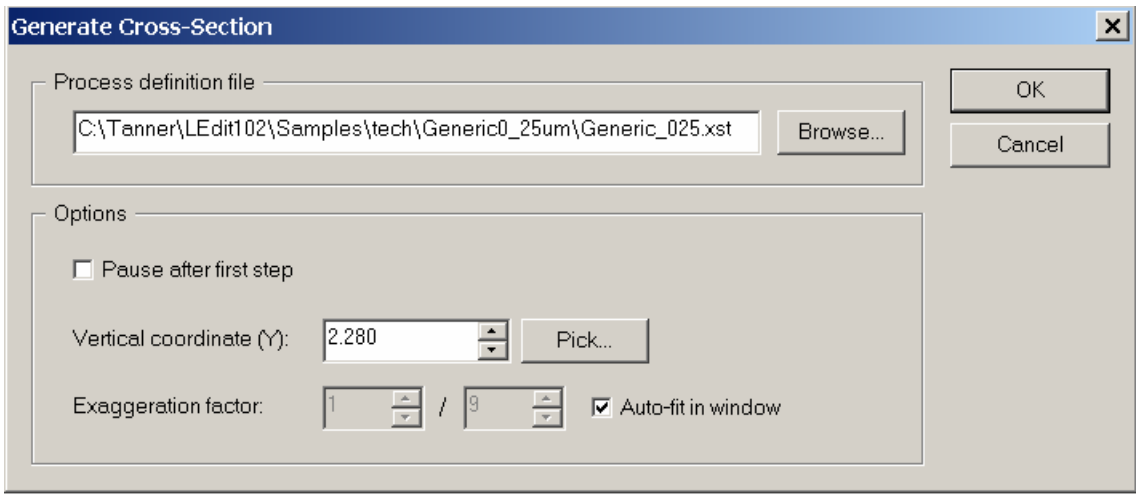

Figure 14. Generate Cross-Section Dialog

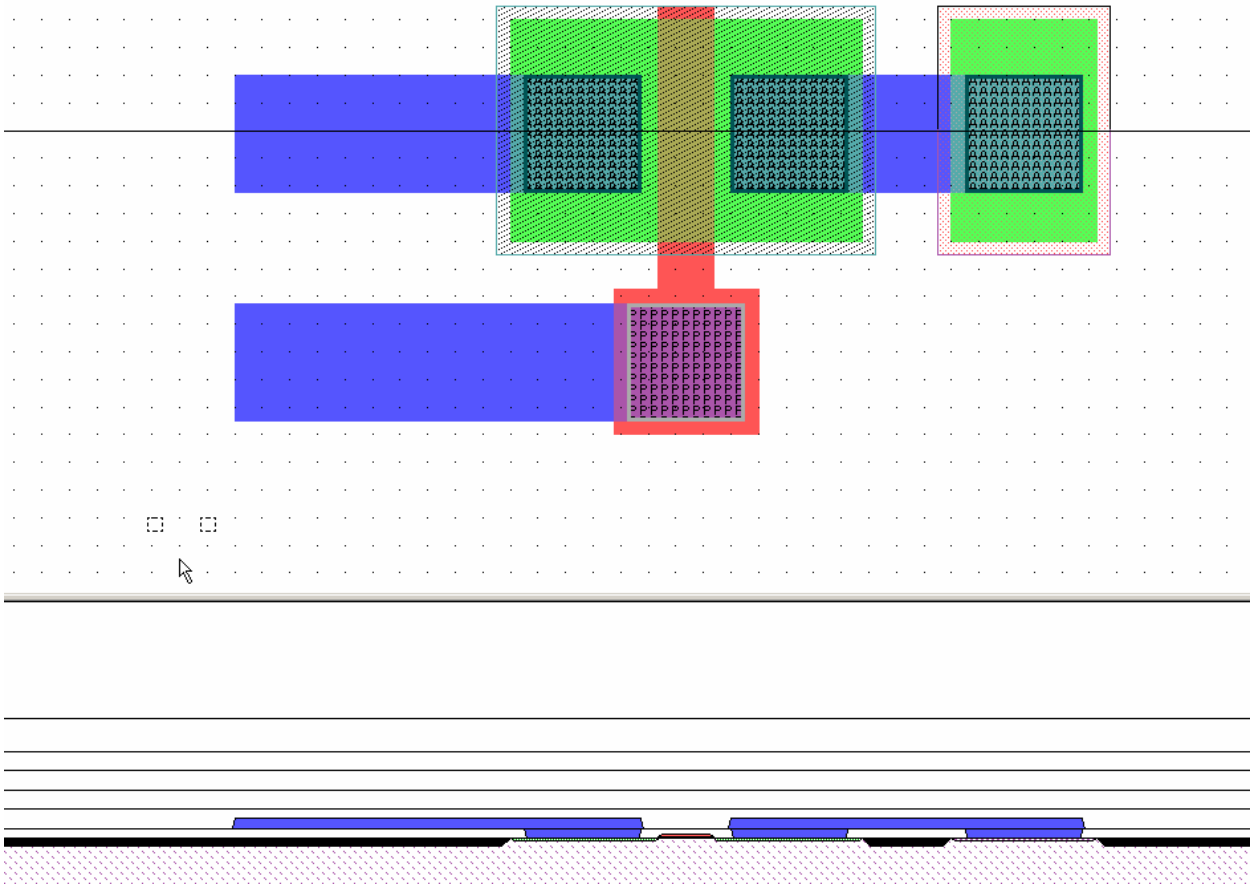

Figure 15. Cross-Sectional View

4. Cells

The design process in L-Edit is centered on cells, which are the fundamental building blocks at all levels of hierarchy – from a single MOSFET, to a logic gate, to an entire design. The figure below shows a cell hierarchy including MOSFETs as well as digital logic assembled on several levels to create a complete layout. The TDB files that L-Edit works with are essentially a collection of all cells related to a single design.

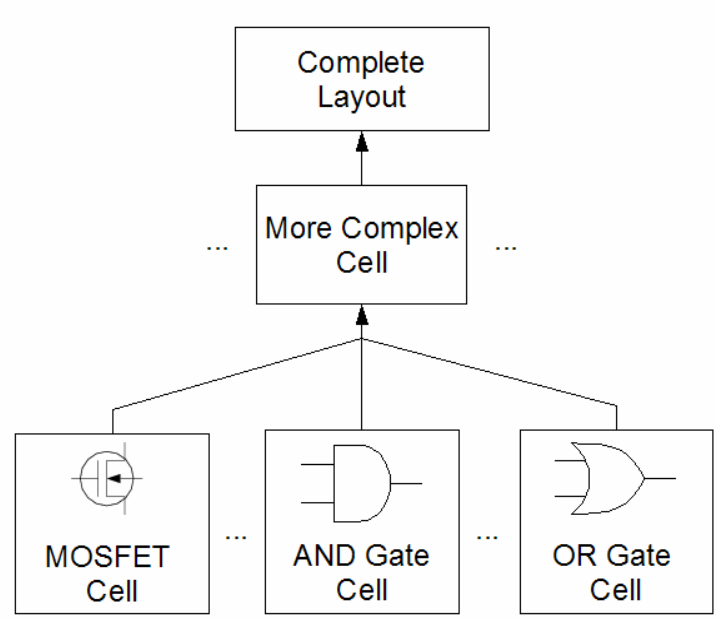

Figure 16. Cell Hierarchy

What's Important:

- ***Cell Menu: New, Open, Copy, Rename, Delete, Instance***

5. Tutorial #2: Cell Hierarchy Based Inverter Design

In the first tutorial we created a **tutorial.tdb** file containing the cells **NMOS** and **PMOS**. Because of the hierarchical design structure of L-Edit, we can now use these two cells together in a third cell to create an inverter, as shown in Figure 20.

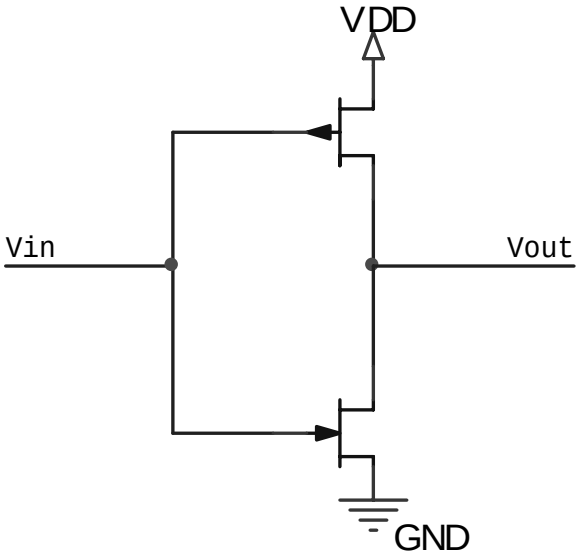

Figure 17. Inverter Schematic

When the input of this device is high, the lower (NMOS) transistor is on and the upper transistor is off – causing the output to be pulled low. When the input is low, the upper (PMOS) transistor is on and the lower transistor is off – causing the output to be pulled high. Although using the two NMOS and PMOS transistors we drew to create an inverter will work, we will see that using two separate components can be messy and that a better approach is to use two transistors connected directly together within a standard cell frame. Standard cell frames will be discussed in more detail in the section on Standard Place and Route. The layout process for an inverter using two transistors is as follows: