POSITIVE AND NEGATIVE OUTPUT DC-DC CONVERTER

FEATURES

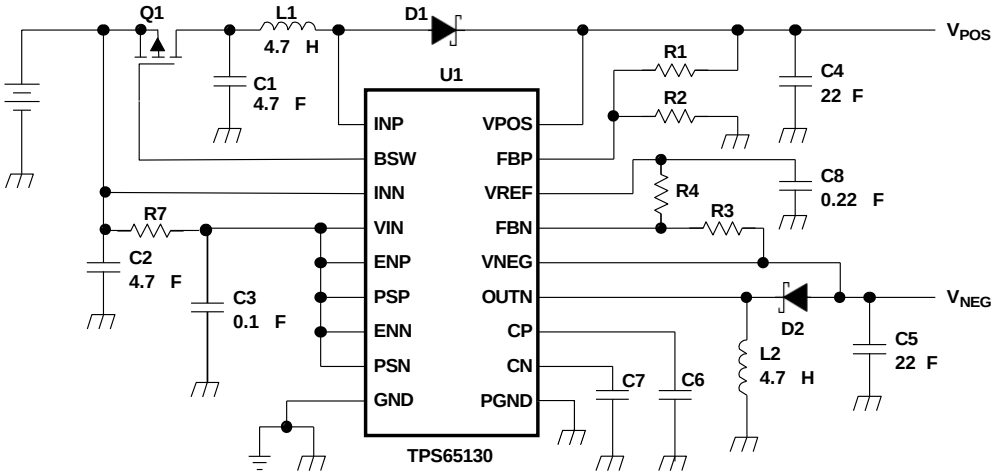
- **Dual Adjustable Output Voltages Up to +15 V and Down to –15 V**
- **800-mA Typical Switch Current Limit at Boost and Inverter Main Switches at TPS65130**
- **2-A Typical Switch Current Limit at Boost and Inverter Main Switches at TPS65131**
- **Up to 89% Efficiency at Positive Output Voltage Rail**
- **Up to 81% Efficiency at Negative Output Voltage Rail**
- **Power-Save Mode for High Efficiency at Low Load Currents**
- **Independent Enable Inputs for Power Up and Power Down Sequencing**
- **Control Output for External PFET to Support Completely Disconnecting the Battery**
- **2.7-V to 5.5-V Input Voltage Range**
- **Minimum 1.25-MHz Fixed Frequency PWM Operation**
- **Thermal Shutdown**
- **Overvoltage Protection on Both Outputs**
- **1-µA Shutdown Current**
- **Small 4 mm x 4 mm QFN-24 Package (RGE)**

APPLICATIONS

- **Small to Medium Size OLED Displays**
- **(TFT) LCD and CCD Bias Supply**
- **PDAs, Pocket PCs, Smartphones**
- **Digital Cameras**
- **Camcorders**

DESCRIPTION

The TPS65130/1 is dual-output dc-dc converter generating a positive output voltage up to 15 V and a negative output voltage down to -15 V with output currents in a 200-mA range in typical applications, depending on input voltage to output voltage ratio. With a total efficiency up to 85%, the device is ideal for portable battery-powered equipment. The input voltage range of 2.7 V to 5.5 V allows the TPS65130/1 to be directly powered from a Li-ion battery, from 3 cells NiMH/NiCd or alkaline batteries. The TPS65130/1 comes in a small 4 mm x 4 mm QFN-24 package. Together with a minimum switching frequency of 1.25 MHz it enables designing small power supply applications because it requires only a few small external components.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The converter operates with a fixed frequency PWM control topology and, if power-save mode is enabled, it uses a pulse-skipping mode at light load currents. It operates with only 500-µA device quiescent current. Independent enable pins allow power up and power down sequencing for both outputs. The device has an internal current limit overvoltage protection and a thermal shutdown for highest reliability under fault conditions.

ORDERING INFORMATION

T_A	SWITCH CURRENT LIMIT		PART NUMBER(1)
	BOOST CONVERTER	INVERTING CON-VERTER	
–40°C to 85°C	800 mA	800 mA	TPS65130RGE
–40°C to 85°C	1950 mA	1950 mA	TPS65131RGE

(1) The RGE package is availabletaped and reeled. Add an R suffix to the device type (i.e., TPS65130RGER) toorder quantities of 3000 devices per reel. It is also available in minireels. Add a T suffix to the device type (i.e., TPS65130RGET) toorder quantities of 250 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS65130/1
VIN, INN	Input voltage range at pins (2)	–0.3 V to +6.0 V
VPOS	Maximum voltage at pin (2)	17 V
VNEG	Minimum voltage at pin (2)	–17 V
	Voltage at pins ENN, ENP, FBP, FBN, CN, CP, PSP, PSN, BSW (2)	–0.3 V to V_{IN} + 0.3 V
INP	Input voltage at pin (2)	17 V
	Differential voltage between pins OUTN to V_{INN}(2)	24 V
T_J	Operating virtual junction temperature	–40°C to 150°C
T_{STG}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listedunder "absolute maximum ratings" may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the deviceat these or any other conditions beyond those indicated under "recommendedoperating conditions" is not implied. Exposure to absolute-maximum-ratedconditions for extended periods may affect device reliability.
(2) All voltage values are withrespect to network ground terminal, unless otherwisenoted.

DISSIPATION RATINGS TABLE(1)

PACKAGE	Θ_{JA}	Θ_{JB}	Θ_{JC}	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RGE	37.8 °C/W	27.8 °C/W	57.9 °C/W	2646 mW	26 mW/°C	1455 mW	1058 mW

(1) This thermal data is based on assembly of the device on a JEDEC high K board. The PowerPAD must be soldered on a pad on the board. There must be vias within the pad that contact the ground plane in the PCB. Exceeding the maximum junctiontemperature will force the device into thermalshutdown.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	2.7		5.5	V
T_A	Operating free-air temperature range	-40		85	°C
T_J	Operating virtual junction temperature range	-40		125	°C

ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range and over recommended input voltage range, typical at an ambient temperature of 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE (V_{POS}, V_{NEG})						
V_{POS}	Adjustable output voltage range		V_{IN}+ 0.5 V		15	V
V_{NEG}	Adjustable output voltage range		-15		-2	V
V_{REF}	Reference voltage	I_{REF} = 10 µA	1.2	1.213	1.225	V
I_{FBP}	Positive feedback input bias current	V_{FBP} = V_{REF}		50		nA
I_{FBN}	Negative feedback input bias current	V_{FBN} = 0.1 V_{REF}		50		nA
V_{FBP}	Positive feedback regulation voltage	V_{IN} = 2.7 V to 5.5 V	1.189	1.213	1.237	V
V_{FBN}	Negative feedback regulation voltage	V_{IN} = 2.7 V to 5.5 V	-0.024	0	0.024	V
	Total Output DC accuracy			+3%		
$R_{DS(ONN)}$	Inverter switch on-resistance	V_{IN} = 3.6 V		440	620	mΩ
		V_{IN} = 5.0 V		330	530	
I_{LIMN}	TPS65130 Inverter switch current limit	2.7 V < V_{IN} < 5.5 V	700	800	900	mA
I_{LIM}	TPS65131 Inverter switch current limit	V_{IN} = 3.6 V	1800	1950	2200	mA
$R_{DS(ONP)}$	Boost switch on-resistance	V_{POS} = 5 V		230	300	mΩ
		V_{POS} = 10 V		170	200	
I_{LIMP}	TPS65130 Boost switch current limit	2.7 V < V_{IN} < 5.5 V	700	800	900	mA
I_{LIMP}	TPS65131 Boost switch current limit	V_{IN} = 3.6 V, V_{POS} = 8.0 V	1800	1950	2200	mA
D_{MAXP}	Maximum duty cycle boost converter			87.5%		
D_{MAXN}	Maximum duty cycle inverting converter			87.5%		
D_{MINP}	Minimum duty cycle boost converter			12.5%		
D_{MINN}	Minimum duty cycle inverting converter			12.5%		
CONTROL STAGE						
f_S	Oscillator frequency		1250	1380	1500	kHz
$V_{ENP,ENN,PSP,PSN}$	High level input voltage		1.4			V
$V_{ENP,ENN,PSP,PSN}$	Low level input voltage				0.4	V
$I_{ENP,ENN,PSP,PSN}$	Input current	ENP, ENN, PSP, PSN = GND or VIN		0.01	0.1	µA
R_{BSW}	Output resistance			27		kΩ
V_{IN}	Input voltage range		2.7		5.5	V

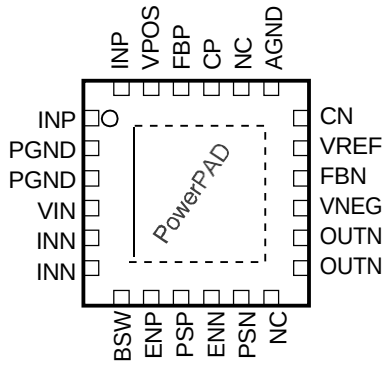
ELECTRICAL CHARACTERISTICS (continued)

Over recommended free-air temperature range and over recommended input voltage range, typical at an ambient temperature of 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(Q)}$	Quiescent current	VIN	V_{IN} = 3.6 V, I_{OUTP} = I_{OUTN} = 0, ENP = ENN = PSP = PSN = V_{IN}, V_{POS} = 8 V, V_{NEG} = -5 V		300	500	µA
		VPOS			100	120	µA
		VNEG			100	120	µA
I_{SD}	Shutdown supply current		ENN = ENP = GND		0.2	1.5	µA
V_{UVLO}	Undervoltage lockout threshold			2.1	2.35	2.7	V
	Thermal shutdown				150		°C
	Thermal shutdown hysteresis		Junction temperature decreasing		5		°C

PIN ASSIGNMENTS

HTTSOP PowerPAD™
(TOP VIEW)



NC − No internal connection

Terminal Functions

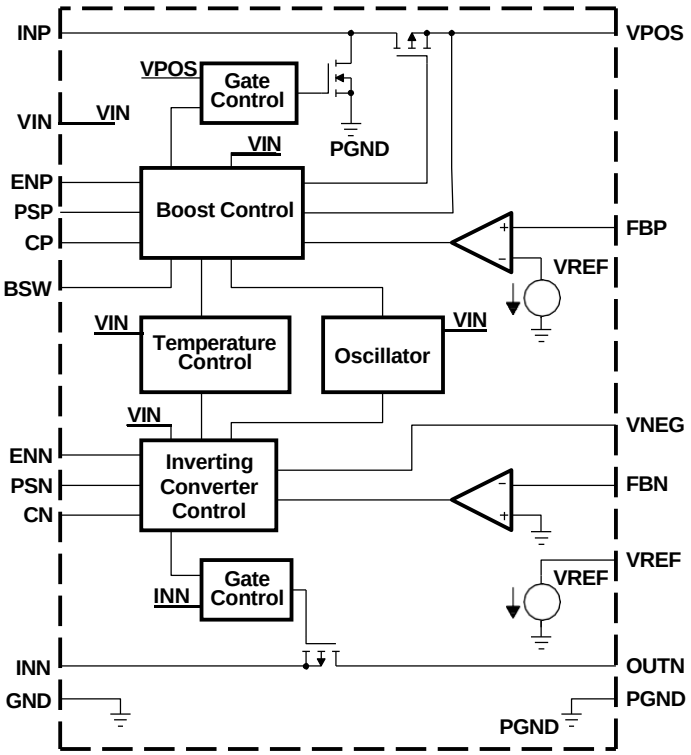
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
INP	1, 24	I	Boost converter switch input.
INN	5, 6	I	Inverting converter switch input
PGND	2, 3		Power ground pin
AGND	19		Analog ground pin
ENN	10	I	Enable pin for the negative output voltage (0 V: disabled, VIN: enabled)
ENP	8	I	Enable pin for the positive output voltage (0 V: disabled, VIN: enabled)
FBN	16	I	Feedback pin for the negative output voltage divider
FBP	22	I	Feedback pin for the positive output voltage divider
OUTN	13, 14	O	Inverting converter switch output.
VREF	17	O	Reference output voltage. Bypass this pin with a 220-nF capacitor to ground. Connect the lower resistor of the negative output voltage divider to this pin
CP	21		Compensation pin for boost converter control
CN	18		Compensation pin for inverting converter control
VIN	4	I	Control supply input
VPOS	23	I	Positive output voltage sense input
VNEG	15	I	Negative output voltage sense input

PIN ASSIGNMENTS (continued)

Terminal Functions (continued)

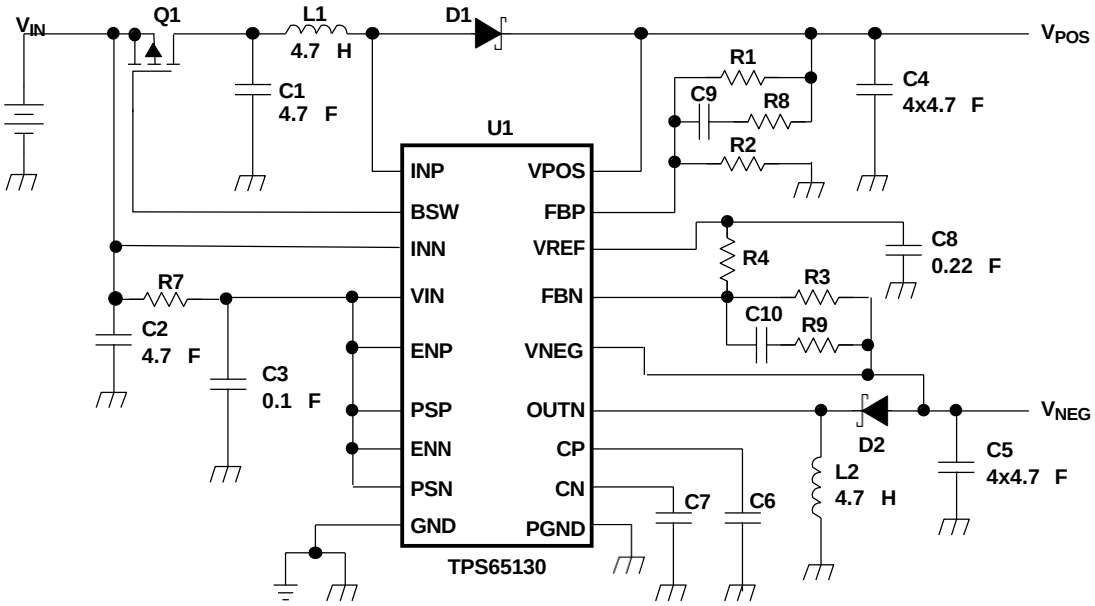
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PSP	9	I	Power-save mode enable for boost converter stage (0 V: disabled, VIN: enabled)
PSN	11	I	Power-save mode enable for inverter stage (0 V: disabled, VIN: enabled)
BSW	7	O	Gate control pin for external battery switch. This pin goes low when ENP is set high.
NC	12, 20		Not connected

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



List of Components

REFERENCE	DESCRIPTION
C1, C2	X7R/X5R ceramic
C4, C5	4x4.7 µF X7R/X5R ceramic
D1, D2	MBRM120
L1, L2	Wurth Elektronik (TPS65130), EPCOS B82462-G4472 (TPS65131)

PERFORMANCE GRAPHS

Table of Graphs

GRAPH	DESCRIPTION
Figure 1	TPS65130 maximum output current versus input voltage, V_{POS} = 12 V, 8 V, 5 V
Figure 2	TPS65131 maximum output current versus input voltage, V_{POS} = 15 V, 10 V, 5 V
Figure 3	TPS65130 maximum output current versus input voltage, V_{NEG} = –4 V, –8 V, –10 V
Figure 4	TPS65131 maximum output current versus input voltage, V_{NEG} = –4 V, –10 V, –15 V
Figure 5	TPS65130 efficiency versus output current, V_{POS}= 5 V
Figure 6	TPS65131 efficiency versus output current, V_{POS}= 5 V
Figure 7	TPS65130 efficiency versus output current, V_{POS}= 8 V
Figure 8	TPS65131 efficiency versus output current, V_{POS}= 10 V
Figure 9	TPS65130 efficiency versus output current, V_{POS}= 12 V
Figure 10	TPS65131 efficiency versus output current, V_{POS}= 15 V
Figure 11	TPS65130 efficiency versus output current, V_{NEG}= –4 V, (V_{IN} = 4 V, 3 V)
Figure 12	TPS65131 efficiency versus output current, V_{NEG}= –4 V, (V_{IN} = 5 V, 3 V)
Figure 13	TPS65130 efficiency versus output current, V_{NEG}= –8 V, (V_{IN} = 4.2 V, 3 V)
Figure 14	TPS65131 efficiency versus output current, V_{NEG}= –10 V, (V_{IN} = 5 V, 3 V)
Figure 15	TPS65130 efficiency versus output current, V_{NEG}= –10 V, (V_{IN} = 4.2 V, 3 V)

Table of Graphs (continued)

GRAPH	DESCRIPTION
Figure 16	TPS65131 efficiency versus output current, V_{NEG}= –15 V, (V_{IN} = 5 V, 3 V)
Figure 17	TPS65130 efficiency versus input voltage, V_{POS}= 5 V in power-save mode
Figure 18	TPS65130 efficiency versus input voltage, V_{POS}= 8 V in power-save mode
Figure 19	TPS65130 efficiency versus input voltage, V_{POS}= 12 V in power-save mode
Figure 20	TPS65130 efficiency versus input voltage, V_{NEG}= –4 V in power-save mode
Figure 21	TPS65130 efficiency versus input voltage, V_{NEG}= –8 V in power-save mode
Figure 22	TPS65130 efficiency versus input voltage, V_{NEG}= –10 V in power-save mode
Figure 23	TPS65130 efficiency versus output current, V_O= 13.5 V (+9 V, –4.5 V), (V_{IN} = 4.2 V, 3 V)
Figure 24	TPS65131 efficiency versus output current, V_O= 30 V (±15 V, (V_{IN} 5 V, 3 V)
Figure 25	TPS65130 efficiency versus input voltage, V_O= 13.5 V (9 V, –4.5 V) in power save mode
Figure 26	TPS65130 output voltage versus output current, V_{POS}= 5 V, V_{IN} = 3 V
Figure 27	TPS65131 output voltage versus output current, V_{POS}= 5 V, V_{IN} = 4.2 V
Figure 28	TPS65130 output voltage versus output current, V_{POS}= 8 V, V_{IN} = 3 V
Figure 29	TPS65131 output voltage versus output current, V_{POS}= 10 V, V_{IN} = 5 V
Figure 30	TPS65130 output voltage versus output current, V_{POS}= 12 V (V_{IN} = 3 V)
Figure 31	TPS65131 output voltage versus output current, V_{POS}= 15 V (V_{IN} = 5 V)
Figure 32	TPS65130 output voltage versus output current, V_{NEG}= –4 V, V_{IN} = 3 V
Figure 33	TPS65131 output voltage versus output current, V_{NEG}= –4 V, V_{IN} = 5 V
Figure 34	TPS65130 output voltage versus output current, V_{NEG}= –8 V, V_{IN} = 3 V
Figure 35	TPS65131 output voltage versus output current, V_{NEG}= –10 V, V_{IN} = 5 V
Figure 36	TPS65130 output voltage versus output current, V_{NEG}= –10 V, V_{IN} = 3 V
Figure 37	TPS65131 output voltage versus output current, V_{NEG}= –15 V, V_{IN} = 5 V
Figure 38	No load supply current into V_{IN} versus input voltage
Figure 39	No load supply current into V_{POS} versus input voltage
Figure 40	No load supply current into V_{NEG} versus input voltage
Figure 41	Positive output voltage in continuous current mode
Figure 42	Negative output voltage in continuous current mode
Figure 43	Positive output voltage at power-save mode disabled
Figure 44	Negative output voltage at power-save mode disabled
Figure 45	Positive output voltage in power-save mode, V_I = 3.6 V, V_{POS} = 5.5 V
Figure 46	Negative output voltage in power-save mode, V_I = 3.6 V, V_{NEG} = –8 V
Figure 47	Load transient response, V_I = 3.6 V, V_{POS} = 8 V
Figure 48	Load transient response, V_I = 3.6 V, V_{NEG} = –8 V
Figure 49	Line transient response, V_I = 3.6 V to 4.2 V, V_{POS} = 8 V
Figure 50	Line transient response, V_I = 3.6 V to 4.2 V, V_{NEG} = –8 V
Figure 51	Start-up after enable, V_{POS} = 8 V, V_I = 3.6 V
Figure 52	Start-up after enable, V_{NEG} = –8 V, V_I = 3.6 V

TYPICAL CHARACTERISTICS

TPS65130
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

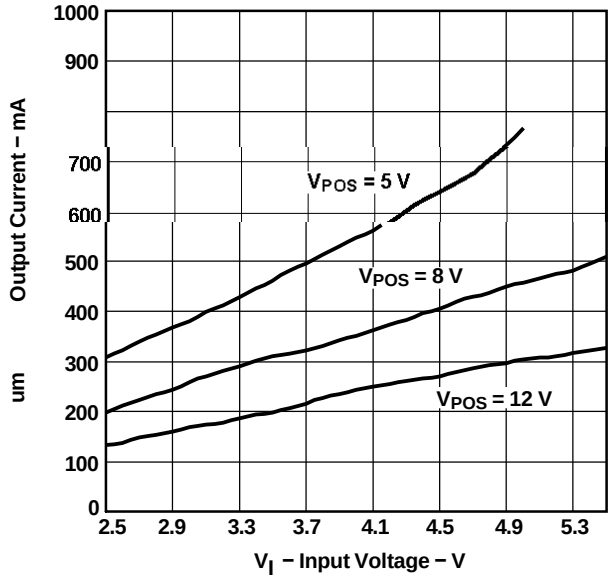


Figure 1.

TPS65131
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

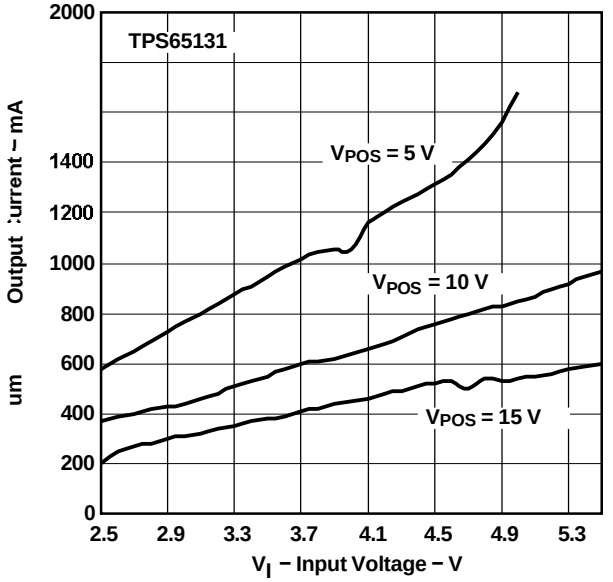


Figure 2.

TPS65130
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

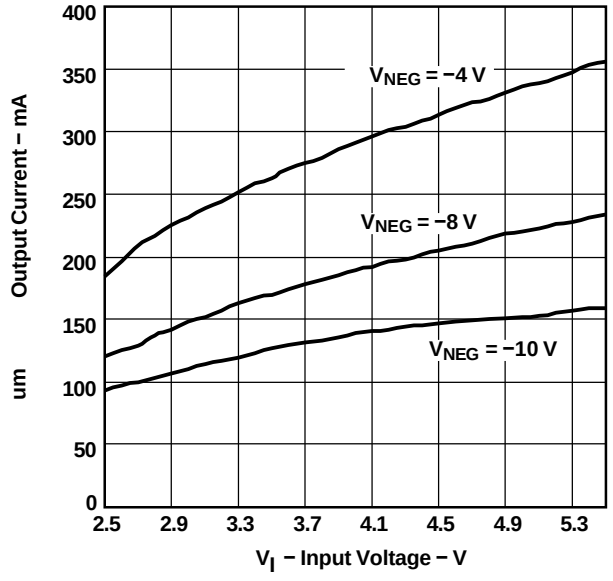


Figure 3.

TPS65131
MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

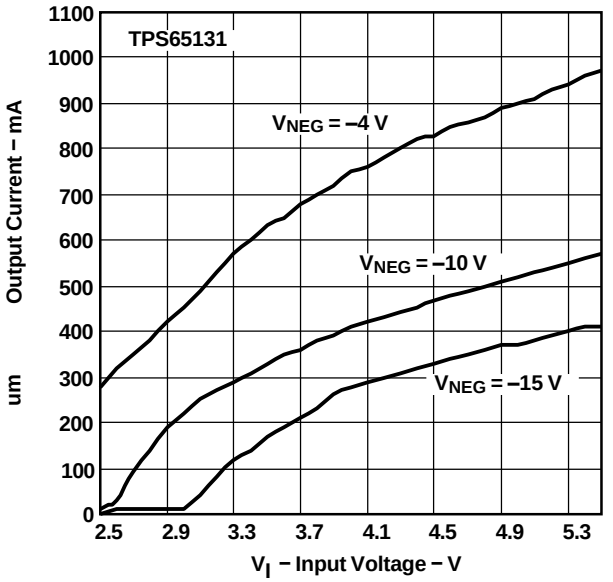


Figure 4.

TYPICAL CHARACTERISTICS (continued)

TPS65130
EFFICIENCY
vs
OUTPUT CURRENT

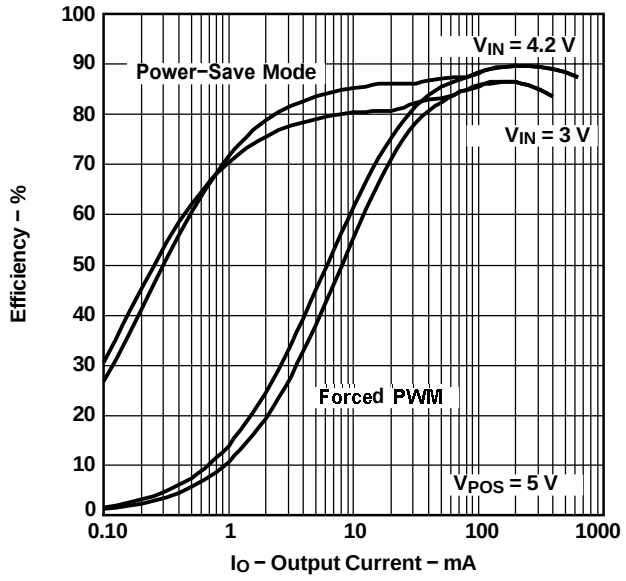


Figure 5.

TPS65131
EFFICIENCY
vs
OUTPUT CURRENT

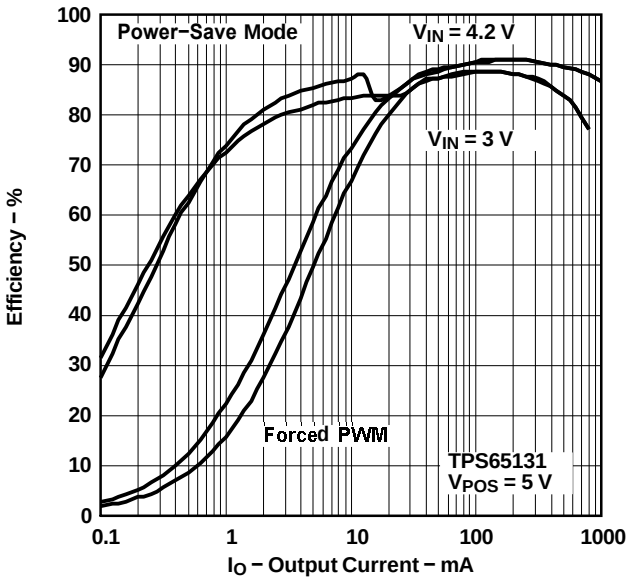


Figure 6.

TPS65130
EFFICIENCY
vs
OUTPUT CURRENT

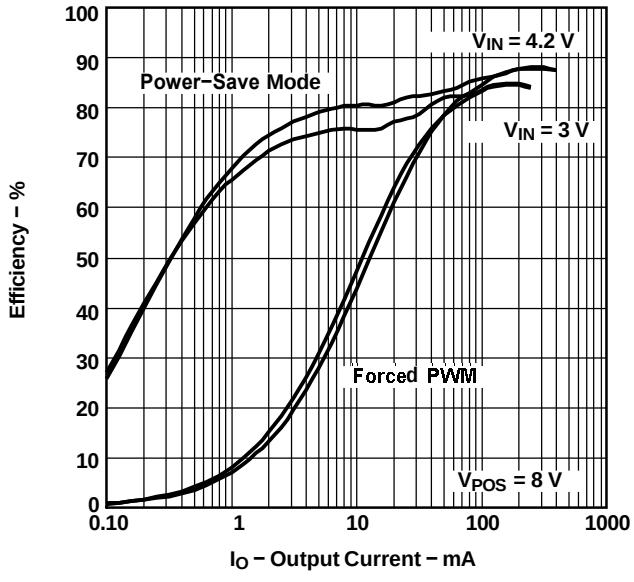


Figure 7.

TPS65131
EFFICIENCY
vs
OUTPUT CURRENT

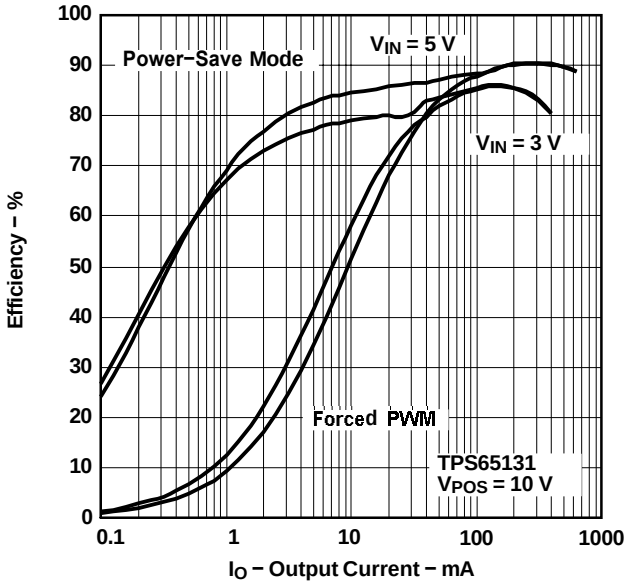


Figure 8.