❑ MN101D06F , MN101D06G , MN101D06H

Type	MN101D06F	MN101D06G	MN101D06H
ROM (×8-bit)	96 K	128 K	160 K
RAM (×8-bit)	3 K	4 K	5 K

Package QFP100-P-1818B *Lead-free

Minimum Instruction Execution Time
With main clock operated 0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz)
71.5 µs (at 3.0 V to 5.5 V fixed to 14.3 MHz inte al frequenc division)
When sub-clock operated 61 µs (at 2.2 V to 5.5 V, 32.768 kHz)

Interrupts
• RESET • Runaway • External 0 • External 1 • External 2 • External 3 • Ex nal 4 • key input (P50 to 54)
• Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • C stan FG • Contr 1 • HSW
• Cylinder(Drum) FG • Servo V-sync • Synchronous output • OS • XDS Serial 0 • Serial 1 • Serial 2
• A/D (common with PWM 4 reference frequency) • OSD V-sync

Timer Counter

Timer counter 0: 16-bit × 1
(timer function, clock function [max. 2 s or max. 36 h at cascade nnecting with timer 6])
Clock source ····· 1/2, (1/4,) 1/8, (1/16) of system clock frequency; overflow of timer counter 6; 1/512 of XI oscil tion clock or OSC oscillation clock frequency
Interrupt source ····· overflow of timer unter 0

Timer counter 1: 16-bit × 1 (timer function linear tim r counter function)
Clock source ····· 1/2, (1/4,) /8, (1/16) f system clock frequency; CTL signal
Interrupt source ····· overflow of t er counter 1

Timer counter 2: 16-bit × 1 (timer functi input ure, duty judgment of CTL signal(VISS/VASS detection function))
Clock source ····· 1/2 (1/4,) 1/8, (1/16,) 1/12, (1/24) of system clock frequency
Interrupt source ····· overflow imer counter 2; input of CTL specified edge; underflow of timer 2 ift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shif gister compare register

Timer counter 3: 16 bit × 1
(timer function, detec n of serial indexing, generation of remote control output carrier frequency)
Clock source ····· 1/2, (1/4,) 1/8, (1/16) of system clock frequency; XI oscillation clock
Inte rupt source ····· verflow of timer counter 3

Timer counter 4 16-bit × 1 (timer function, event count [P15 input], generation of serial transmission clock)
Cl k sou e ····· 1/8, (1/16) of system clock frequency; external clock input
In rrupt source ····· overflow of timer counter 4; coincidence of timer counter 4 with OCR4

Timer co 5: 19-bit × 1 (watchdog, stable oscillation waiting function)
Clock source ····· system clock
Watchdog interrupt source ·· $1/2^{16}$, $1/2^{19}$ of timer counter 5 frequency
Clear by stable oscillation ·· after 256 counts by timer counter 5 (2^{18} counts of OSC oscillation clock)

mer counter 6: 16-bit × 1 (clock function [max. 2 s])
Clock source ····· 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/4, (1/8,) 1/64, (1/128) of system clock frequency

Serial Interface

13 14 15

[redacted] input
terrupt vector.)
B selectable)

Synchronous type clock source 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT0 pin input
Clock for UART ····· 8-division of above clock; 2-division timer 4 output; NSBT0 pin input

Serial Interface (Continue)

Serial 1: 8-bit × 1
(synchronous type/remote control transmission/simple remote control receive) (transfer direction of MSB/LSB selectable, start condition function)

Clock source ·····1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT1 pin input

Remote control clock ·····2-division timer 4 output

Serial 2: 8-bit × 1 (I^2C) (master transmission/reception, slave transm sion/rec tion)

Clock source ·····1/144 to 1/252 of system clock; SCK i input

OSD

OSD mode: Accommodation with menu(internal synchronous) or super impo (external synchronous) display

Applicable broadcasting system:NTSC, PAL, PAL-M, PA N

Screen configuration	: 24 characters × 2n ro s (n = 1 6)
Character type	: max. 512 character es (variable, incude special characters)
Character size	: 12 × 18 dots (Vertical d ction: 1 dot for 2H at not enlargement)
Enlarged characters	: each × 2, × 3 or × settings i horizontal and vertical
Character interpolation	: none
Line background color	: 8-hue settable (settable in the row unit at menu display)
Line background intensity	: 8 grad ons settable i the row unit (at output of composite video signal)
Screen background color	: 8-hue s table (at output of composite video signal)
Character color	: white (a utput of composite video signal)
Character intensity	8 gradatio s settable in the row unit (at output of composite video signal)
Frame function	: 1 dot frame n 4 or 8 directions
Frame intensity	: 4 gr dations settable in the row unit (at output of composite video signal)
Box shade function	: sett in the character unit (at output of composite video signal with 129 or more characters (character types))
Blinking	ne (covered by software)
Inverted charac r	: settable in the character unit
Halftone	: settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal)

CCD mode: Sup rts Clo d C tion in the U.S.A.

Screen config ration	: 32 characters × 16 rows
Character type	: max. 128 character types (variable)
haracter size	: 12 × 26 dots (Vertical direction: 1 dot for 1H, including 8 dots in the underlined area)
Enlarged characters	: none
Cha interpolation	: none
ine background color	: 8-hue settable
L background intensity	: 8 gradations settable in the screen unit (at output of composite video signal)
Screen background color	: 8-hue settable (at output of composite video signal)
Character color	: 8 colors (at RGB output)
	: White (at output of composite video signal)
Character intensity	: 8 gradations settable in the screen unit (at output of composite video signal)
Frame function	: none
Box shade function	: none
Inverted character	: none
Halftone	: settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal)
Others	: Underline, italic, blinking function and scroll
Input	: composite video signal input (output level: 1 V[p-p] / 2 V[p-p])
Clamp method	: sync tip clamp, clamp level in 4 levels
Output	: composite video output
	: digital output (6 pins)
Measure against image fluctuation	: built-in AFC circuit
Dot clock	: 1/2 of OSC oscillation clock (automatic phase adjustment)

See the next page for electrical characteristics, pin assignment and support tool.

XDS			Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.)
ROM Correction			Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM
I/O Pins	**I/O**	75	• Common use: 66
	Input	2	• Common use: 2
A/D Inputs			8-bit × 13-ch. (without S/H)
PWM			13-bit × 2-ch. (at repetition cycle 572 µs at 14.32 MHz), 10-bit × 2-ch. (at repetition cycle 71.5 µs at 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 71.5 µs, 0.572 ms, 1.14 ms, 2.29 m at 32 MHz)
ICR			18-bit × 6-ch.
OCR			16-bit × 2 (8-bit synchronous output; 4-bit 3-state synchro ous outp 16-bit × 1 (weak electric field V-sync backup), 16-bit × 1 (Rec TL)
Special Ports			Buzzer output; 3-state output VLP pin; remote control receive; CTL signal input terminal; Capstan FG inputterminal; Sylinder(Durm) PG/FG input terminals; HSW output terminal; Head Amp/Rortary control tput terminals; output of 1/2 OSC oscillation clock (2 V[p-p]) tp f 1/4 OSC oscillation clock (1 V[p-p])

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MH p ation without load, VDD = 5 V		60	100	mA
	IDD2	1/1024 of 14 32 MHz ope a on without load, VDD = 3.0 V		2	5	mA
	IDD3	Stop of 1 32 MHz oscillation, VDD = 2.7 V 32 kH oscillation operation without load		50	100	µA
Supply current at STOP	IDSP	Stop of oscillation ithout load, VDD = 5 V, Ta = 55 °C			10	µA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	µA

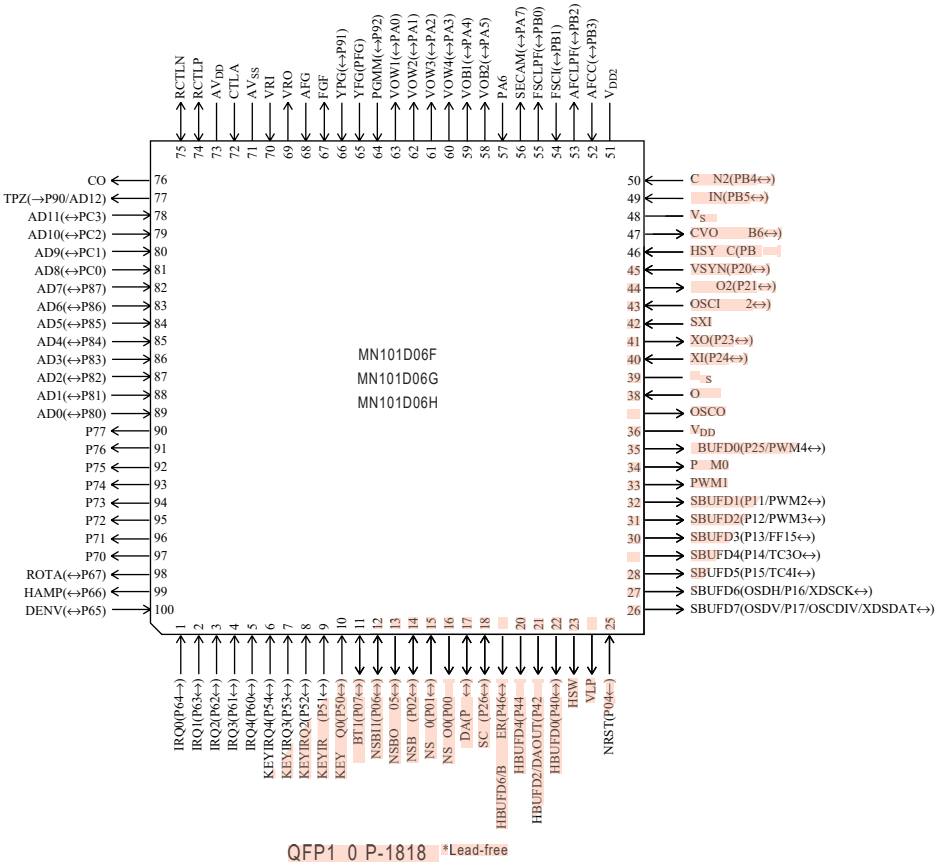
(Ta = 25 °C ± 2 °C , VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time						µs
Analog Input Voltage					5	V

0 V , VSS = 0 V)

Pin Assignment



Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101D -QFP100-P-1818B-M	
Flash Memory Built-in Type	Type	MN101DF06ZAF
	ROM (× 8 bit)	224 K
	RAM (× bit	6 K
	Mi mum instruction execution time	0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 µs (at 3.0 V to 5.5 V, fixed to 14.32 MHz internal division) 61 µs (at 2.5 V to 5.5 V, 32.768 kHz)
	Package	QFP100-P-1818B *Lead-free

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RAM (8 位)ROM (8 位)类型封装 QFP100-P-1818B *无铅
MN101D06F ,MN101D06G ,MN101D06H
最小指令执行时间主时钟运行时
0.1397 秒（4.0 V 至 5.5 V，14.32 MHz）
71.5 秒（3.0 V 至 5.5 V 固定为 14.32 MHz　　分频）
副时钟运行时
61 秒（2.2 V 至 5.5 V，32.768 kHz）
中断
RESET 失控外部 0 外部 1 外部 2 外部 3 外部 4 键输入（P50 至 54）
定时器 0 定时器 1 定时器 2 定时器 3 定时器 4 定时器 6 主动轮 FG 控制 HSW
气缸（滚筒）FG 伺服 V-sync 同步输出 OSD XDS 串行 0 串行 1 串行 2
A/D（与 PWM 4 参考频率共用）OSD V-sync
定时器计数器定时器计数器 0：16 位 1
定时器功能，时钟功能［最大 2 秒或与定时器 6 级联时最大 36 小时］)
时钟源系统时钟频率的 1/2、(1/4、) 1/8、(1/16)；定时器计数器 6 溢出；
XI 振荡时钟或 OSC 振荡时钟频率的 1/512
定时器计数器 0 的中断源溢出定时器计数器 1：16 位 1（定时器功能、线性定时器计数器功能）
时钟源系统时钟频率的 1/2、(1/4、) 1/8、(1/16)；CTL 信号定时器计数器 1 的中断源溢出定时器计数器 2：16 位 1（定时器功能、输入捕获、CTL 信号的占空比判断（VISS/VASS 检测功能）
时钟源系统时钟频率的 1/2、(1/4、) 1/8、(1/16、) 1/12、(1/24)
定时器计数器 2 的中断源溢出；CTL 指定边沿的输入；定时器 2 的下溢移位寄存器 4 位计数器；定时器 2 移位寄存器与定时器 2 一致移位寄存器比较寄存器定时器计数器 3：16 位 1
定时器功能、串行索引检测、遥控输出载波频率生成)
时钟源系统时钟频率的 1/2、(1/4、)1/8、(1/16)；XI 振荡时钟定时器计数器 3 的中断源溢出定时器计数器 4：16 位 1 (定时器功能、事件计数［P15 输入］、串行传输时钟生成)
时钟源系统时钟频率的 1/8、(1/16)；外部时钟输入定时器计数器 4 的中断源溢出；定时器计数器 4 与 OCR4 一致定时器计数器 5：19 位 1 (看门狗、稳定振荡等待功能)
时钟源系统时钟看门狗中断源定时器计数器 5 频率的 1/216、1/219
定时器计数器 5 计数 256 次后稳定振荡清除 (OSC 振荡时钟的 218 次计数)

定时器计数器 6:16 位 1（时钟功能　大 2 秒]）
时钟源 OSC 振荡时钟频率的 1/512　I 振荡时钟；
系统时钟频率的 1/4、(1/8、)1/6　(1/128)
中断源定时计数器 6 的 1/213、1　4、1/215 溢出定时计数器 7：8 位 1 或 4 位 2（定时器功能，事件计数）
时钟源系统时钟频率的 1/4、(1/8　1/16、(1/32)；外部时钟输入中断源定时计数器 7 溢出（虽然 4 位 2 时有一个中断向量。）
串行接口串行 0：8 位 1（同步型　停同步型）(MSB/LSB 传输方向可选）
同步型时钟源系统时钟频率的 1/8　/16、1/32、1/64、1/128、1/256；
2 分频定时器 4 输出；NSBT0 引脚输入
UART 时钟上述时钟的 8 分频；2 分频定时器 4 输出；NSBT0 引脚输入
96 K MN101D06F 3 K 128 K MN101D06G 4 K 160 K MN101D06H 5 K MAD00029FEM
s (4.0 V 至 5.5 V, 14.32 MHz)

s (4.0 V 至 5.5 V, 14.32 MHz)
s (3.0 V 至 5.5 V 固定为 14.32 MHz　分频)
s (3.0 V 至 5.5 V 固定为 14.32 MHz　分频)
s (2.2 V 至 5.5 V,32.768 kHz)
s (2.2 V 至 5.5 V,32.768 kHz)
RESET 失控外部 0 外部 1 外部 2 外部 3 外部 4 键输入 (P50 至 54)

RESET 失控外部 0 外部 1 外部 2 外部 3 外部 4 键输入 (P50 至 54)
定时器 0 定时器 1 定时器 2 定时器 3 定时器 4 定时器 6 绞盘 FG 控制 HSW
定时器 0 定时器 1 定时器 2 定时器 3 定时器 4 定时器 6 绞盘 FG 控制 HSW
气缸 (滚筒)FG 伺服 V-sync 同步输出 OSD XDS 串行 0 串行 1 串行 2
气缸(滚筒)FG 伺服 V-sync 同步输出 OS　DS 串　0 串行　串　2

A/D (与 PWM 4 参考频率共用)OSD V-sync

A/D (与 PWM 4 参考频率共用)OSD V-sync
定时器功能，时钟功能[与定时器 6 级联时最大 2 秒或最大 36 小时])

定时器功能，时钟功能[与定时器 6 级联时最大 2 秒或最大 36 小时])
系统时钟频率的 1/2，(1/4,) 1/8，(1/16)；定时器计数器 6 溢出;

系统时钟频率的 1/2，(1/4,) 1/8，(1/16)；定时器计数器 6 溢出;
XI 振荡时钟或 OSC 振荡时钟频率的 1/512

XI 振荡时钟或 OSC 振荡时钟频率的 1/512
溢出定时器计数器 0 溢出
定时器计数器 0

1 (定时器功能，线性定时器计数器功能)

1 (定时器功能，线性定时器计数器功能)

系统时钟频率的 1/2,(1/4,)1/8,(1/16)；CTL 信号

系统时钟频率的 1/2,(1/4,)1/8,(1/16)；CTL 信号
溢出定时器计数器 1 溢出
定时器计数器 1

1 (定时器功能，输入捕获、CTL 信号占空比判断（VISS/VASS 检测功能）

1 (定时器功能、输入捕获、CTL 信号占空比判断（VISS/VASS 检测功能）

系统时　　率　　(1/4　1/8、(　6、　　、(　4)

系统时钟频率的 1/2、(1/4、)1/8、(1/16、)1/12、(1/24)
中断源
中断源

定时器计数器 2 溢出；CTL 指定边沿　　入；定时器 2 下溢

定时器计数器 2 溢出；CTL 指定边沿的输入；定时器 2 下溢移位寄存器 4 位计数器；定时器 2 移位寄存器一致带定时器 2

移位寄存器 4 位计数器；定时器 2 移位寄存器与定时器 2 一致移位　　器比较寄存器

移位寄存器比较寄存器定时器计数器 3：16 位　　定时　　数器 3：16 位　　1　　1
定时器功能，检测串行索引，产生远程控制输出载波频率)

定时器功能，检测串行索引，产生远　　制输出载波频率)
时钟源
时钟源

系统时钟频率的 1/2，(1/4，)1/8，(　6)；XI 振荡时钟

系统时钟的 1/2，(1/4，)1/8，(1/16)频率;XI 振荡时钟中断源
中断源溢出
　　溢出定时器计数器 4：16 位　　定时器计数器 4：16 位
1 (定时器功能，事件计数[P15 输入]，串行传输时钟的生成)

1 (定时　　能，事件计数[P15 输入]，串行传输时钟的生成)
时钟源
时钟源
　　断
中断源 t　　出

ti 溢出　器计数器　19 位　定时器计数器 5：19 位　时钟源
时钟源
看门　断源　看门狗中断源通过稳定振荡清除
通过稳　荡清除定时器计数器 6：16 位 定时器计数器 6：16 位时钟源 时钟源定时器计数器 7：8 位 定时器计数器 7：8 位 MN101D06F、MN101D06G、MN101D06H 串行接口（续）串行 1：8 位 1
同步型/　发送/简易遥控接收）(MSB/LSB 传输方向可选，启动条件功能）
时钟源　时钟频率的 1/8、1/16、1/32、1/64、1/128、1/256；
2 分频定　4 输出；NSBT1 引脚输入遥控时钟 2 分频定时器 4 输出串行 2：8 位 1（I2C）（主发送/接收，从属发送/接收）
时钟源系统时钟的 1/144 至 1/252；SCK 引脚输入
OSD OSD 模式：
适应菜单（　同步）或叠加（外部同步）显示适用广播系统：NTSC，PAL，PAL-M，PAL-N
屏幕配置
24 个字符 2n 行（n =　6）
字符类型最大 512 个　类型（可变，包括特殊字符）
字符大小
12 18 点　直　向　时 2H 为 1 点）
放大字　平　直　或 4 个设置字符插值：无线背景颜色
8 种色　设　菜单显　时可按行设置）
行背景
8 种灰　按　置（复　视频信号输出时）
屏幕背景颜色 8　色调　置（复合视频信号输出时）
字符颜色白色（复合视频　号输出时）
字符强度
8 个等级可按行设置（复　视频信号输出时）
框架功能
4 或　个方向　框　框架强度
4 个　可按　复　视频信号输出时）