FFT IP Core

User Guide

Updated for Intel® Quartus® Prime Design Suite: **17.1**

Online Version
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UG-FFT

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Contents

1. About This IP Core

Related Information

- FFT IP Core User Guide Document Archive on page 50
  Provides a list of user guides for previous versions of the FFT IP core.
- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

1.1. Intel® DSP IP Core Features

- Avalon® Streaming (Avalon-ST) interfaces
- DSP Builder for Intel® FPGAs ready
- Testbenches to verify the IP core
- IP functional simulation models for use in Intel-supported VHDL and Verilog HDL simulators

1.2. FFT IP Core Features

- Bit-accurate MATLAB models
- Variable streaming FFT:
  - Single-precision floating-point or fixed-point representation
  - Radix-4, mixed radix-4/2 implementations (for floating-point FFT), and radix-2^2 single delay feedback implementation (for fixed-point FFT)
  - Input and output orders: natural order, or digit-reversed, and DC-centered (-N/2 to N/2)
  - Reduced memory requirements
  - Support for 8 to 32-bit data and twiddle width (foxed-point FFTs)
- Fixed transform size FFT that implements block floating-point FFTs and maintains the maximum dynamic range of data during processing (not for variable streaming FFTs)
  - Multiple I/O data flow options: streaming, buffered burst, and burst
  - Uses embedded memory
  - Maximum system clock frequency more than 300 MHz
  - Optimized to use Stratix series DSP blocks and TriMatrix memory
  - High throughput quad-output radix 4 FFT engine
  - Support for multiple single-output and quad-output engines in parallel
- User control over optimization in DSP blocks or in speed in Stratix V devices, for streaming, buffered burst, burst, and variable streaming fixed-point FFTs
- Avalon Streaming (Avalon-ST) compliant input and output interfaces
- Parameterization-specific VHDL and Verilog HDL testbench generation
- Transform direction (FFT/IFFT) specifiable on a per-block basis

1.3. General Description

The FFT IP core is a high performance, highly-parameterizable Fast Fourier transform (FFT) processor. The FFT IP core implements a complex FFT or inverse FFT (IFFT) for high-performance applications.

The FFT MegaCore function implements:

- Fixed transform size FFT
- Variable streaming FFT

1.3.1. Fixed Transform Size FFT

The fixed transform FFT implements a radix-2/4 decimation-in-frequency (DIF) FFT fixed-transform size algorithm for transform lengths of 2m where 6 ≤ m ≤16. This FFT uses block-floating point representations to achieve the best trade-off between maximum signal-to-noise ratio (SNR) and minimum size requirements.

The fixed transform FFT accepts a two's complement format complex data vector of length N inputs, where N is the desired transform length in natural order. The function outputs the transform-domain complex vector in natural order. The FFT produces an

accumulated block exponent to indicate any data scaling that has occurred during the transform to maintain precision and maximize the internal signal-to-noise ratio. You can specify the transform direction on a per-block basis using an input port.

1.3.2. Variable Streaming FFT

The variable streaming FFT implements two different types of FFT. The variable streaming FFTs implement either a radix-2^2 single delay feedback FFT, using a fixed-point representation, or a mixed radix-4/2 FFT, using a single precision floating point representation. After you select your FFT type, you can configure your FFT variation during runtime to perform the FFT algorithm for transform lengths of 2m where $3 \leq m \leq 18$.

The fixed-point representation grows the data widths naturally from input through to output thereby maintaining a high SNR at the output. The single precision floating-point representation allows a large dynamic range of values to be represented while maintaining a high SNR at the output.

The order of the input data vector of size N can be natural or digit-reversed, or -N/2 to N/2 (DC-centered). The fixed-point representation supports a natural or DC-centered order and the floating point representation supports a natural, digit-reversed order. The FFT outputs the transform-domain complex vector in natural or digit-reversed order. You can specify the transform direction on a per-block basis using an input port.

1.4. DSP IP Core Device Family Support

Intel offers the following device support levels for Intel FPGA IP cores:

- Advance support—the IP core is available for simulation and compilation for this device family. FPGA programming file (`.pof`) support is not available for Quartus Prime Pro Stratix 10 Edition Beta software and as such IP timing closure cannot be guaranteed. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- Preliminary support—Intel verifies the IP core with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. You can use it in production designs with caution.
- Final support—Intel verifies the IP core with final timing models for this device family. The IP core meets all functional and timing requirements for the device family. You can use it in production designs.

Table 1. DSP IP Core Device Family Support

Device Family	Support
Arria® II GX	Final
Arria II GZ	Final
Arria V	Final

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Device Family	Support
Intel Arria 10	Final
Cyclone® IV	Final
Cyclone V	Final
Intel Cyclone 10	Final
Intel MAX® 10 FPGA	Final
Stratix® IV GT	Final
Stratix IV GX/E	Final
Stratix V	Final
Intel Stratix 10	Advance
Other device families	No support

1.5. DSP IP Core Verification

Before releasing a version of an IP core, Intel runs comprehensive regression tests to verify its quality and correctness. Intel generates custom variations of the IP core to exercise the various parameter options and thoroughly simulates the resulting simulation models with the results verified against master simulation models.

1.6. FFT IP Core Release Information

Table 2. FFT IP Core Release Information

Item	Description
Version	17.1
Release Date	November 2017
Ordering Code	IP-FFT

Related Information

- Intel FPGA IP Release Notes
- Errata for FIR II IP core in the Knowledge Base

1.7. Performance and Resource Utilization

Table 3. Performance and Resource Utilization

Typical performance using the Quartus Prime software with the Arria V (5AGXFB3H4F40C4), Cyclone V (5CGXFC7D6F31C6), and Stratix V (5SGSMD4H2F35C2) devices

Device	Parameters			ALM	DSP Blocks	Memory		Registers		f_{MAX} (MHz)
	Type	Length	Engines			M10K	M20K	Primary	Secondary	
Arria V	Buffered Burst	1,024	1	1,572	6	16	--	3,903	143	275
Arria V	Buffered Burst	1,024	2	2,512	12	30	--	6,027	272	274

continued...

Device	Parameters			ALM	DSP Blocks	Memory		Registers		f_{MAX} (MHz)
	Type	Length	Engines			M10K	M20K	Primary	Secondary	
Arria V	Buffered Burst	1,024	4	4,485	24	59	--	10,765	426	262
Arria V	Buffered Burst	256	1	1,532	6	16	--	3,713	136	275
Arria V	Buffered Burst	256	2	2,459	12	30	--	5,829	246	245
Arria V	Buffered Burst	256	4	4,405	24	59	--	10,539	389	260
Arria V	Buffered Burst	4,096	1	1,627	6	59	--	4,085	130	275
Arria V	Buffered Burst	4,096	2	2,555	12	59	--	6,244	252	275
Arria V	Buffered Burst	4,096	4	4,526	24	59	--	10,986	438	265
Arria V	Burst Quad Output	1,024	1	1,565	6	8	--	3,807	147	273
Arria V	Burst Quad Output	1,024	2	2,497	12	14	--	5,952	225	275
Arria V	Burst Quad Output	1,024	4	4,461	24	27	--	10,677	347	257
Arria V	Burst Quad Output	256	1	1,527	6	8	--	3,610	153	272
Arria V	Burst Quad Output	256	2	2,474	12	14	--	5,768	233	275
Arria V	Burst Quad Output	256	4	4,403	24	27	--	10,443	437	257
Arria V	Burst Quad Output	4,096	1	1,597	6	27	--	3,949	151	275
Arria V	Burst Quad Output	4,096	2	2,551	12	27	--	6,119	223	275
Arria V	Burst Quad Output	4,096	4	4,494	24	27	--	10,844	392	256
Arria V	Burst Single Output	1,024	1	672	2	6	--	1,488	101	275
Arria V	Burst Single Output	1,024	2	994	4	10	--	2,433	182	275
Arria V	Burst Single Output	256	1	636	2	3	--	1,442	95	275
Arria V	Burst Single Output	256	2	969	4	8	--	2,375	152	275
Arria V	Burst Single Output	4,096	1	702	2	19	--	1,522	126	270
Arria V	Burst Single Output	4,096	2	1,001	4	25	--	2,521	156	275
Arria V	Streaming	1,024	—	1,880	6	20	--	4,565	167	275

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