K9XXG08UXD

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Document Title

4G x 8 Bit/ 8G x 8 Bit/ 16G x 8 Bit NAND Flash Memory

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	Mar. 14th 2008	Advance
0.1	1. K9PDG08U5D-L's package thickness is changed. 2. $\overline{CE}$ and R/$\overline{B}$ pin location of K9PDG08U5D-L is changed.	Oct. 16th 2008	Preliminary
0.2	1. Interleaving operation is modified. 2. Interleaving page read operation is added.		

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4G x 8 Bit/ 8G x 8 Bit/ 16G x 8 Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9LBG08U0D-P	2.7V ~ 3.6V	x8	TSOP1
K9HCG08U1D-P			
K9MDG08U5D-P			TSOP1-DSP
K9HCG08U1D-I			52TLGA
K9PDG08U5D-L			52TLGA(14x18)

FEATURES

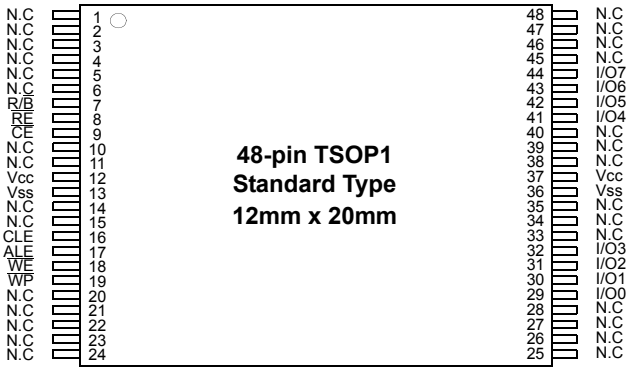
- Voltage Supply
  - 3.3V Device : 2.7V ~ 3.6V
- Organization
  - Memory Cell Array : (2G + 109M) x 8bit
  - Data Register : (4K + 218) x 8bit
- Automatic Program and Erase
  - Page Program : (4K + 218)Byte
  - Block Erase : (512K + 27.25K)Byte
- Page Read Operation
  - Page Size : (4K + 218)Byte
  - Random Read : 60μs(Max.)
  - Serial Access : 30ns(Min.)
  *K9XDG08U5D: 50ns(Min.)
- Memory Cell : 2bit / Memory Cell
- Fast Write Cycle Time
  - Program time : 800μs(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : TBD Cycles(with TBD ECC)
  - Data Retention : TBD Years
- Command Register Operation
- Unique ID for Copyright Protection
- Package :
  - K9LBG08U0D-PCB0/PIB0 : Pb-FREE PACKAGE
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9HCG08U1D-PCB0/PIB0 : Pb-FREE PACKAGE
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9MDG08U5D-PCB0/PIB0: Two K9HCG08U1D packages stacked
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch) : Pb-FREE PACKAGE
  - K9HCG08U1D-ICB0/IIB0
    52 - Pin TLGA (12 x 17 / 1.00 mm pitch)
  - K9PDG08U5D-LCB0/LIB0 : Pb/Halogen-FREE PACKAGE
    52 - Pin TLGA (14 x 18 / 1.00 mm pitch)

GENERAL DESCRIPTION

Offered in 4Gx8bit, the K9LBG08U0D is a 32G-bit NAND Flash Memory with spare 1,744M-bit. The device is offered in 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 800μs on the 4,314-byte page and an erase operation can be performed in typical 1.5ms on a (512K+27.25K)byte block. Data in the data register can be read out at 30ns(K9XDG08U5D: 50ns) cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9LBG08U0D's extended reliability of TBD cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9LBG08U0D is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

PIN CONFIGURATION (TSOP1)

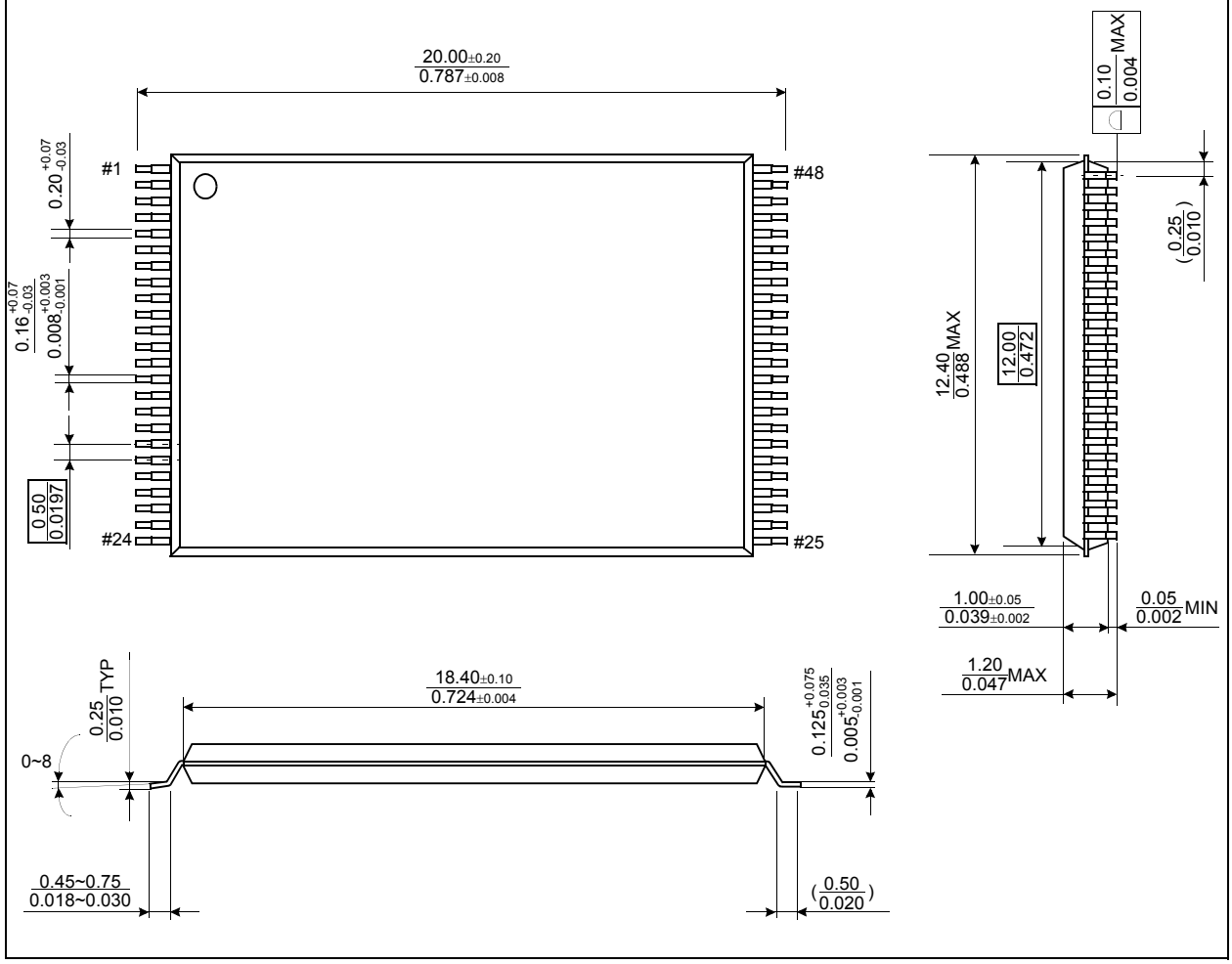
K9LBG08U0D-PCB0/PIB0



PACKAGE DIMENSIONS

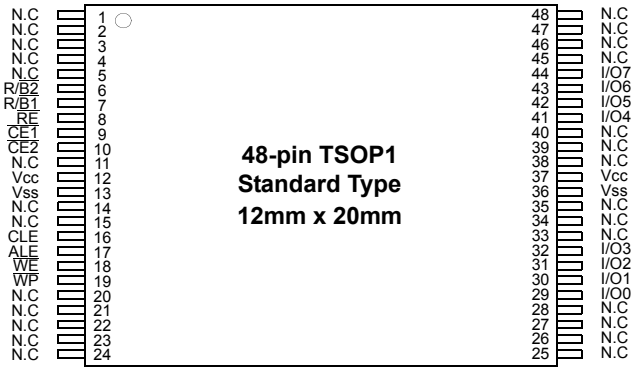
48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



PIN CONFIGURATION (TSOP1)

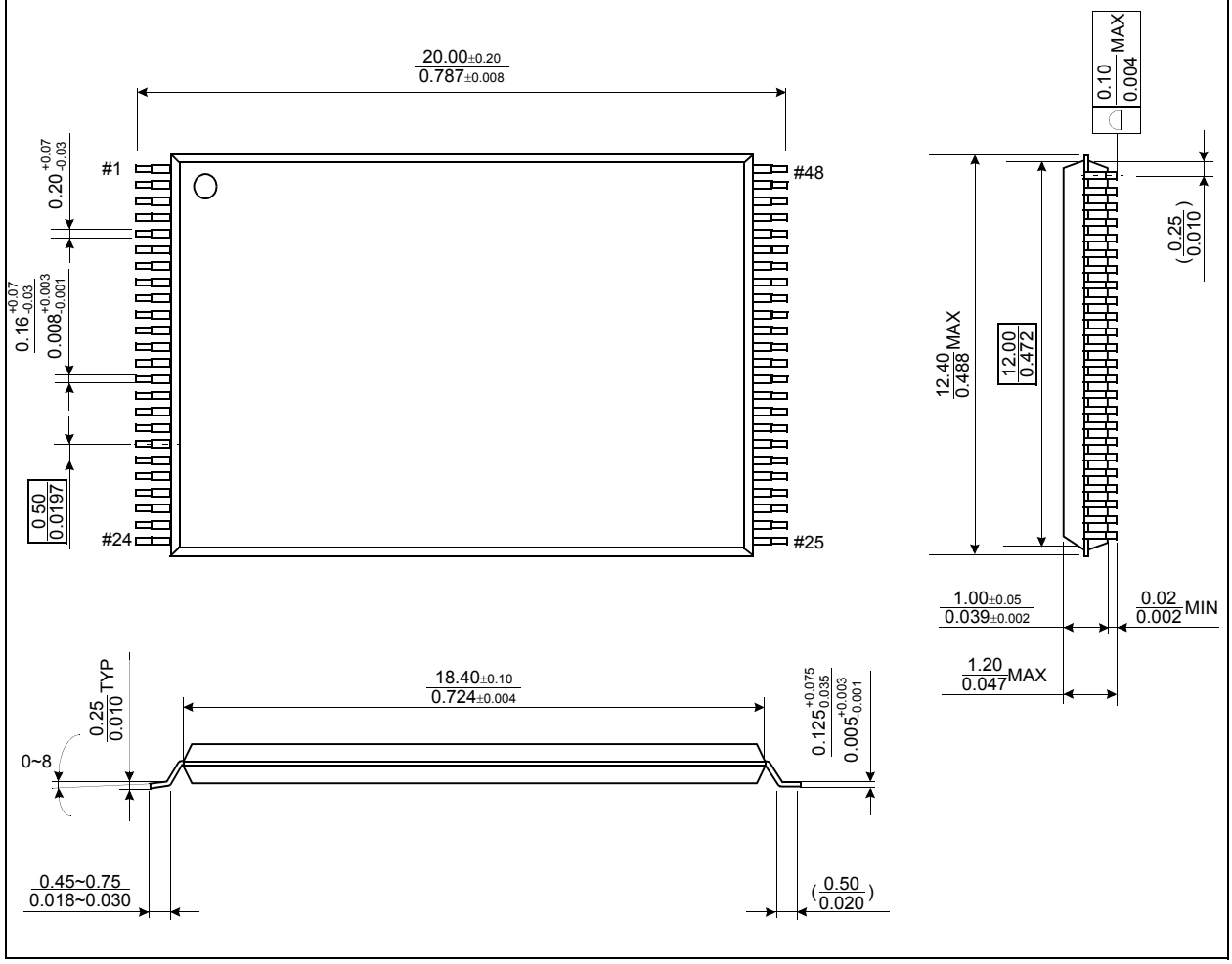
K9HCG08U1D-PCB0/PIB0



PACKAGE DIMENSIONS

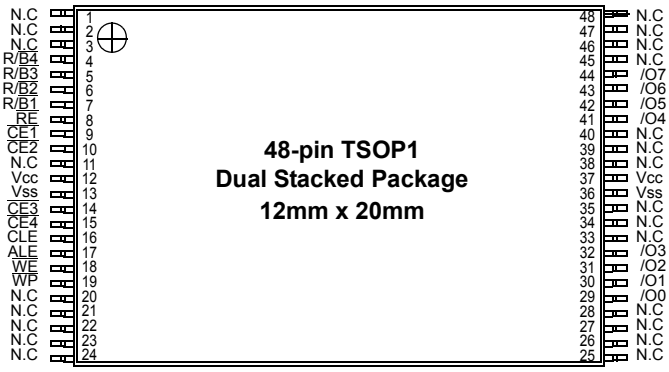
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48 - TSOP1 - 1220AF Unit :mm/Inch



PIN CONFIGURATION (TSOP1-DSP)

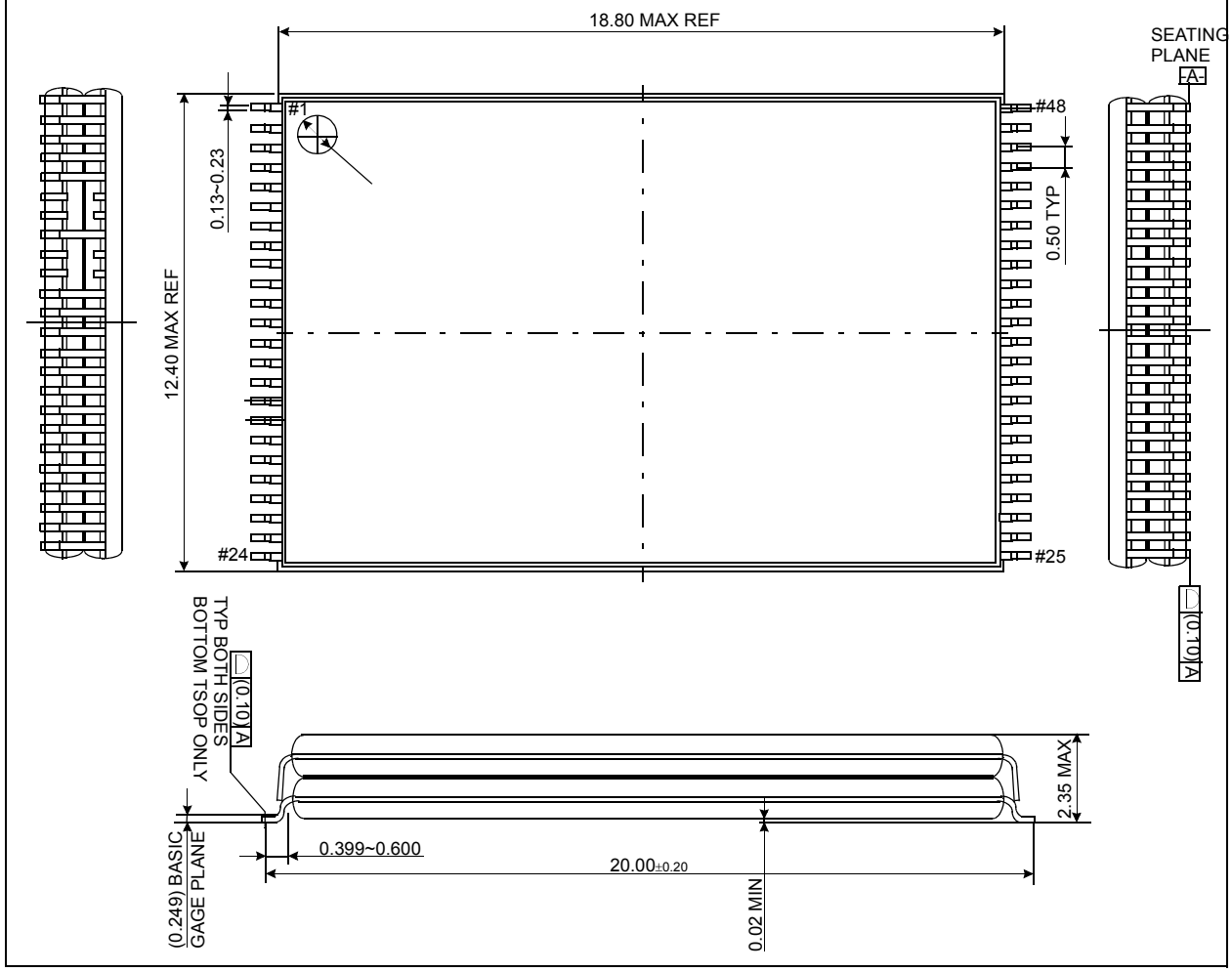
K9MDG08U5D-PCB0/PIB0



PACKAGE DIMENSIONS

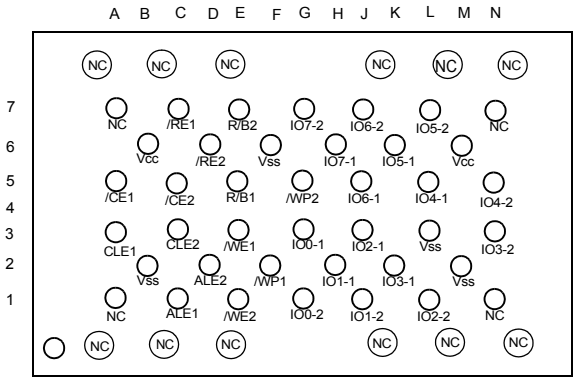
48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



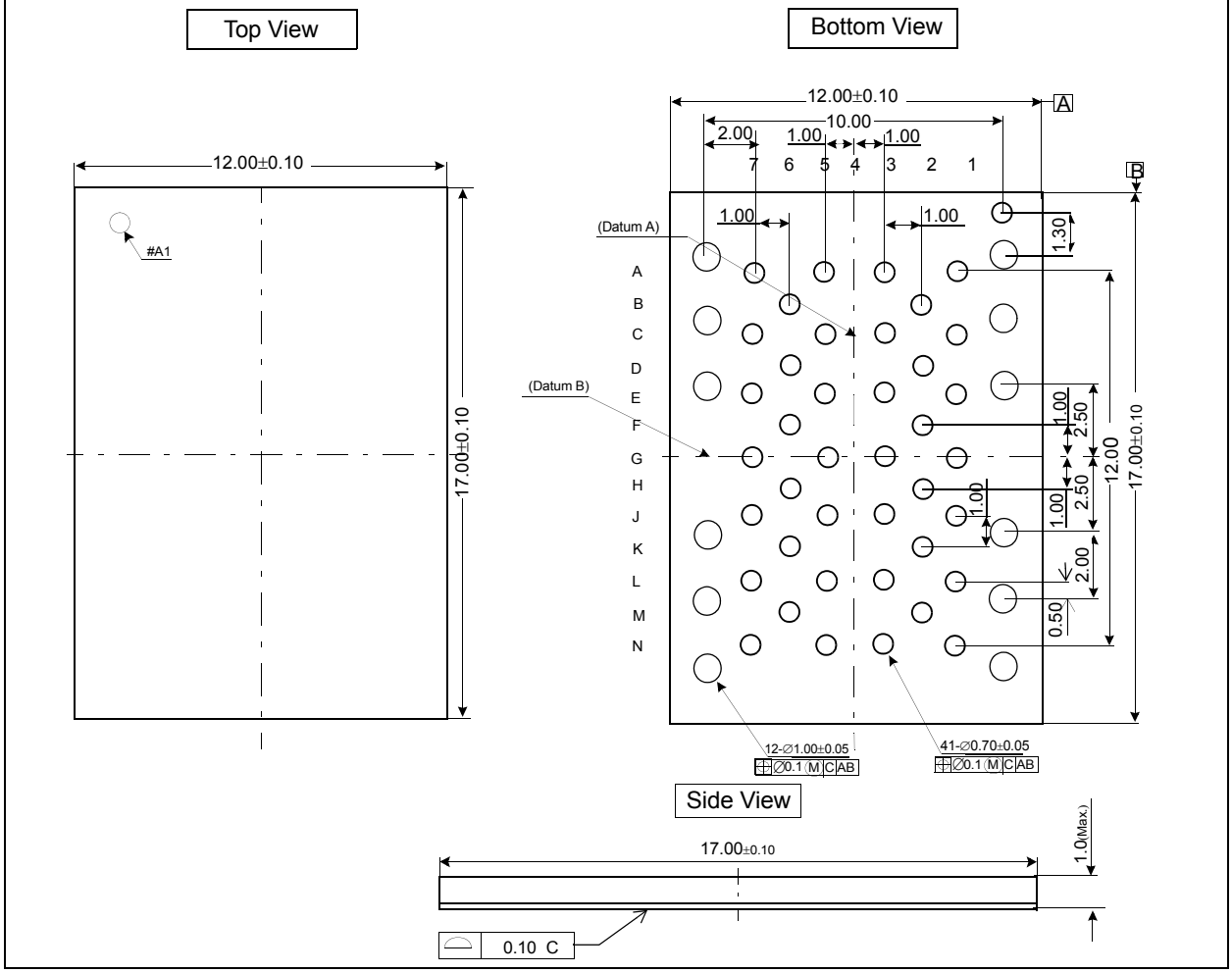
PIN CONFIGURATION (TLGA)

K9HCG08U1D - ICB0 / IIB0

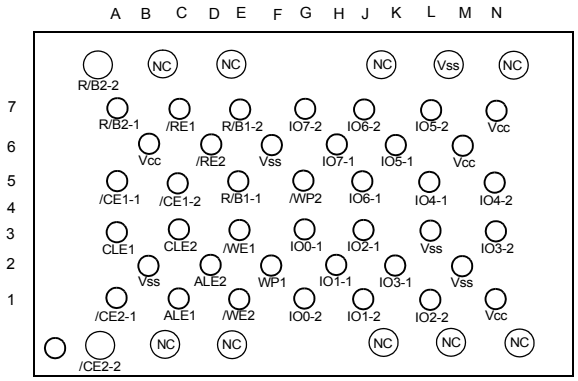


PACKAGE DIMENSIONS

52-TLGA (measured in millimeters)

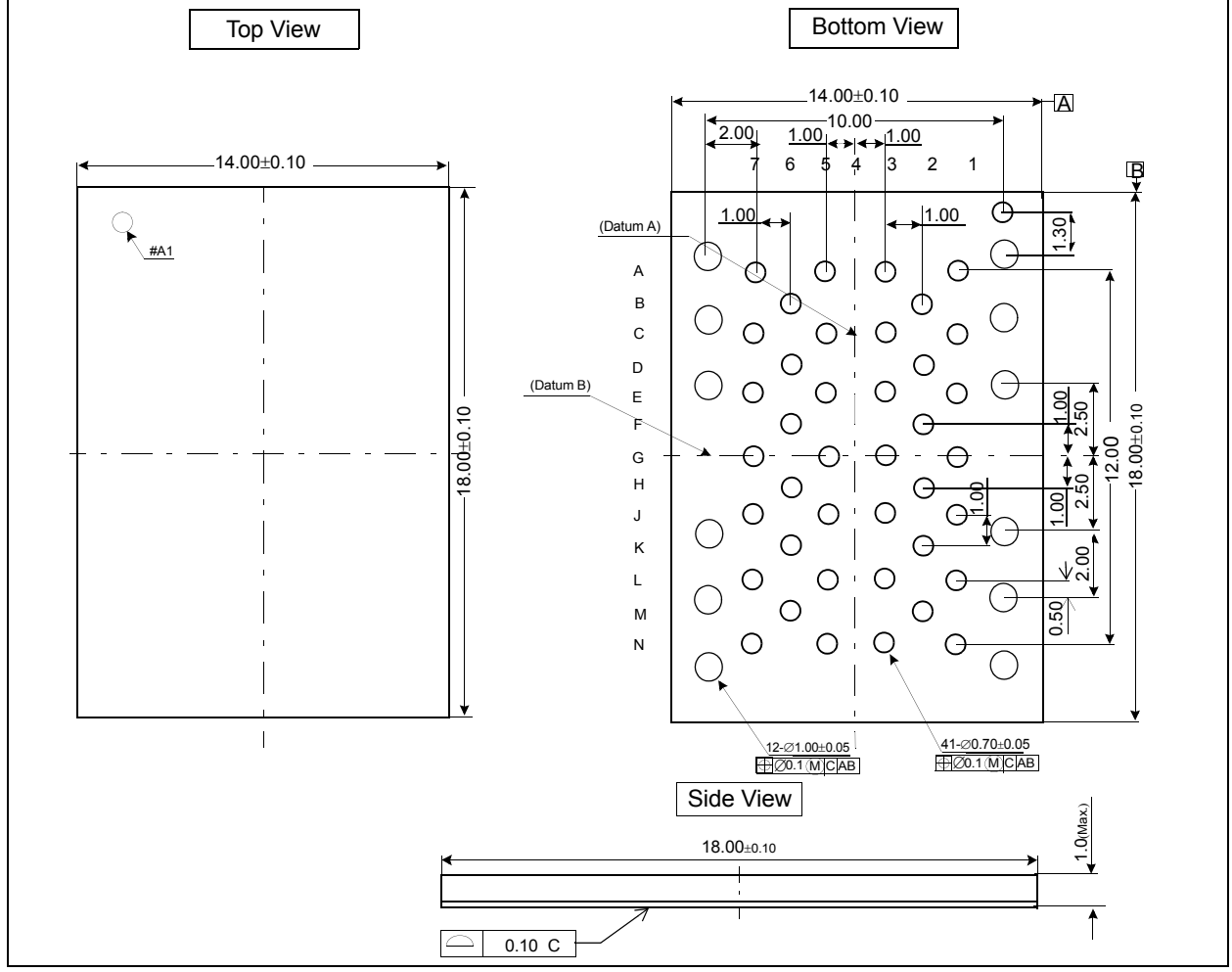


K9PDG08U5D-LCB0/LIB0



PACKAGE DIMENSIONS

52-TLGA (measured in millimeters)



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$ / $\overline{CE1}$	**CHIP ENABLE** The $\overline{CE}$ / $\overline{CE}$ 1 input is the device selection control. When the device is in the Busy state, $\overline{CE}$ / $\overline{CE1}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{CE}$ / $\overline{CE}$1 control during read operation , refer to 'Page Read' section of Device operation
$\overline{CE2}$	**CHIP ENABLE** The $\overline{CE}$2 input enables the second K9LBG08U0D
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$ / R/$\overline{B}$1	**READY/BUSY OUTPUT** The R/$\overline{B}$ / R/$\overline{B}$1 output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
R/$\overline{B}$2	**READY/BUSY OUTPUT** The R/$\overline{B}$2 output indicates the status of the second K9LBG08U0D.
V_{CC}	**POWER** V_{CC} is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

NOTE : Connect all V_{CC} and Vss pins of each device to common power supply outputs.
Do not leave V_{CC} or Vss disconnected.

There are two $\overline{CE}$ pins ($\overline{CE}$1 & $\overline{CE}$2) in the K9HCG08U1D, and four $\overline{CE}$ pins ($\overline{CE}$1 & $\overline{CE}$2 & $\overline{CE}$3 & $\overline{CE}$4) in the K9XDG08U5D.
There are two R/$\overline{B}$ pins (R/$\overline{B}$1 & R/$\overline{B}$2) in the K9HCG08U1D, and four R/$\overline{B}$ pins (R/$\overline{B}$1 & R/$\overline{B}$2 & R/$\overline{B}$3 & R/$\overline{B}$4) in the K9XDG08U5D.

Figure 1. K9LBG08U0D Functional Block Diagram

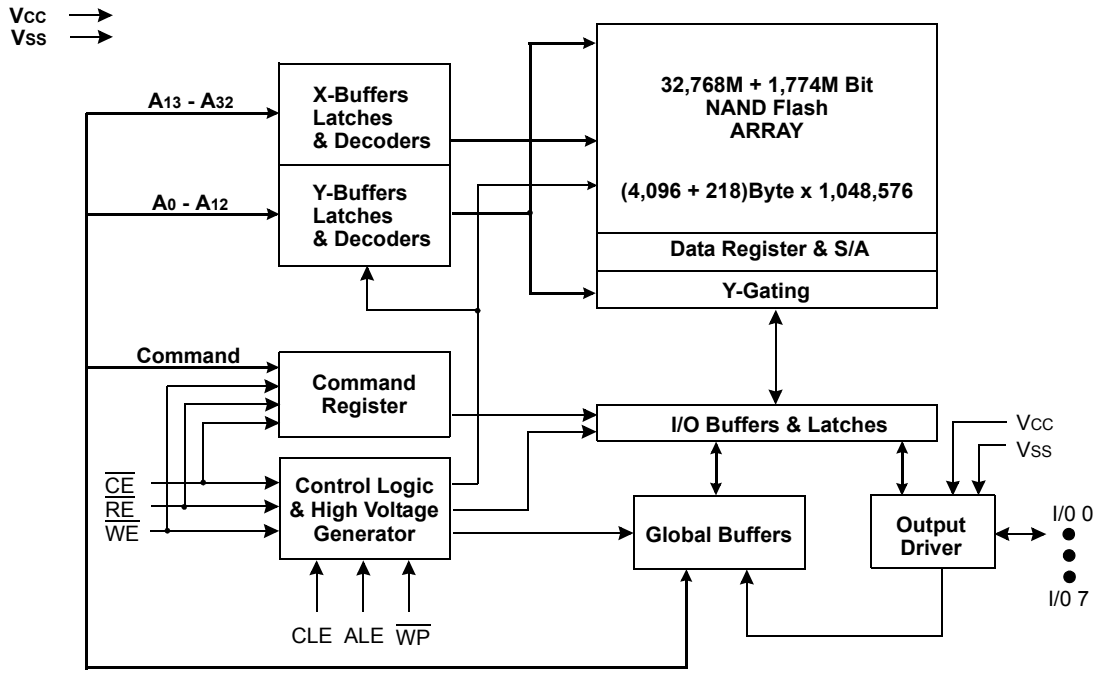
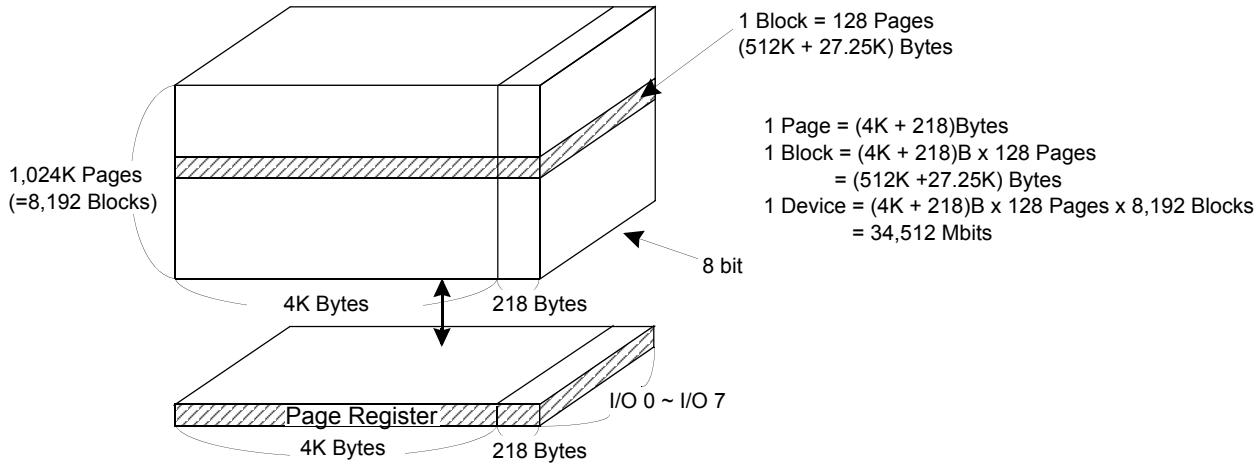


Figure 2. K9LBG08U0D Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	A12	*L	*L	*L	
3rd Cycle	A13	A14	A15	A16	A17	A18	A19	A20	Row Address; Page Address : A13 ~ A19 Plane Address : A20 Block Address : A21 ~ the last Address
4th Cycle	A21	A22	A23	A24	A25	A26	A27	A28	
5th Cycle	A29	A30	A31	A32	*L	*L	*L	*L	

NOTE : Column Address : Starting Address of the Register.

* L must be set to 'Low'.

* The device ignores any additional input of address cycles than required.

* Row Address consists of Page address (A13 ~ A19) & Plane address(A20) & Block address(A21 ~ the last Address)

Product Introduction

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc. require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9LBG08U0D.

Table 1. Command Sets

Function	1st Set	2nd Set	
Read	00h	30h	
Read for Copy Back	00h	35h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	
Page Program	80h	10h	
Cache Program	80h	15h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input(1)	85h	-	
Random Data Output(1)	05h	E0h	
Two-Plane Read (3)	60h----60h	30h	
Two-Plane Read for Copy-Back(3)	60h----60h	35h	
Two-Plane Random Data Output (1) (3)	00h----05h	E0h	
Two-Plane Cache Read(3)	60h----60h	33h	
Two-Plane Page Program(2)	80h----11h	81h----10h	
Two-Plane Copy-Back Program(2)	85h----11h	81h----10h	
Two-Plane Cache Program(2)	80h----11h	81h----15h	
Two-Plane Block Erase	60h----60h	D0h	
Read ID	90h	-	
Read Status	70h	-	O
Chip1 Status	F1h		O
Chip2 Status	F2h		O
Reset	FFh	-	O

NOTE : 1. Random Data Input/Output can be executed in a page.

2. Any command between 11h and 80h/81h/85h is prohibited except 70h/F1h/F2h and FFh.

3. Two-Plane Random Data out must be used after Two-Plane Read or Two-Plane Cache Read operation

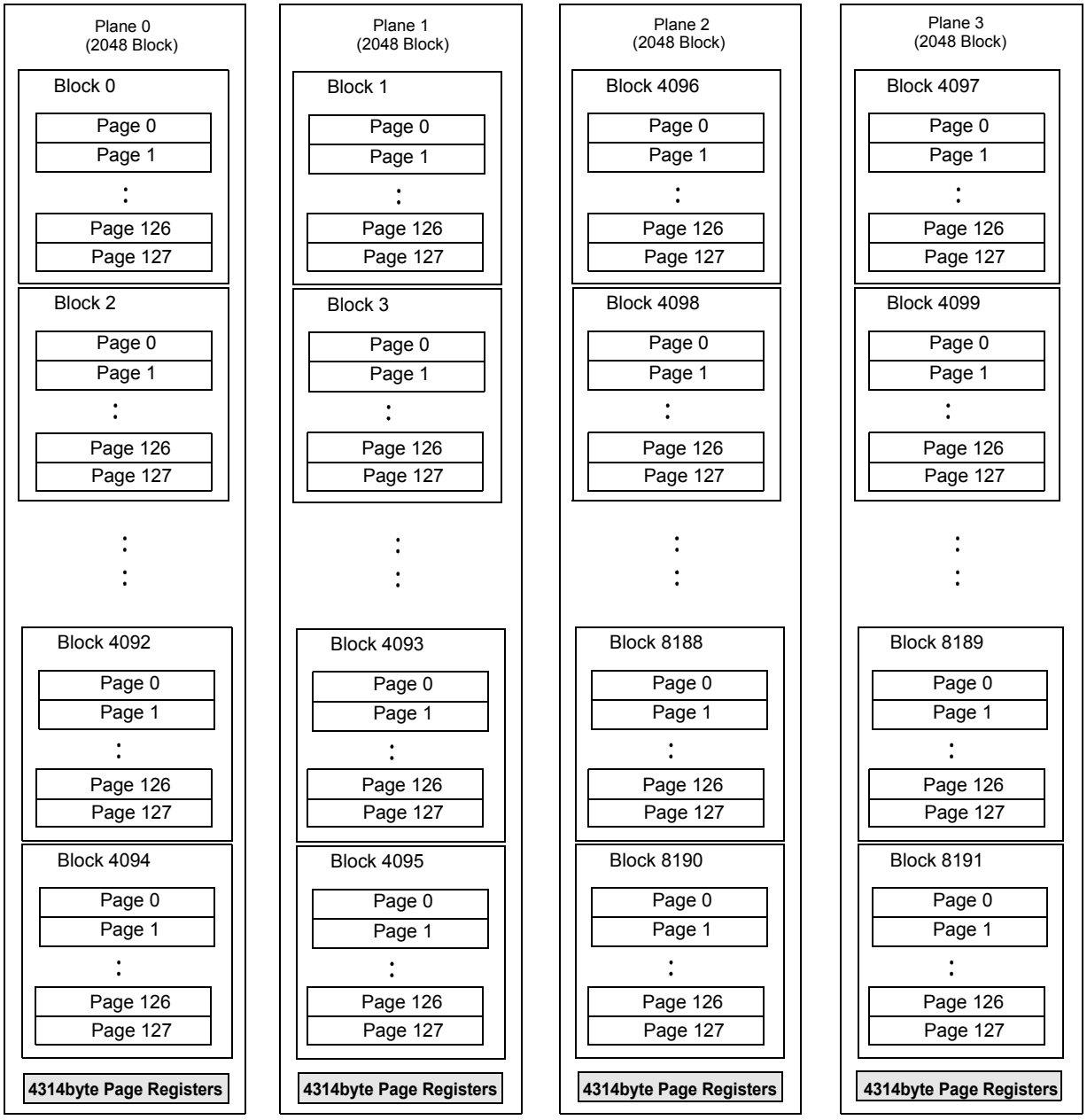
4. Interleave-operation between two chips is allowed.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

Memory Map

K9LBG08U0D is arranged in four 8Gb memory planes. Each plane contains 2,048 blocks and 4314 byte page registers. This allows it to perform simultaneous page program and block erase by selecting one page or block from each plane. The block address map is configured so that two-plane program/erase operations can be executed by dividing the memory array into plane 0~1 or plane 2~3 separately.

For example, two-plane program/erase operation into plane 0 and plane 2 is proh bited. That is to say, two-plane program/erase operation into plane 0 and plane 1 or into plane 2 and plane 3 is allowed.



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{CC}	-0.6 to + 4.6	V
		V_{IN}	-0.6 to + 4.6	
		$V_{I/O}$	-0.6 to Vcc+0.3 (<4.6V)	
Temperature Under Bias	K9XXG08UXD-XCB0	T_{BIAS}	-10 to +125	C
	K9XXG08UXD-XIB0		-40 to +125	
Storage Temperature	K9XXG08UXD-XCB0	T_{STG}	-65 to +150	C
	K9XXG08UXD-XIB0			
Short Circuit Current		Ios	5	mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9XXG08UXD-XCB0 :T_A=0 to 70 C, K9XXG08UXD-XIB0:T_A=-40 to 85 C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	tRC=30ns (K9XDG08U5D: 50ns) $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	15	35	mA
	Program	I_{CC2}	-				
	Erase	I_{CC3}	-				
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	20	100	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±20	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±20	
Input High Voltage		V_{IH}(1)	-	0.8 xVcc	-	Vcc +0.3	V
Input Low Voltage, All inputs		V_{IL}(1)	-	-0.3	-	0.2 xVcc	
Output High Voltage Level		V_{OH}	I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

NOTE : 1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC} +0.4V for durations of 20 ns or less.
2. Typical value is measured at Vcc=3.3V, T_A=25 C. Not 100% tested.
3. The typical value of he K9HCG08U1D's I_{SB2} is 40µA and the maximum value is 200µA.
4. The typical value of the K9XDG08U5D's I_{SB2} is 80µA and the maximum value is 400µA.
5. The maximum value of K9HCG08U1D-P's I_{LI} and I_{LO} is ±40µA.
6. The maximum value of K9PDG08U5D-L's I_{LI} and I_{LO} is ±40µA and K9MDG08U5D-P's I_{LI} and I_{LO} is ±80µA.

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
K9LBG08U0D	N_{VB}	7,992	-	8,192	Blocks
K9HCG08U1D		15,984	-	16,384	
K9XDG08U5D		31,968	-	32,768	

NOTE :
1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase opera ion. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment
3. The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

* : Each K9LBG08U0D chip in the K9HCG08U1D, K9XDG08U5D has maximum 200 invalid blocks.

AC TEST CONDITION

(K9XXG08UXD-XCB0 :T_A=0 to 70 C, K9XXG08UXD-XIB0:T_A=-40 to 85 C, K9XXG08UXD: Vcc=2.7V ~ 3.6V,unless otherwise noted)

Parameter	K9XXG08UXD
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=50pF (K9LBG08U0D-P, K9HCG08U1D-I)
	1 TTL GATE and CL=30pF (K9HCG08U1D-P, K9XDG08U5D-P/L)

CAPACITANCE(T_A=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	K9LBG08U0D		K9HCG08U1D		K9MDG08U5D		Unit
			Min	Max	Min	Max	Min	Max	
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	13	-	23	-	43	pF
	$C_{I/O(W)}$*		-	10	-	20	-	40	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	13	-	23	-	43	pF
	$C_{IN(W)}$*		-	10	-	20	-	40	pF

NOTE : 1. Capacitance is periodically sampled and not 100% tested.
2. $C_{I/O(W)}$ and $C_{IN(W)}$ are tested at wafer level.
3. K9HCG08U1D-IXB0's capacitance(I/O, Input) is 13pF and K9PDG08U5D-LXB0's capacitance(I/O, Input) is 23pF.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⎍	H	X	Read Mode	Command Input
L	H	L	⎍	H	X		Address Input(5clock)
H	L	L	⎍	H	H	Write Mode	Command Input
L	H	L	⎍	H	H		Address Input(5clock)
L	L	L	⎍	H	H	Data Input	
L	L	L	H	⎎	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	0.8	3	ms
Dummy Busy Time for Two-Plane Program	t_{DBSY}	-	0.5	1	μs
Dummy Busy Time for Cache Program	t_{CBSY}	-	-	3	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	1	cycle
Block Erase Time	t_{BERS}	-	1.5	10	ms

NOTE: 1.Typical program time is measured at Vcc=3.3V, TA=25 C. Not 100% tested.
2. Typical Program time is defined as the time within which more than 50% of the whole pages are programed at 3.3V Vcc and 25 C temperature.
3. Within a same block, program time(tPROG) of page group A is faster than that of page group B. Typical tPROG is the average program time of the page group A and B(Table 5).
Page Group A: Page 0, 1, 2, 3, 6, 7, 10, 11, ... , 110, 111, 114, 115, 118, 119, 122, 123
Page Group B: Page 4, 5, 8, 9, 12, 13, 16, 17, ... , 116, 117, 120, 121, 124, 125, 126, 127
4. t_{CBSY} depends on the timing between internal programming time and data in time.

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min		Max		Unit
		K9LBG08U0D K9HCG08U1D	K9XDG08U5D	K9LBG08U0D K9HCG08U1D	K9XDG08U5D	
CLE Setup Time	t_{CLS}(1)	15	25	-	-	ns
CLE Hold Time	t_{CLH}	5	10	-	-	ns
$\overline{CE}$ Setup Time	t_{CS}(1)	20	35	-	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	10	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	15	25	-	-	ns
ALE Setup Time	t_{ALS}(1)	15	25	-	-	ns
ALE Hold Time	t_{ALH}	5	10	-	-	ns
Data Setup Time	t_{DS}(1)	15	20	-	-	ns
Data Hold Time	t_{DH}	5	10	-	-	ns
Write Cycle Time	t_{WC}	30	45	-	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	10	15	-	-	ns
Address to Data Loading Time	t_{ADL}(2)	100	100	-	-	ns

NOTES : 1. The transition of he corresponding control pins must occur only once while $\overline{WE}$ is held low
2. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle

AC Characteristics for Operation

Parameter	Symbol	Min		Max		Unit
		K9LBG08U0D K9HCG08U1D	K9XDG08U5D	K9LBG08U0D K9HCG08U1D	K9XDG08U5D	
Data Transfer from Cell to Register	t_R	-		60	60	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	10	-		ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	10	-		ns
Ready to $\overline{RE}$ Low	t_{RR}	20	20	-		ns
$\overline{RE}$ Pulse Width	t_{RP}	15	25	-		ns
$\overline{WE}$ High to Busy	t_{WB}	-	-	100	100	ns
$\overline{WP}$ High to $\overline{WE}$ Low	t_{WW}	100	100			ns
Read Cycle Time	t_{RC}	30	50	-		ns
$\overline{RE}$ Access Time	t_{REA}	-	-	20	30	ns
$\overline{CE}$ Access Time	t_{CEA}	-	-	25	45	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	-	100	100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	-	30	30	ns
$\overline{CE}$ High to ALE or CLE Don't Care	t_{CSD}	0	0	-		ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15	15	-		ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5	-	-		ns
$\overline{RE}$ High Hold Time	t_{REH}	10	15	-		ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	0	-		ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	100	-		ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	60	-		ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	-	5/10/500(1)	5/10/500(1)	µs
Cache Busy in Read Cache (following 31h and 3Fh)	t_{DCBSYR}	-	-	65	65	µs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5µs.

NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that the last page of every initial invalid block has non-FFh data at the column address of 4,096.The initial invalid block information is also erasable in most cases, and it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.

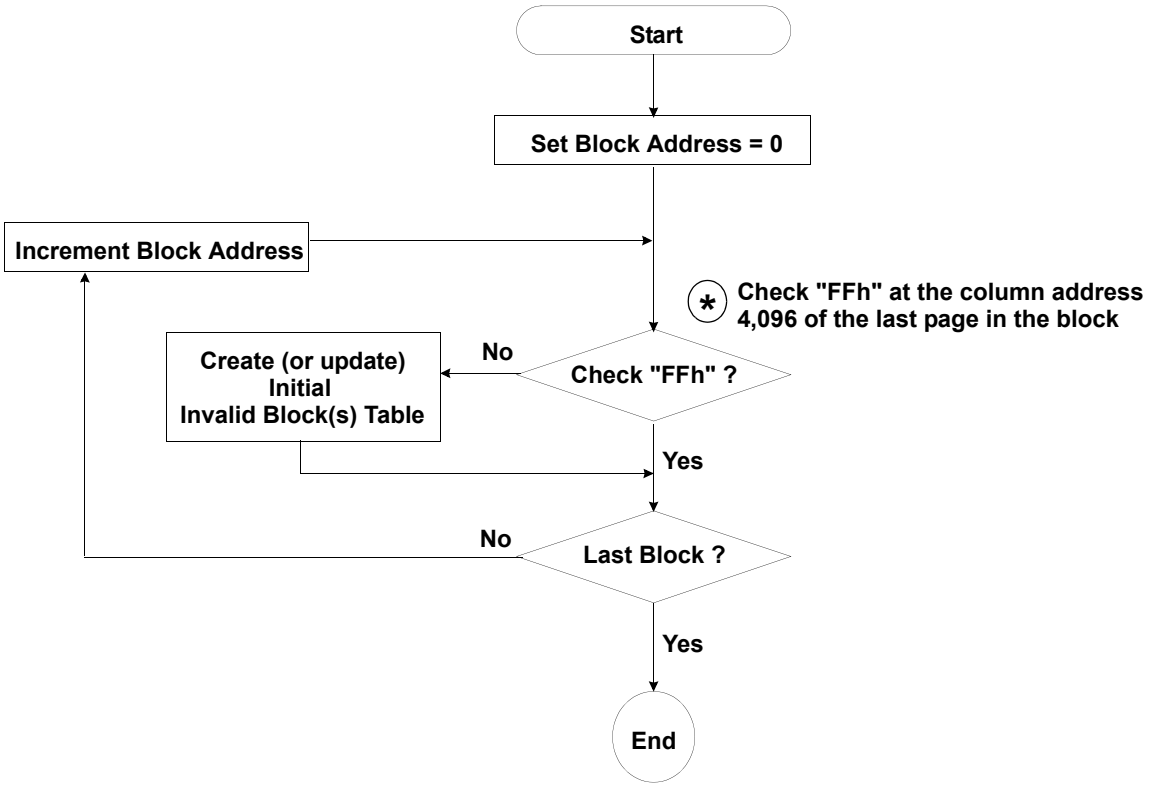


Figure 3. Flow chart to create initial invalid block table.

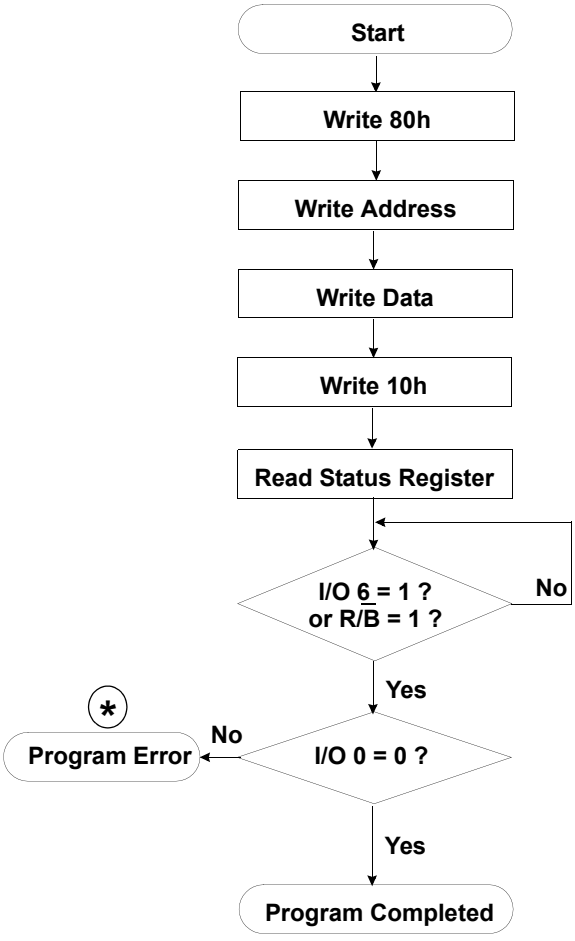
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Up to Eight Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> RS Code or BCH Code etc.
Example) 8bit correction / 512-byte

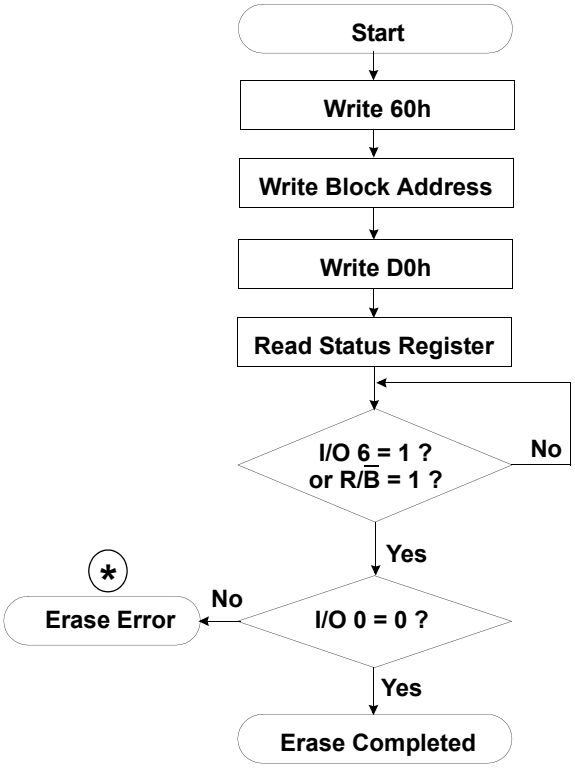
Program Flow Chart



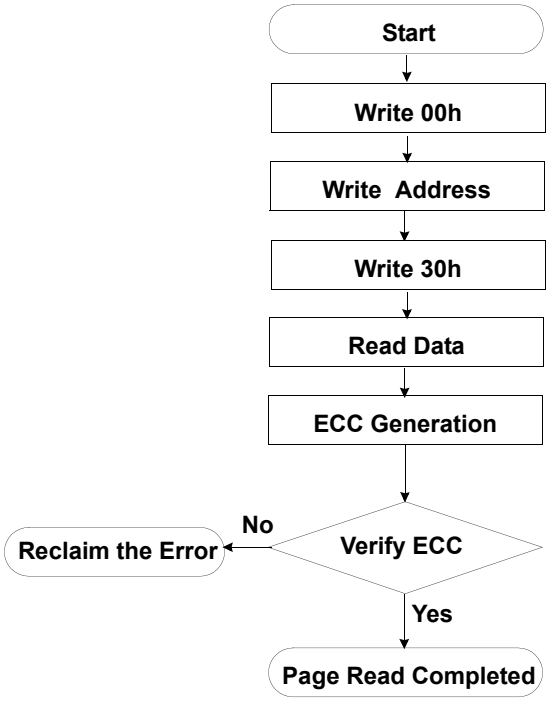
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes (Continued)

Erase Flow Chart

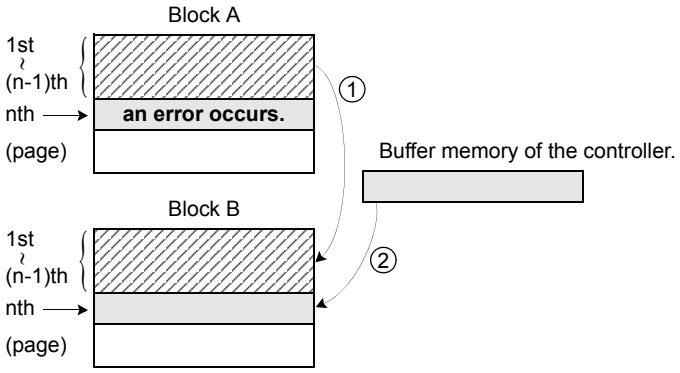


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program Block 'A' by creating an 'invalid block' table or other appropriate scheme.

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