



**NOVOSENSE**  
纳芯微电子

**NSI6601M-Q1**

# Single-Channel Isolated Gate Driver

Datasheet (EN) 1.1

## Product Overview

The NSI6601M is a family of high reliability single-channel isolated gate driver ICs which can be designed to drive IGBTs, power MOSFETs and SiC MOSFETs in many applications. That provide minimum peak output currents up to 5A and an integrated active Miller Clamp circuit with the same current rating .

The NSI6601M provides 3000V<sub>rms</sub> isolation in SOP8 package, and 5700V<sub>rms</sub> isolation in SOW8 package. System robustness is supported by 150kV/ $\mu$ s minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 28V, while the input-side accepts from 3V to 17V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

Because of high driving current ability, excellent robustness, wide supply voltage range and fast signal propagation, NSI6601M is suitable for high reliability, power density and efficient switching power system.

## Key Features

- Isolated single-channel driver
- Active Miller Clamp
- Input side supply voltage: 3V to 17V
- Driver side supply voltage: up to 28V with 9V, and 12V UVLO options
- 5A peak source and sink output current
- Minimum CMTI:  $\pm 150\text{kV}/\mu\text{s}$
- 80ns typical propagation delay
- RoHS & REACH Compliance
- Operation temperature:  $-40^\circ\text{C} \sim 125^\circ\text{C}$
- AEC-Q100 Grade1

## Safety Regulatory Approvals

- UL recognition:
  - SOW8: 5700V<sub>rms</sub> for 1 minute per UL1577

- SOP8: 3000V<sub>rms</sub> for 1 minute per UL1577

- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

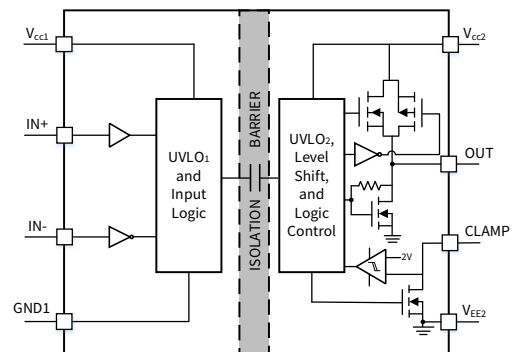
## Applications

- Isolated DC/DC and AC/DC Power Supplies
- High Voltage PFC
- Solar Inverters
- Motor Drives and EV Charging
- UPS and Battery Chargers

## Device Information

| Part Number      | UVLO Level | Package | Body Size      |
|------------------|------------|---------|----------------|
| NSI6601MB-Q1SWVR | 9V         | SOW8    | 7.5×5.85×2.3mm |
| NSI6601MC-Q1SWVR | 12V        | SOW8    | 7.5×5.85×2.3mm |
| NSI6601MB-Q1SPR  | 9V         | SOP8    | 4.9×3.9×1.35mm |
| NSI6601MC-Q1SPR  | 12V        | SOP8    | 4.9×3.9×1.35mm |
| NSI6601WC-Q1SWVR | 12V        | SOW8    | 7.5×5.85×2.3mm |

## Block Diagram



NSI6601M/W Diagram

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### 1. Pin Configuration and Function

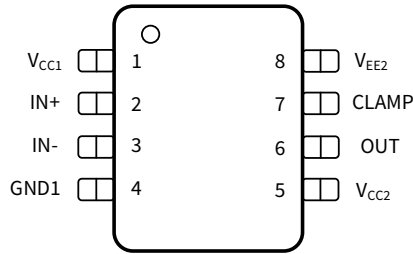


Figure 1.1 NSI6601MC/MB (Top View)

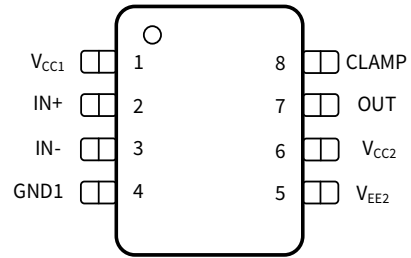


Figure 1.2 NSI6601WC (Top View)

Table 1.1 NSI6601M/W Pin Configuration and Description

| PIN NAME         | PIN NO.     |           | TYPE | FUNCTION                                                        |
|------------------|-------------|-----------|------|-----------------------------------------------------------------|
|                  | NSI6601MC/B | NSI6601WC |      |                                                                 |
| V <sub>CC1</sub> | 1           | 1         | P    | Input-side supply rail                                          |
| IN+              | 2           | 2         | I    | Non-inverted input signal with internal pull down to GND1       |
| IN-              | 3           | 3         | I    | Inverted input signal with internal pull up to V <sub>CC1</sub> |
| GND1             | 4           | 4         | G    | Input-side ground reference                                     |
| V <sub>CC2</sub> | 5           | 6         | P    | Positive output supply rail                                     |
| OUT              | 6           | 7         | O    | Gate Driver Output                                              |
| CLAMP            | 7           | 8         | I    | Active Miller-Clamp input                                       |
| V <sub>EE2</sub> | 8           | 5         | G    | Driver-side ground reference                                    |

## 2. Absolute Maximum Ratings

| Parameters                 | Symbol                                   | Min           | Max           | Unit |
|----------------------------|------------------------------------------|---------------|---------------|------|
| Input Side Supply Voltage  | $V_{CC1-GND1}$                           | -0.3          | 18            | V    |
| Input Signal Voltage       | $V_{IN+-GND1}, V_{IN-GND1}$              | -0.3          | 18            | V    |
| Driver Side Supply Voltage | $V_{CC2-V_{EE2}}$                        | -0.3          | 35            | V    |
| Output Signal Voltage      | $V_{OUT} - V_{EE2}, V_{CLAMP} - V_{EE2}$ | $V_{EE2}-0.3$ | $V_{CC2}+0.3$ | V    |
| Junction Temperature       | $T_J$                                    | -40           | 150           | °C   |
| Storage Temperature        | $T_{stg}$                                | -65           | 150           | °C   |

## 3. ESD Ratings

| Ratings                 |                                                                 | Value      | Unit |
|-------------------------|-----------------------------------------------------------------|------------|------|
| Electrostatic discharge | Human body model (HBM), per AEC-Q100-002-RevD<br>● All pins     | $\pm 4000$ | V    |
|                         | Charged device model (CDM), per AEC-Q100-011-RevB<br>● All pins | $\pm 1500$ | V    |

## 4. Recommended Operating Conditions

| Parameters                 | Symbol                           | Min  | Max | Unit |
|----------------------------|----------------------------------|------|-----|------|
| Input Side Supply Voltage  | $V_{CC1-GND1}$                   | 3    | 17  | V    |
| Input Signal Voltage       | $V_{IN+-GND1}, V_{IN-GND1}$      | -0.3 | 17  | V    |
| Driver Side Supply Voltage | $V_{CC2-V_{EE2}}$<br>(NSI6601MB) | 10   | 28  | V    |
|                            | $V_{CC2-V_{EE2}}$<br>(NSI6601MC) | 13   | 28  |      |
| Ambient Temperature        | $T_A$                            | -40  | 125 | °C   |

## 5. Thermal Information

| Parameters                                                | Symbol         | SOW8 | SOP8 | Unit |
|-----------------------------------------------------------|----------------|------|------|------|
| Junction-to-ambient thermal resistance <sup>(1)</sup>     | $R_{JA}$       | 110  | 120  | °C/W |
| Junction-to-case(top) thermal resistance <sup>(2)</sup>   | $R_{JC (top)}$ | 45   | 60   | °C/W |
| Junction-to-top characterization parameter <sup>(3)</sup> | $\Psi_{JT}$    | 18   | 38   | °C/W |

|                                                            |             |    |    |      |
|------------------------------------------------------------|-------------|----|----|------|
| Junction-to-board characterization parameter <sup>3)</sup> | $\Psi_{JB}$ | 47 | 59 | °C/W |
|------------------------------------------------------------|-------------|----|----|------|

1)Standard JESD51-3 Low Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.

2)Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.

3)Obtained by Simulating in an environment described in JESD51-2a.

## 6. Specifications

### 6.1. DC Electrical Characteristics

$V_{CC1}=5V$ , with a bypass capacitor of  $1\mu F$  from  $V_{CC1}$  to GND1, and  $V_{CC2}=15V$  with a capacitor of  $10\mu F$  from  $V_{CC2}$  to  $V_{EE2}$ ,  $T_a=-40^{\circ}C$  to  $125^{\circ}C$ , Unless otherwise noted, Typical values are at  $T_a=25^{\circ}C$ .

| Parameter                                                                      | Symbol               | Min                  | Typ                   | Max                  | Unit    | Condition                                   |
|--------------------------------------------------------------------------------|----------------------|----------------------|-----------------------|----------------------|---------|---------------------------------------------|
| <b>Supply Currents</b>                                                         |                      |                      |                       |                      |         |                                             |
| Input Supply Quiescent Current                                                 | $I_{CC1}$            |                      | 0.9                   | 1.5                  | mA      | $V_{IN+}=GND1, V_{IN-}=5V$                  |
| Output Supply Quiescent Current                                                | $I_{CC2}$            |                      | 1.6                   | 3                    | mA      | $V_{IN+}=GND1, V_{IN-}=GND1$                |
| <b>Input Side Supply UVLO Threshold</b>                                        |                      |                      |                       |                      |         |                                             |
| VCC1 UVLO Rising Threshold                                                     | $V_{CC1\_ON}$        |                      | 2.9                   | 3.1                  | V       |                                             |
| VCC1 UVLO Falling Threshold                                                    | $V_{CC1\_OFF}$       | 2.55                 | 2.78                  |                      | V       |                                             |
| VCC1 UVLO Hysteresis                                                           | $V_{CC1\_HYS}$       |                      | 0.12                  |                      | V       |                                             |
| <b>Driver Side Supply UVLO Threshold (NSI6601MB 9V UVLO Level)</b>             |                      |                      |                       |                      |         |                                             |
| VCC2 UVLO Rising Threshold                                                     | $V_{CC2\_ON}$        |                      | 9.2                   | 10                   | V       |                                             |
| VCC2 UVLO Falling Threshold                                                    | $V_{CC2\_OFF}$       | 8                    | 8.5                   |                      | V       |                                             |
| VCC2 UVLO Hysteresis                                                           | $V_{CC2\_HYS}$       |                      | 0.7                   |                      | V       |                                             |
| <b>Driver Side Supply UVLO Threshold (NSI6601MC, NSI6601WC 12V UVLO Level)</b> |                      |                      |                       |                      |         |                                             |
| VCC UVLO Rising Threshold                                                      | $V_{CC2\_ON}$        |                      | 12.2                  | 13                   | V       |                                             |
| VCC UVLO Falling Threshold                                                     | $V_{CC2\_OFF}$       | 10.3                 | 11.2                  |                      | V       |                                             |
| VCC UVLO Hysteresis                                                            | $V_{CC2\_HYS}$       |                      | 1                     |                      | V       |                                             |
| <b>Input Pin Characteristics</b>                                               |                      |                      |                       |                      |         |                                             |
| Logic High Input Threshold (IN+, IN-)                                          | $V_{IN+H}, V_{IN-H}$ |                      | $0.55 \times V_{CC1}$ | $0.7 \times V_{CC1}$ | V       |                                             |
| Logic Low Input Threshold (IN+, IN-)                                           | $V_{IN+L}, V_{IN-L}$ | $0.3 \times V_{CC1}$ | $0.45 \times V_{CC1}$ |                      | V       |                                             |
| Input Hysteresis Voltage (IN+, IN-)                                            | $V_{IN\_hys}$        |                      | $0.1 \times V_{CC1}$  |                      | V       |                                             |
| IN+ Input Current                                                              | $I_{IN+}$            |                      | 55                    | 70                   | $\mu A$ | $V_{IN+}=V_{CC1}$                           |
| IN- Input Current                                                              | $I_{IN-}$            | -70                  | -55                   |                      | $\mu A$ | $V_{IN-}=GND1$                              |
| <b>Output Pin Characteristics</b>                                              |                      |                      |                       |                      |         |                                             |
| High Level Output Voltage ( $V_{CC2}-V_{OUT}$ )                                | $V_{OH}$             |                      | 140                   | 320                  | mV      | $I_{OUT}=-50mA, V_{IN+}=High, V_{IN-}=Low$  |
| Low Level Output Voltage (OUT)                                                 | $V_{OL}$             |                      | 30                    | 70                   | mV      | $I_{CLAMP}=50mA, V_{IN+}=Low, V_{IN-}=High$ |

| Parameter                                                         | Symbol           | Min | Typ  | Max | Unit     | Condition                                                             |
|-------------------------------------------------------------------|------------------|-----|------|-----|----------|-----------------------------------------------------------------------|
| Output Pull-up Resistance                                         | $R_{OH}$         |     | 2.8  |     | $\Omega$ | $V_{OH}/50mA$                                                         |
| Output Pull-down Resistance                                       | $R_{OL}$         |     | 0.6  |     | $\Omega$ | $V_{OL}/50mA$                                                         |
| Peak Source Current                                               | $I_{OH}$         |     | 5    |     | A        | $V_{IN+}=High, V_{IN-}=Low, pulse\ width < 10\mu s$                   |
| Peak Sink Current                                                 | $I_{OL}$         |     | 5    |     | A        | $V_{IN+}=Low, V_{IN-}=High, pulse\ width < 10\mu s$                   |
| <b>Active Miller Clamp</b>                                        |                  |     |      |     |          |                                                                       |
| Clamp Low Level Voltage                                           | $V_{LL\_CLAMP}$  |     | 11.2 | 24  | mV       | $I_{CLAMP}=20mA, V_{IN-}=V_{IN+}=Low$                                 |
| Clamp Threshold Voltage                                           | $V_{CLAMP\_TH}$  |     | 2.1  | 2.3 | V        | Referred to $V_{EE2}$                                                 |
| Low Level Clamp Current (Peak)                                    | $I_{LL\_CLAMP}$  |     | 5    |     | A        | $V_{IN-}=V_{IN+}=Low, V_{CLAMP}=2V\ pulse$                            |
| Clamp Delay Falling                                               | $T_{CD}$         |     | 46   |     | ns       |                                                                       |
| <b>Short Circuit Clamping</b>                                     |                  |     |      |     |          |                                                                       |
| Clamping Voltage (OUT)<br>( $V_{OUT} - V_{CC2}$ )                 | $V_{CLP\_OUT}$   |     | 1    | 1.6 | V        | $I_{OUT}=500mA\ with\ t_{pulse}=10\mu s, V_{IN+}=High, V_{IN-}=Low$   |
| Clamping Voltage (CLAMP)<br>( $V_{CLAMP}-V_{CC2}$ )               | $V_{CLP\_CLAMP}$ |     | 1.2  | 1.5 | V        | $I_{CLAMP}=500mA\ with\ t_{pulse}=10\mu s, V_{IN+}=High, V_{IN-}=Low$ |
|                                                                   |                  |     | 0.7  | 1   | V        | $I_{CLAMP}=20mA, V_{IN+}=High, V_{IN-}=Low$                           |
| <b>Active Pull-down</b>                                           |                  |     |      |     |          |                                                                       |
| Active Pull-down Voltage on CLAMP<br>( $V_{CLAMP}$ to $V_{EE2}$ ) | $V_{ACTPD}$      |     | 2.3  |     | V        | $I_{CLAMP}=0.1 * I_{CLAMP(typ)}, V_{CC1}=V_{CC2}=Open$                |

## 6.2. Switching Characteristics

Switching characteristics are measured by using  $V_{CC1}=5V$ ,  $1\mu F$  capacitor from  $V_{CC1}$  to GND1, and  $V_{CC2}=15V$  with  $10\mu F$  bypass capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $T_a=-40^{\circ}C$  to  $125^{\circ}C$ , Unless otherwise noted, Typical values are at  $T_a=25^{\circ}C$ .

| <i>Parameter</i>                             | <i>Symbol</i> | <i>Min</i> | <i>Typ</i> | <i>Max</i> | <i>Unit</i> | <i>Condition</i>   |
|----------------------------------------------|---------------|------------|------------|------------|-------------|--------------------|
| Minimum Pulse Width                          | $t_{PWmin}$   |            | 30         | 60         | ns          |                    |
| Propagation Delay                            | $t_{pLH}$     | 50         | 80         | 110        | ns          | $C_{LOAD}=100pF$   |
| Propagation Delay                            | $t_{pHL}$     | 50         | 80         | 110        | ns          | $C_{LOAD}=100pF$   |
| Pulse Width Distortion $ t_{pLH}-t_{pHL} $   | $t_{PWD}$     |            | 2          | 25         | ns          | $C_{LOAD}=100pF$   |
| Output Rise Time (20% to 80%)                | $t_R$         |            | 9          | 20         | ns          | $C_{LOAD}=1nF$     |
| Output Fall Time (80% to 20%)                | $t_F$         |            | 8          | 18         | ns          | $C_{LOAD}=1nF$     |
| Common Mode Transient Immunity <sup>1)</sup> | CMTI          | 150        |            |            | kV/ $\mu s$ | verified by design |

### 6.3. Typical Performance Characteristics

Typical characteristics are measured by using  $V_{CC1}=5V$ ,  $1\mu F$  capacitor from  $V_{CC1}$  to  $GND1$ , and  $V_{CC2}=15V$  with  $10\mu F$  bypass capacitor from  $V_{CC2}$  to  $V_{EE2}$   $T_J = -40^{\circ}C$  to  $125^{\circ}C$  (unless otherwise noted).

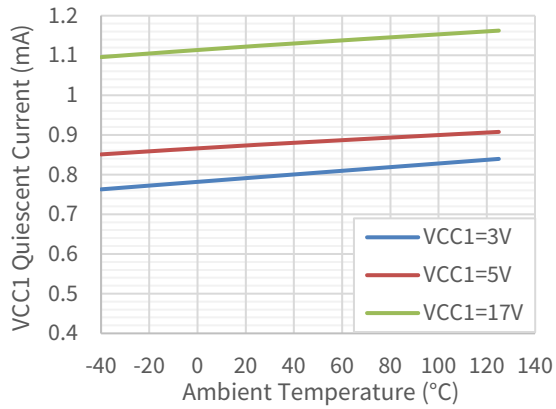


Figure 6.1 Input supply quiescent current Vs Temperature

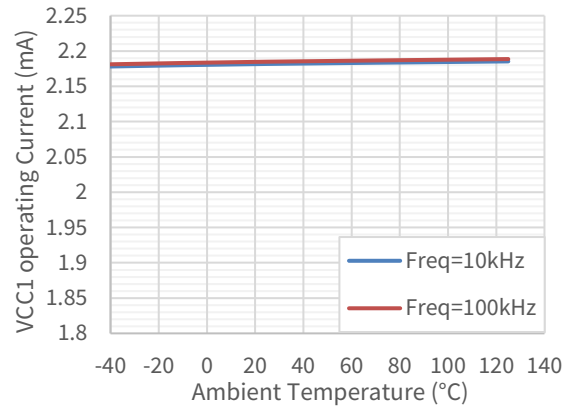


Figure 6.2 Input supply operating current Vs Temperature

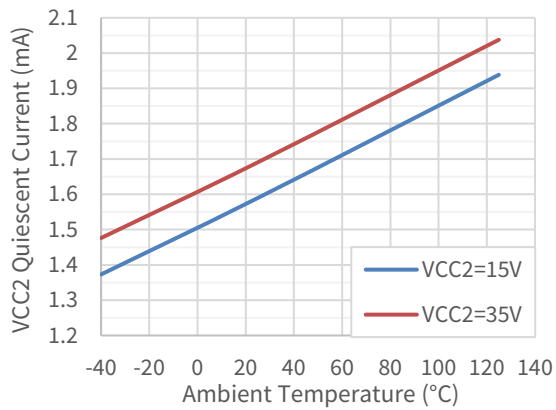


Figure 6.3 Output supply quiescent current Vs Temperature

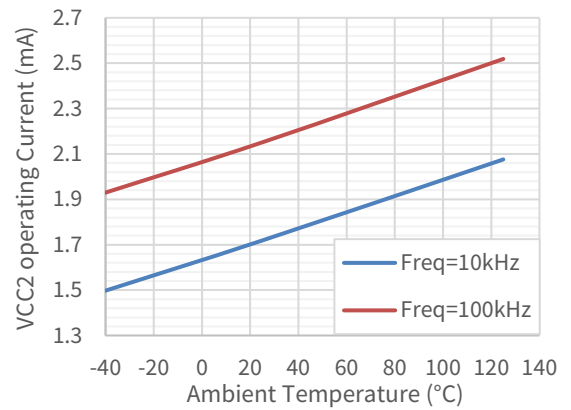


Figure 6.4 Output supply operating current Vs Temperature

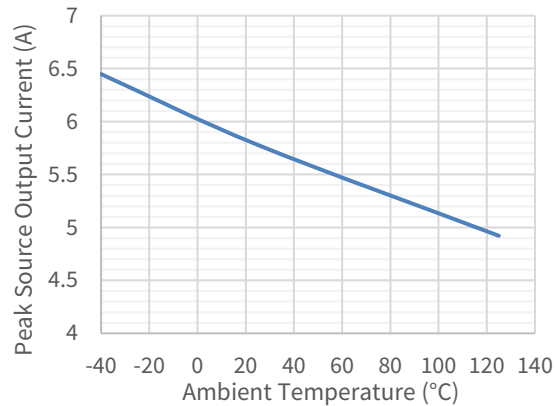


Figure 6.5 Peak source output current Vs Temperature

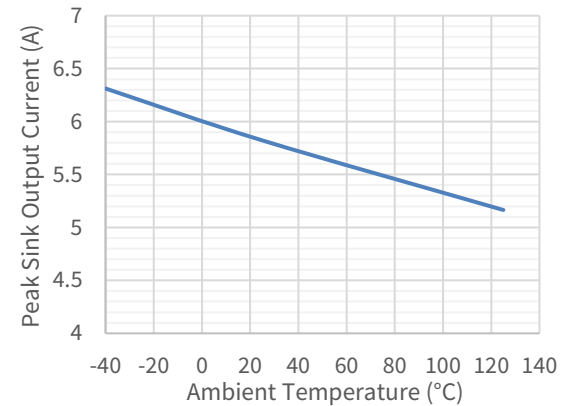


Figure 6.6 Peak sink output current Vs Temperature

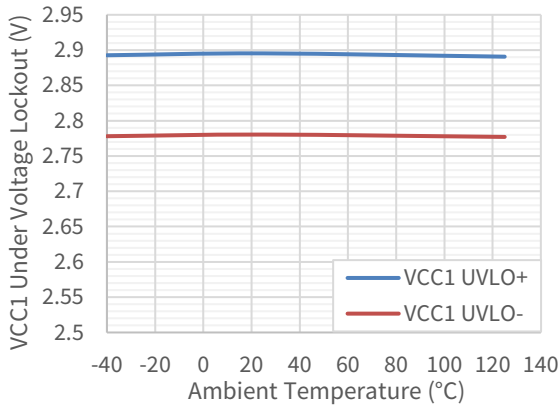


Figure 6.7 VCC1 UVLO Threshold Vs Temperature

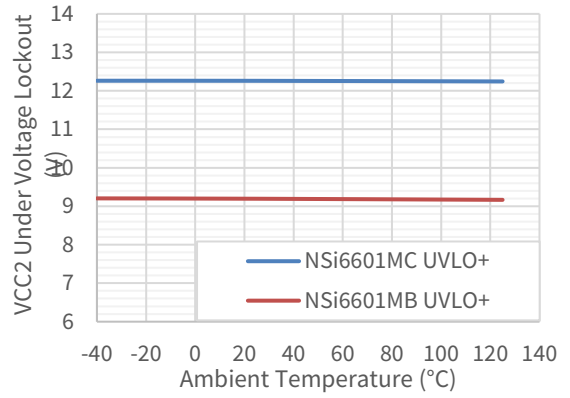


Figure 6.8 VCC2 UVLO\_ON Vs Temperature

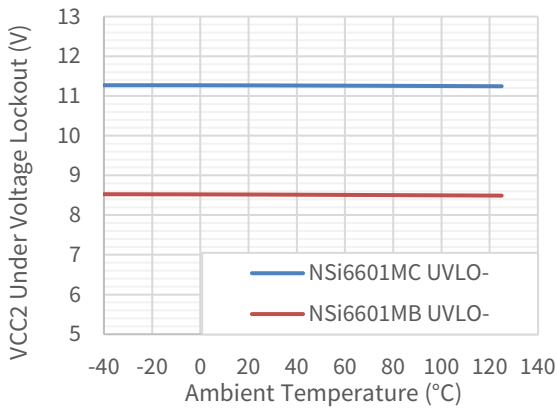


Figure 6.9 VCC2 UVLO\_OFF Vs Temperature

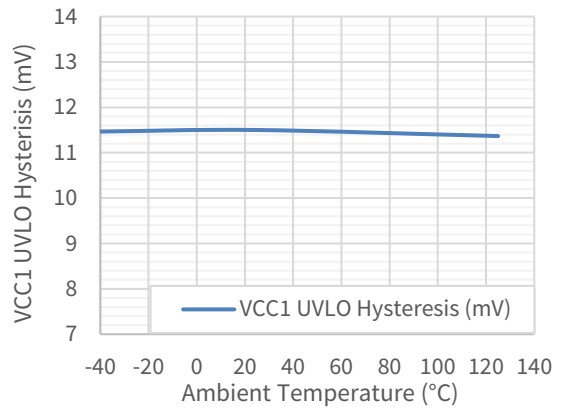


Figure 6.10 VCC1 UVLO Hysteresis Vs Temperature

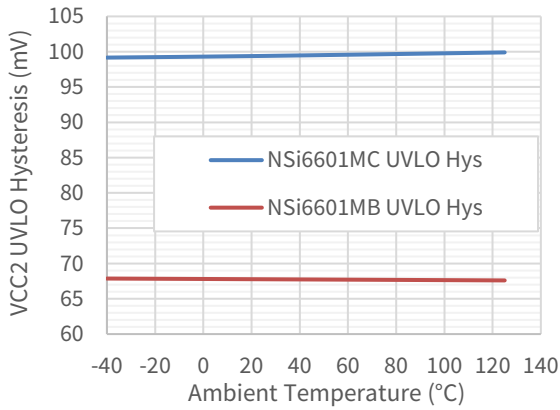


Figure 6.11 VCC2 UVLO Hysteresis Vs Temperature

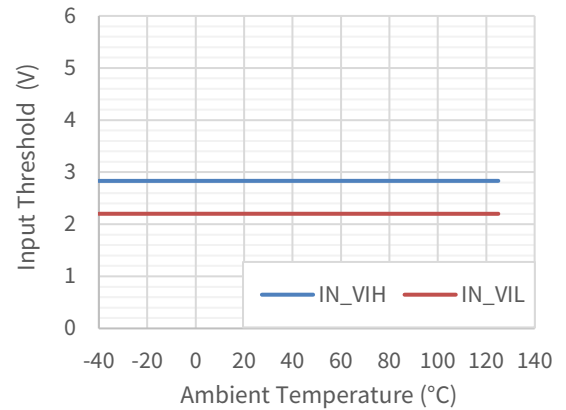


Figure 6.12 Input Threshold Vs Temperature

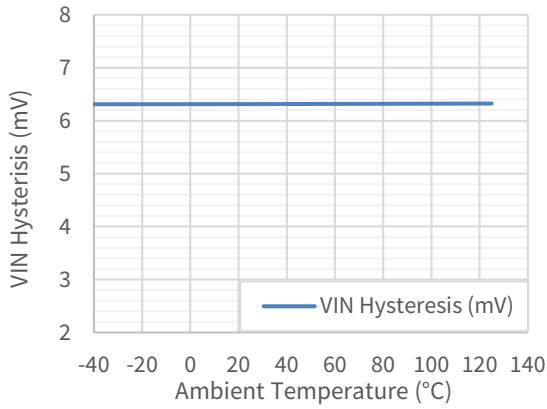


Figure 6.13 Input Hysteresis Vs Temperature

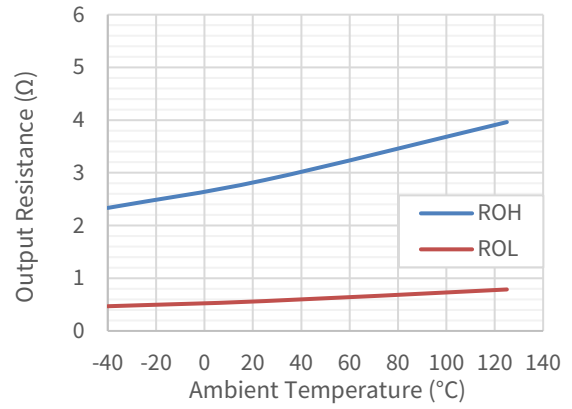


Figure 6.14 Output Resistance Vs Temperature

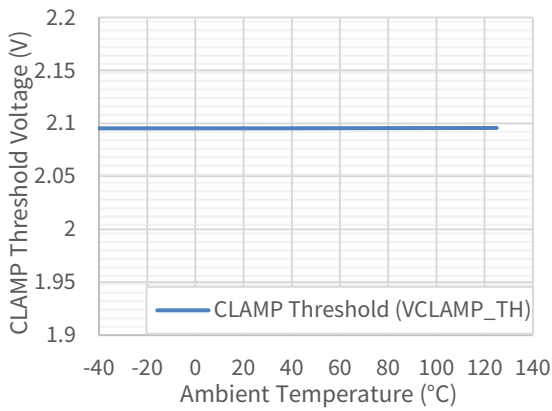


Figure 6.15 CLAMP Threshold Voltage Vs Temperature

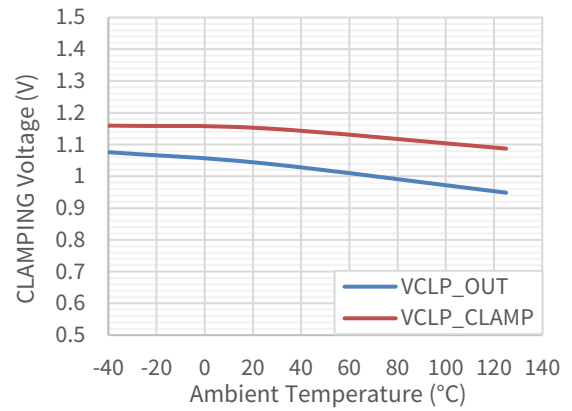


Figure 6.16 CLAMPING Voltage Vs Temperature

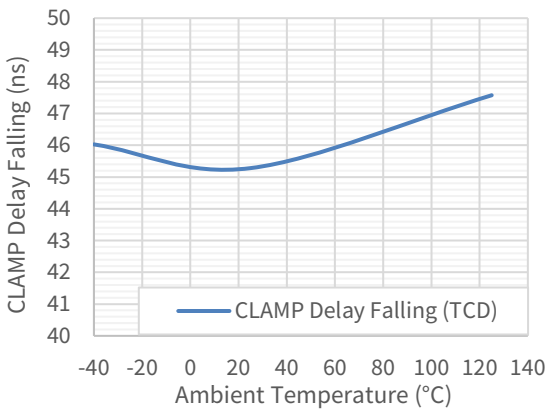


Figure 6.17 CLAMP Delay Falling Vs Temperature

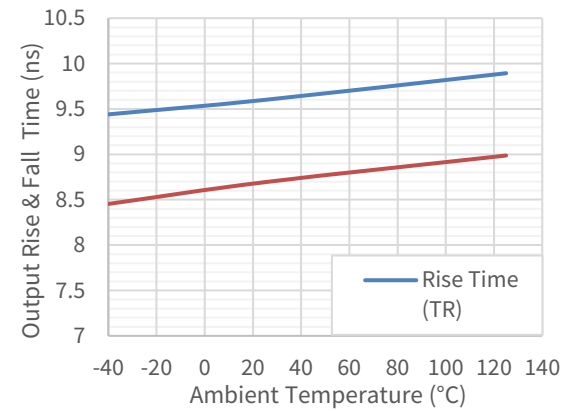


Figure 6.18 Output rise and fall time Vs Temperature

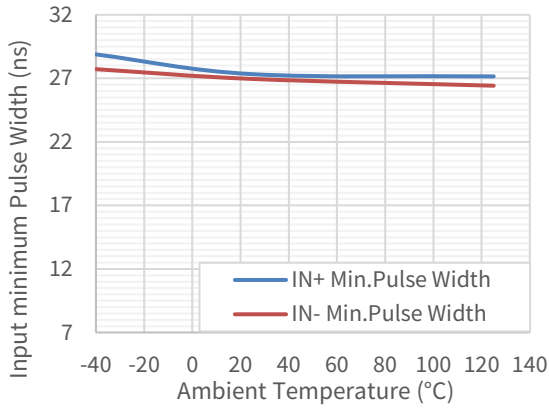


Figure 6.19 Minimum Pulse Width Vs Temperature

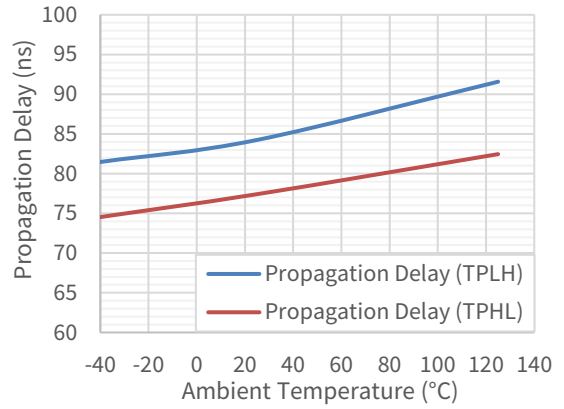


Figure 6.20 Propagation Delay Vs Temperature

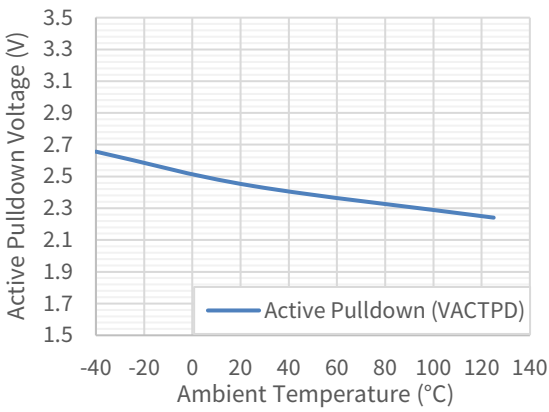


Figure 6.21 Active Pull-down Voltage Vs Temperature

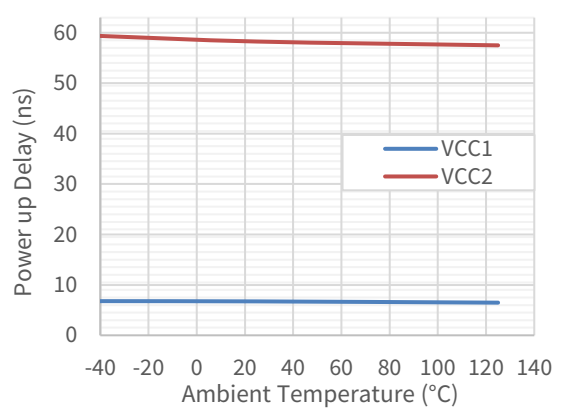


Figure 6.22 Power up Delay Vs Temperature

**6.4. Parameter Measurement Information**

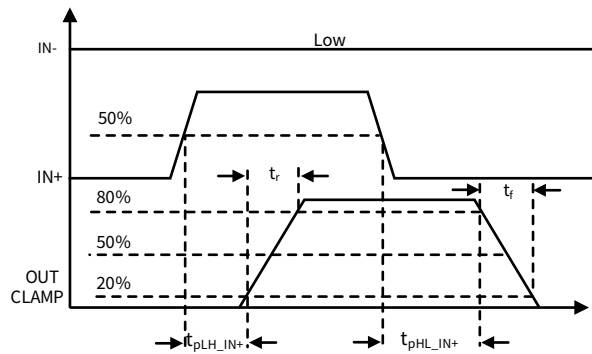


Figure 6.23 Propagation Delay, Rise Time and Fall Time (For Non-Inverting Configuration)

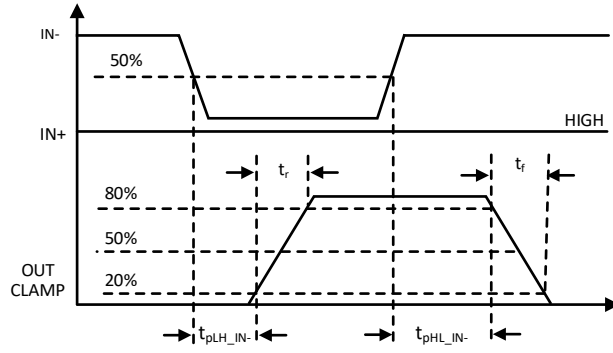


Figure 6.24 Propagation Delay, Rise Time and Fall Time (For Inverting Configuration)

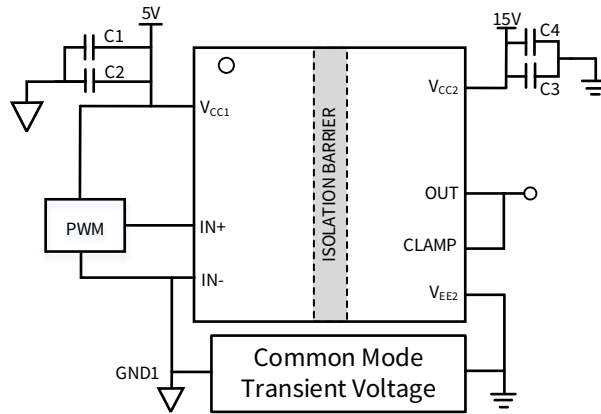


Figure 6.25 Common-Mode Transient Immunity Test Circuit

以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：<https://d.book118.com/226141125214011103>