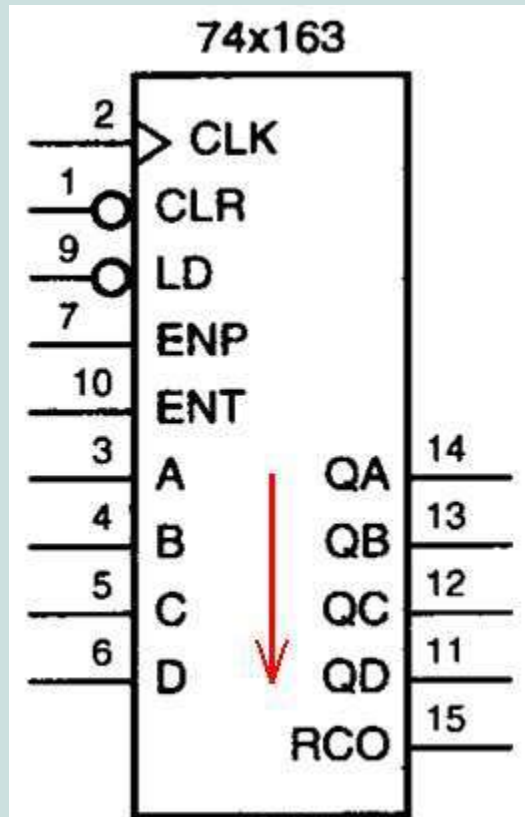


Chapter 8

Sequential logic design practices

Applications of binary counter

MSI Counters



CLR	LD	EN	Q*
1	X	X	0
0	1	X	A
0	0	1	Q+1
0	0	0	Q

Input port

ENP: enable for state change

ENT: enable for state change

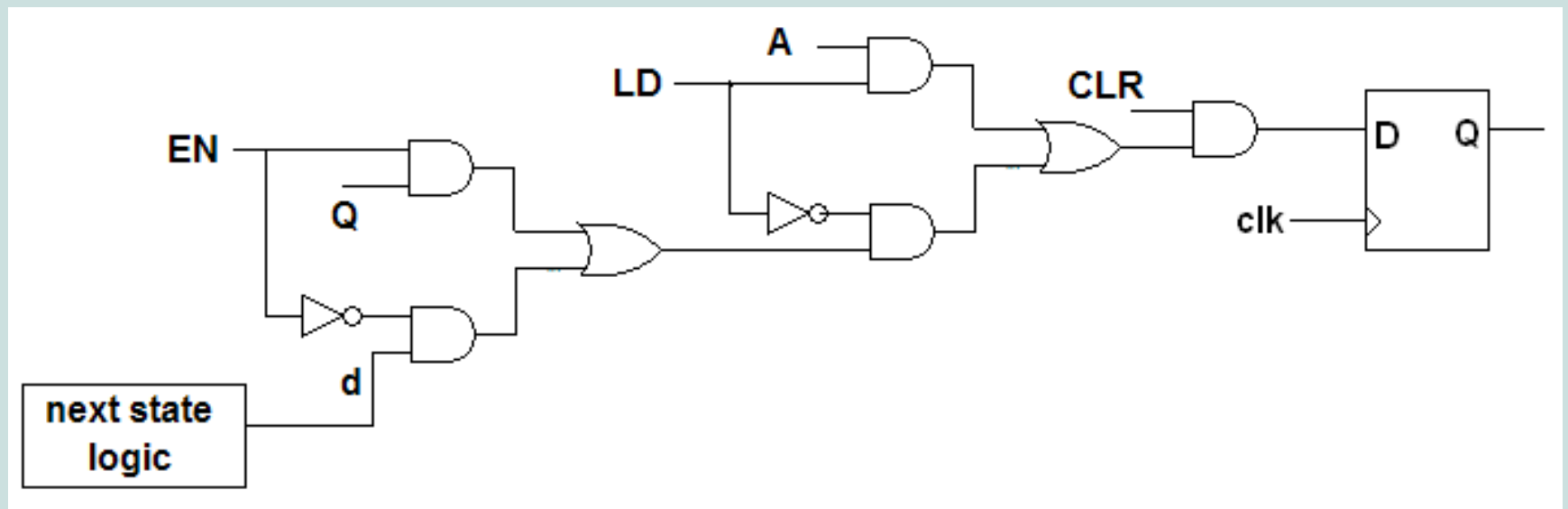
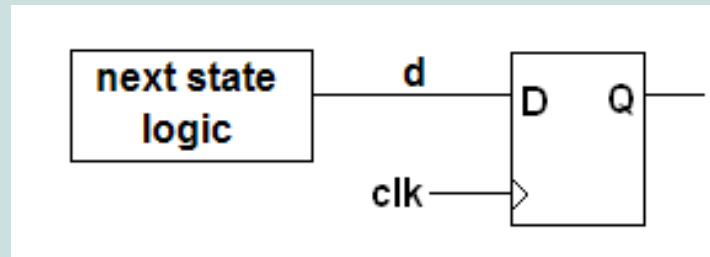
When ENT=0, RCO=0

Output port

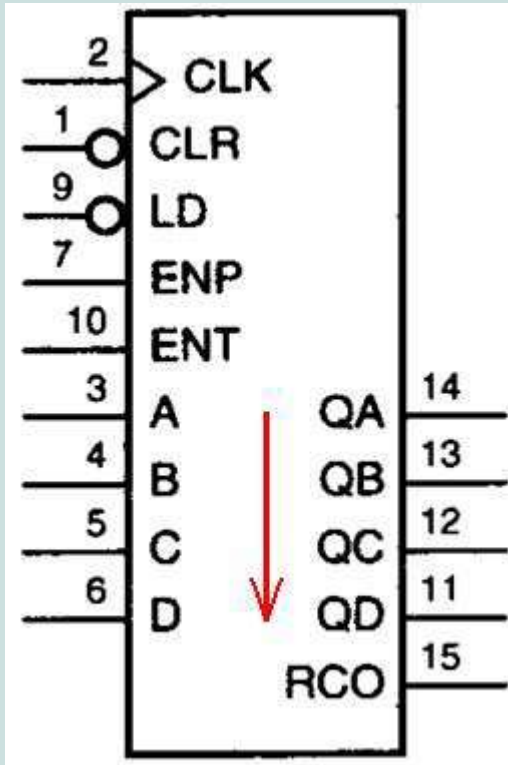
Initial state:0000 final state:1111

ROC: final state =1

MSI Counters



Other MSI Counters



**74x161:mode 16 binary counter
with asynchronous CLR**

Initial state:0000 Final state:1111

**74x160:mode 10 counter with binary
code and asynchronous CLR**

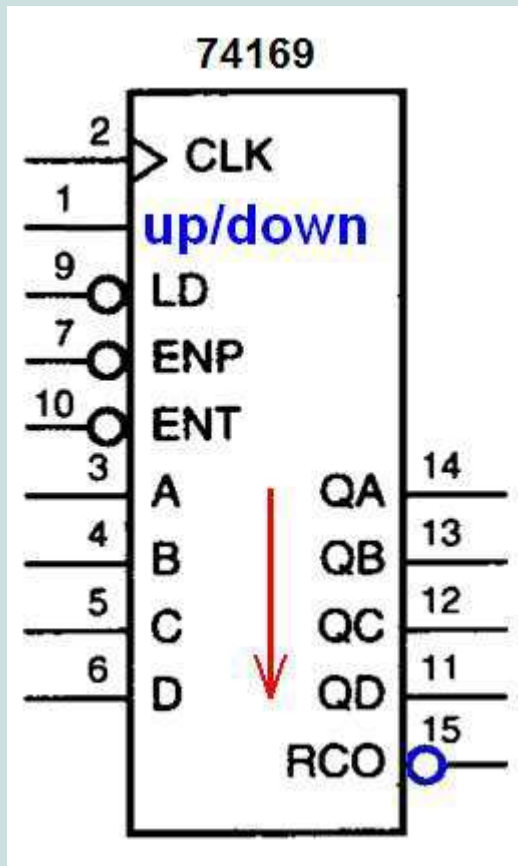
Initial state:0000 Final state:1001

**74x162:mode 10 counter with binary
code and synchronous CLR**

Initial state:0000 Final state:1001

Last state: ROC =1

Other MSI Counters



LD	EN	UP/DOWN	Q*
1	X	X	A
0	0	X	Q
0	1	1	Q+1
0	1	0	Q-1

up/down=1:up

Initial state:0000

Last state:1111

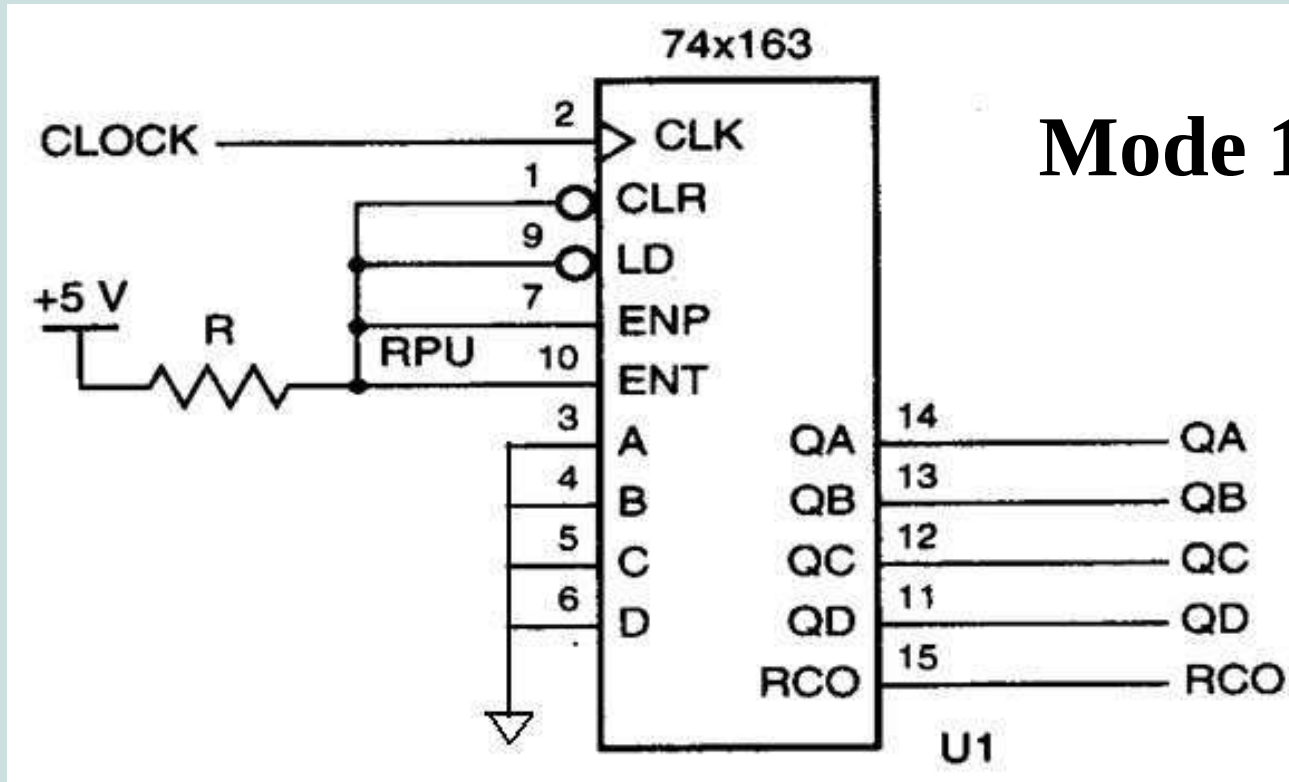
up/down=0:down

Initial state:1111

Last state:0000

Last state: RCO=0 !

The applications of MSI counters



Mode 16 counter

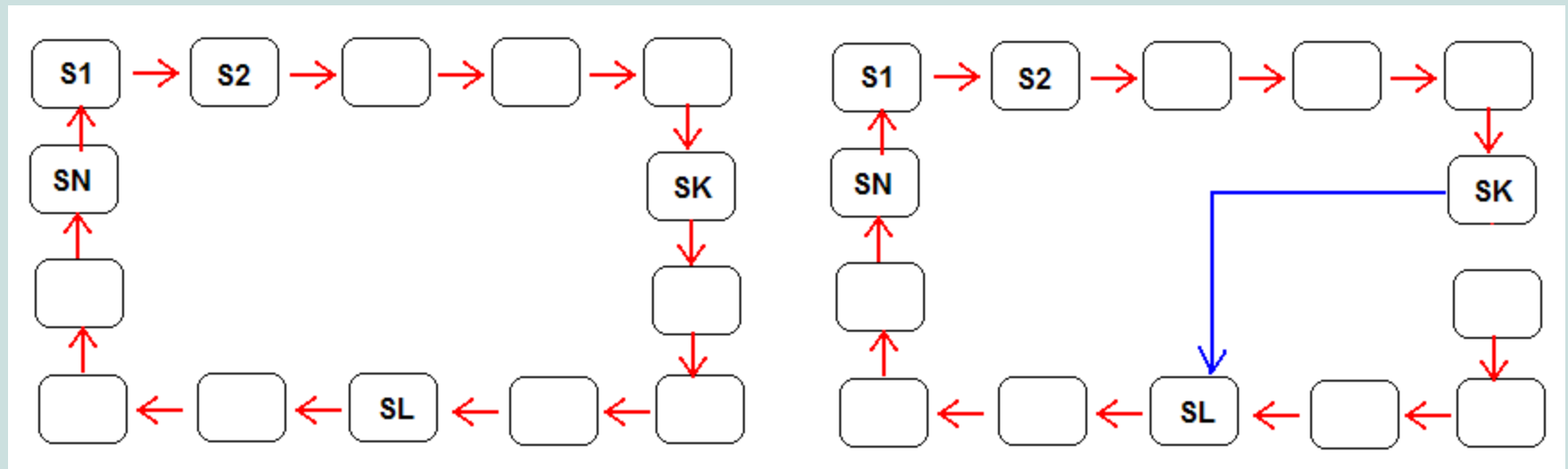
Initial state: 0000

Final state: 1111

The diagram illustrates a 4-bit ripple-carry adder implemented using two 74x163 counters, U1 and U2. Both counters are configured as synchronous counters with the following connections:

- U1 (Left Counter):**
 - CLK:** Connected to the common CLOCK input.
 - CLR:** Connected to the common RESET_L input.
 - LD:** Connected to the common LOAD_L input.
 - ENP:** Connected to the common CNTEN input.
 - ENT:** Connected to pin 10.
 - Data Inputs (A-D):** D0, D1, D2, and D3 are connected to pins 3, 4, 5, and 6 respectively.
 - Outputs (QA-QD):** Labeled Q0, Q1, Q2, and Q3, connected to pins 14, 13, 12, and 11 respectively.
 - RCO:** Labeled RCO4, connected to pin 15.
- U2 (Right Counter):**
 - CLK:** Connected to the common CLOCK input.
 - CLR:** Connected to the common RESET_L input.
 - LD:** Connected to the common LOAD_L input.
 - ENP:** Connected to the common CNTEN input.
 - ENT:** Connected to pin 10.
 - Data Inputs (A-D):** D4, D5, D6, and D7 are connected to pins 3, 4, 5, and 6 respectively.
 - Outputs (QA-QD):** Labeled Q4, Q5, Q6, and Q7, connected to pins 14, 13, 12, and 11 respectively.
 - RCO:** Connected to pin 15.
- Ripple-Carry Connection:** The RCO output of U1 (RCO4) is connected to the ENT input of U2, acting as the carry-in for the second counter.
- Final Output:** The RCO output of U2 is connected to an AND gate, which produces the final RCO8 signal.

Mode change for counters

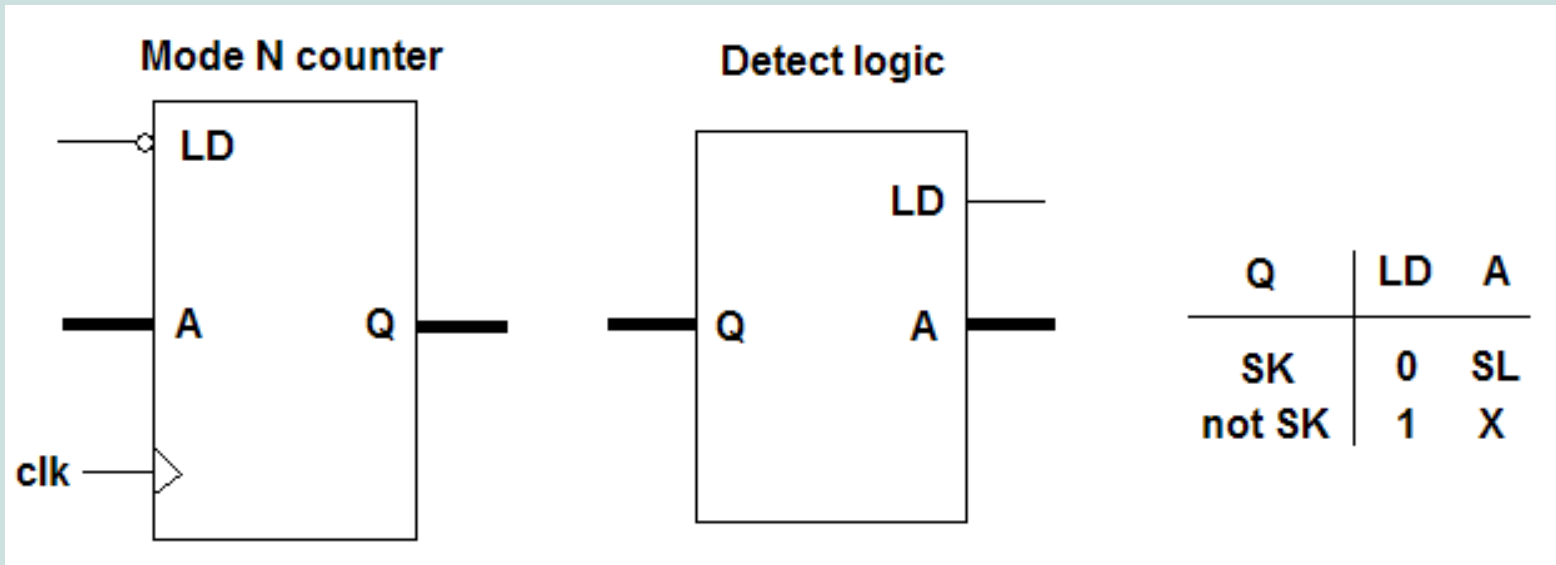


Key point:

Detect SK

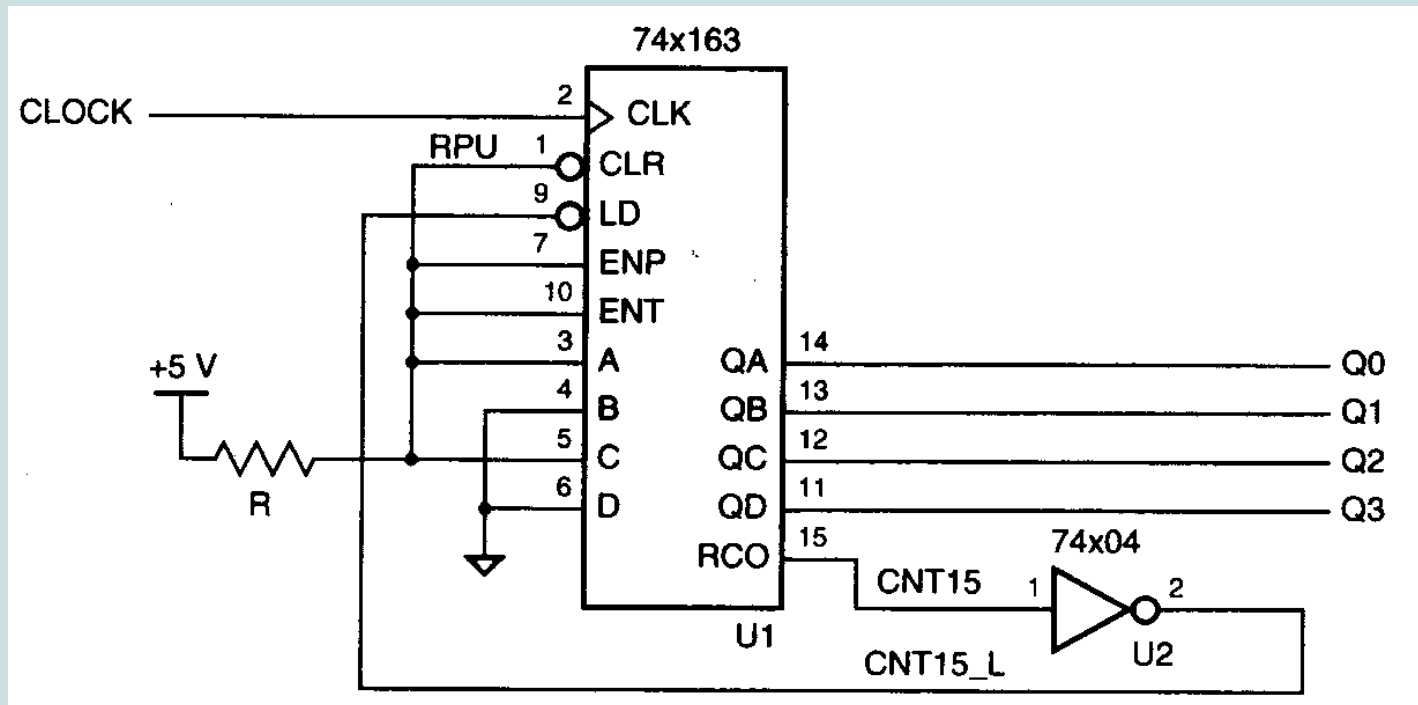
Set SL

Mode change for counters



A may be constant

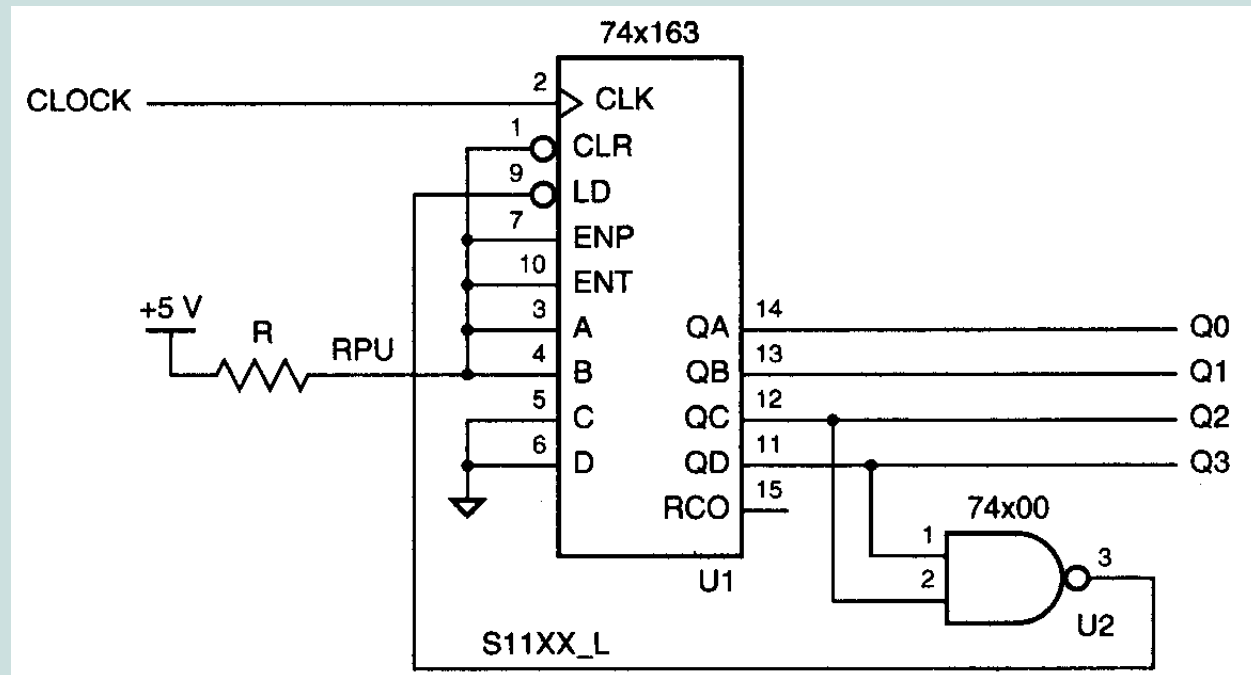
Mode change for counters



Mode-11: 5----15

Detect 1111 Set 0101

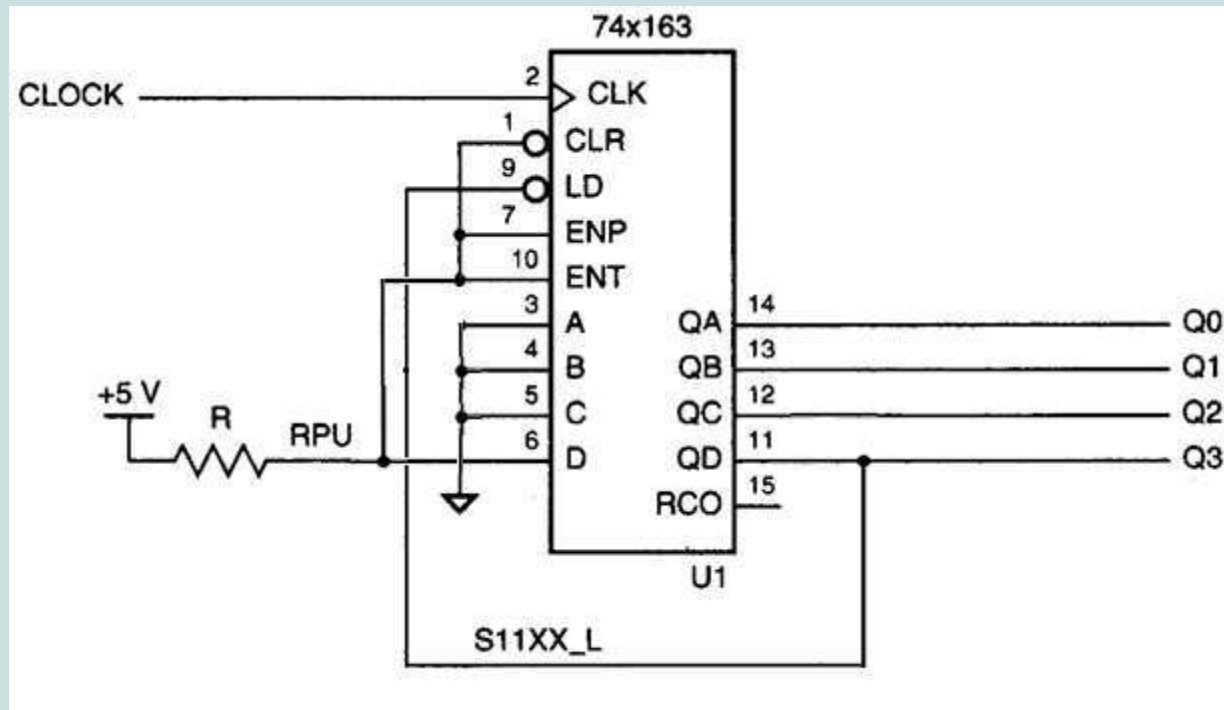
Mode change for counters



Mode 10 : 3---12 (Excess-3 code)

Detect 1100 Set 0011

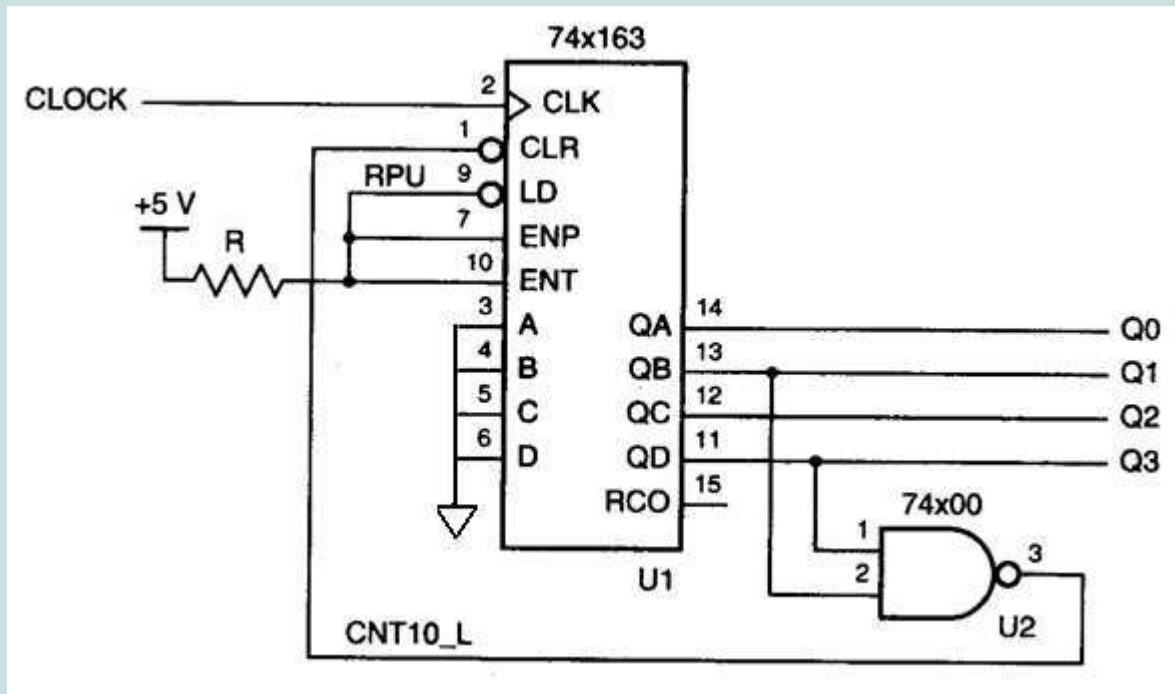
Mode change for counters



Mode 9 : 8---0

Detect 0000 Set 1000

Mode change for counters



Mode 11 : 0---10

Detect 1010 Set 0000

以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：<https://d.book118.com/227116135052006034>