National Semiconductor

October 2004

LM4990 Boomer® Audio Power Amplifier Series
2 Watt Audio Power Amplifier with Selectable Shutdown Logic Level

General Description

The LM4990 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.25 watts of continuous average power to an 8Ω BTL load and 2 watts of continuous average power (LD and MH only) to a 4Ω BTL load with less than 1% distortion (THD+N+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4990 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4990 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by either logic high or low depending on mode selection. Driving the shutdown mode pin either high or low enables the shutdown pin to be driven in a likewise manner to enable shutdown.

The LM4990 contains advanced pop & click circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions.

The LM4990 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- Improved PSRR at 217Hz & 1KHz 62dB
- Power Output at 5.0V, 1% THD+N, 4Ω (LD and MH only) 2W (typ)
- Power Output at 5.0V, 1% THD+N, 8Ω 1.25W (typ)
- Power Output at 3.0V, 1% THD+N, 4Ω 600mW (typ)
- Power Output at 3.0V, 1% THD+N, 8Ω 425mW (typ)
- Shutdown Current 0.1µA (typ)

Features

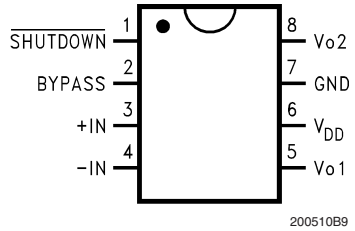
- Available in space-saving packages: LLP, Exposed-DAP TSSOP, MSOP, and ITL
- Ultra low current shutdown mode
- Improved pop & click circuitry eliminates noise during turn-on and turn-off transitions
- 2.2 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability
- User selectable shutdown High or Low logic Level

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

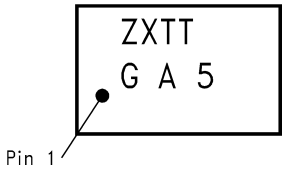
Connection Diagrams

Mini Small Outline (MSOP) Package



Top View
Order Number LM4990MM
See NS Package Number MUA08A

MSOP Marking



Top View
Z - Plant Code
X - Date Code
TT - Die Traceability
G - Boomer Family
A5 - LM4990MM

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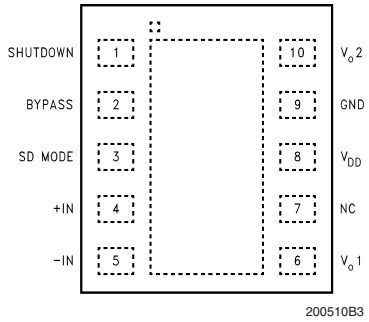
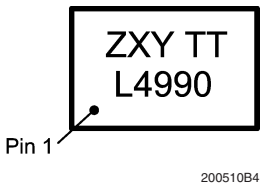
Connection Diagrams (Continued)

LLP Package



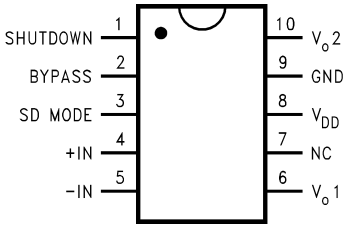
Top View
Order Number LM4990LD
See NS Package Number LDA10B

LLP Marking



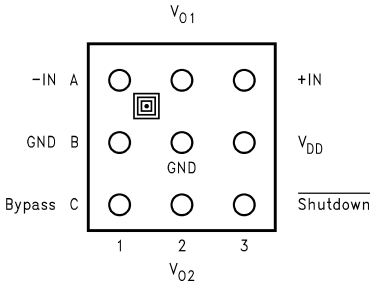
Top View
Z - Plant Code
XY - Date Code
TT - Die Traceability
Bottom Line - Part Number

Exposed-DAP TSSOP Package



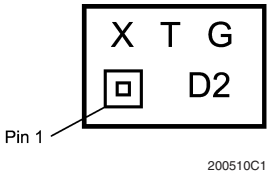
Top View
Order Number LM4990MH
See NS Package Number MXF10A

9 Bump micro SMD



Top View
Order Number LM4990ITL, LM4990ITLX
See NS Package Number TLA09ZZA

9 Bump micro SMD Marking



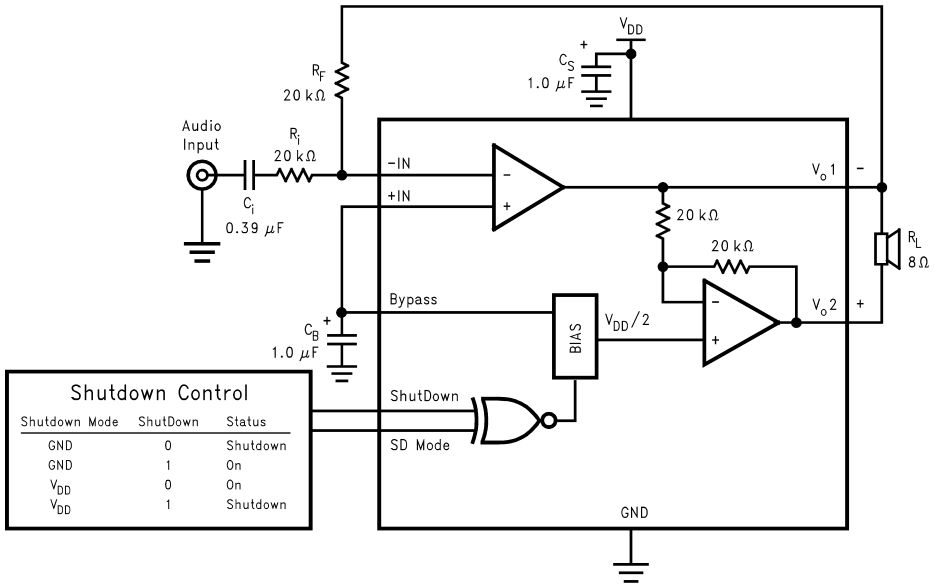
Top View
X — Date Code
T — Die Traceability
G — Boomer Family
D2 — LM4990ITL

Package	LD	MH	MM	ITL
Shutdown Mode	Selectable	Selectable	Low	Low
Typical Power Output at 5V, 1% THD+N	2W (R_L = 4Ω)	2W (R_L = 4Ω)	1.25W (R_L = 8Ω)	1.25W (R_L = 8Ω)

. A SD_MODE select pin determines the Shutdown Mode for the LD and MH packages, whether it is an Asserted High or an Asserted Low device, to activate shutdown.

. The SD_MODE select pin is not available with the MM and ITL packaged devices. Shutdown occurs only with a low assertion.

Typical Application



Note: MM and ITL packaged devices are active low only; Shutdown Mode pin is internally tied to GND.

FIGURE 1. Typical Audio Amplifier Application Circuit (LD and MH)

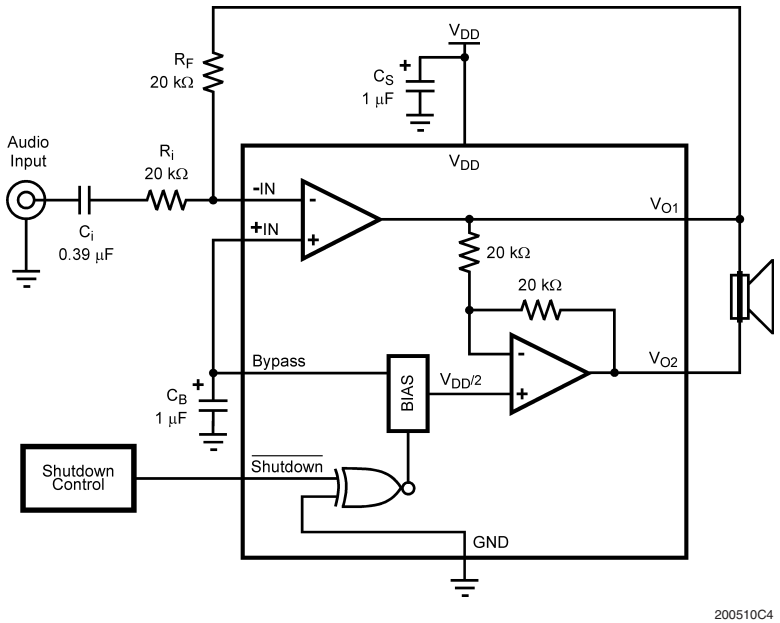


FIGURE 2. Typical Audio Amplifier Application Circuit (ITL and MM)

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 11)	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Notes 3, 12)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JC} (MSOP)	56˚C/W
θ_{JA} (MSOP)	190˚C/W
θ_{JA} (9 Bump micro SMD) (Note 15)	180˚C/W
θ_{JA} (LLP)	63˚C/W (Note 13)
θ_{JC} (LLP)	12˚C/W (Note 13)
Soldering Information	
See AN-1187 "Leadless Leadframe Package (LLP)."	

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40˚C \le T_A \le 85˚C$
Supply Voltage	$2.2V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4990		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	3	7	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	4	10	mA (max)
I_{SD}	Shutdown Current	$V_{SD} = V_{SD\ Mode}$ (Note 8)	0.1	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE} = V_{DD}$	1.5		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE} = V_{DD}$	1.3		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.5		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.3		V
V_{OS}	Output Offset Voltage		7	50	mV (max)
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7	kΩ (max)
				7.0	kΩ (min)
P_o	Output Power (8Ω)	THD+N = 1% (max); f = 1kHz	1.25	0.9	W (min)
	(4Ω) (Notes 13, 14)	THD+N = 1% (max); f = 1kHz	2		W
T_{WU}	Wake-up time		100		ms
THD+N+N	Total Harmonic Distortion+Noise	P_o = 0.5Wrms; f = 1kHz	0.2		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	60 (f = 217Hz) 64 (f = 1kHz)	55	dB (min)

Electrical Characteristics V_{DD} = 3V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4990		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	2	7	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	3	9	mA (max)
I_{SD}	Shutdown Current	$V_{SD} = V_{SD\ Mode}$ (Note 8)	0.1	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE} = V_{DD}$	1.1		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE} = V_{DD}$	0.9		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.3		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.0		V
V_{OS}	Output Offset Voltage		7	50	mV (max)
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7	kΩ (max)
				7.0	kΩ (min)

Electrical Characteristics V_{DD} = 3V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C. (Continued)

Symbol	Parameter	Conditions	LM4990		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
P_o	Output Power (8Ω)	THD+N = 1% (max); f = 1kHz	425		mW
	(4Ω)	THD+N = 1% (max); f = 1kHz	600		mW
T_{WU}	Wake-up time		75		ms
THD+N+N	Total Harmonic Distortion+Noise	P_o = 0.25Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	62 (f = 217Hz) 68 (f = 1kHz)	55	dB (min)

Electrical Characteristics V_{DD} = 2.6V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4990		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	2.0		mA
		V_{IN} = 0V, I_o = 0A, 8Ω Load	3.0		mA
I_{SD}	Shutdown Current	V_{SD} = $V_{SD\ Mode}$ (Note 8)	0.1		µA
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = V_{DD}	1.0		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = V_{DD}	0.9		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.2		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.0		V
V_{OS}	Output Offset Voltage		5	50	mV (max)
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7	kΩ (max)
				7.0	kΩ (min)
P_o	Output Power (8Ω)	THD+N = 1% (max); f = 1kHz	300		mW
	(4Ω)	THD+N = 1% (max); f = 1kHz	400		
T_{WU}	Wake-up time		70		ms
THD+N+N	Total Harmonic Distortion+Noise	P_o = 0.15Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	51 (f = 217Hz) 51 (f = 1kHz)		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4990, see power derating curves for additional information.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF – 240pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: For micro SMD only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

Note 9: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 10: R_{ROUT} is measured from the output pin to ground. This value represents the parallel combination of the 10kΩ output resistors and the two 20kΩ resistors.

Note 11: If the product is in Shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the device will be protected. If the device is enabled when V_{DD} is greater than 5.5V and less than 6.5V, no damage will occur, although operation life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.

Note 12: Maximum power dissipation in the device (P_{DMAX}) occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 1 shown in the **Application Information** section. It may also be obtained from the power dissipation graphs.