# Fronthaul Compression Intel® FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **23.1**

IP Version: **1.0.5**

Online Version
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# 1. About the Fronthaul Compression Intel® FPGA IP

The Fronthaul Compression IP consists of compression and decompression for U-plane IQ data. The compression engine computes μ-law or block floating-point compression based on user data compression header (udCompHdr). This IP uses an Avalon streaming interface for IQ data, conduit signals, and for metadata and sideband signals, and Avalon memory-mapped interface for control and status registers (CSRs).

The IP maps compressed IQs and the user data compression parameter (udCompParam) as per the section payload frame format specified in the O-RAN specification *O-RAN Fronthaul Control, User and Synchronization Plane Version 3.0 - April 2020 (O-RAN-WG4.CUS.0-v03.00)*. Avalon streaming sink and source interface data width are 128-bits for the application interface and 64 bits for the transport interface to support maximum compressoin ratio of 2:1.

**Related Information**

O-RAN website

## 1.1. Fronthaul Compression Intel® FPGA IP Features

- μ-law and block floating-point compression and decompression
- IQ width 8-bit to 16-bit
- Static and dynamic configuration of U-plane IQ format and compression header
- Multisections packet (if **O-RAN Compliant** is on)

## 1.2. Fronthaul Compression Intel® FPGA IP Device Family Support

Intel offers the following device support levels for Intel FPGA IP:

- Advance support—the IP is available for simulation and compilation for this device family. FPGA programming file (`.pof`) support is not available for Quartus Prime Pro Stratix 10 Edition Beta software and as such IP timing closure cannot be guaranteed. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- Preliminary support—Intel verifies the IP core with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. You can use it in production designs with caution.
- Final support—Intel verifies the IP with final timing models for this device family. The IP meets all functional and timing requirements for the device family. You can use it in production designs.

**Table 1. Fronthaul Compression IP Device Family Support**

| Device Family | Support |
|---|---|
| Intel Agilex® 7 (E-tile) | Preliminary |
| Intel Agilex 7 (F-tile) | Advance |
| Intel® Arria® 10 | Final |
| Intel Stratix® 10 (H-, and E-tile devices only) | Final |
| Other device families | No support |

**Table 2. Device Supported Speed Grades**

| Device Family | FPGA Fabric Speed Grade |
|---|---|
| Intel Agilex 7 | 3 |
| Intel Arria 10 | 2 |
| Intel Stratix 10 | 2 |

## 1.3. Release Information for the Fronthaul Compression Intel FPGA IP

Intel FPGA IP versions match the Intel Quartus® Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.