NOVOSENSE
纳芯微电子

NSI6602

High Reliability Isolated Dual-Channel Gate Driver

Datasheet (EN) 1.8

Product Overview

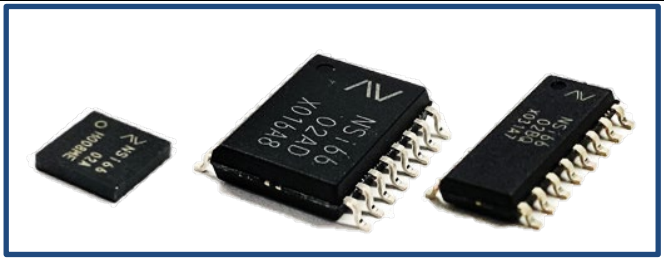
NSI6602 is a family of high reliability isolated dual-channel gate driver ICs which can be designed to drive power transistor up to 2MHz switching frequency. Each output could source 4A and sink 6A peak current with fast 25ns propagation delay and 5ns maximum delay matching.

The NSI6602 provides 2500Vrms isolation per UL1577 in 5-mm x 5-mm LGA13 package, 3000Vrms isolation in SOP16 package, and 5700Vrms isolation in SOW16 or SOW14 package. System robustness is supported by 150kV/μs typical common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 25V, while the input-side accepts from 2.7V to 5V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

Key Features

- Isolated dual channel driver
- Input side supply voltage: 2.7V to 5.5V
- Driver side supply voltage: up to 25V with UVLO
- 4A peak source and 6A peak sink output
- High CMTI: ±150kV/μs typical
- 25ns typical propagation delay
- 5ns maximum delay matching
- 6ns maximum pulse width distortion
- Programmable deadtime
- Accepts minimum input pulse width 15ns
- Operation temperature: -40℃~125℃
- RoHS & REACH Qualified



Safety Regulatory Approvals

- UL recognition:
  - LGA13: 2500V_{rms} for 1 minute per UL1577
  - SOW16/SOW14: 5700V_{rms} for 1 minute per UL1577
  - SOP16: 3000V_{rms} for 1 minute per UL1577
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

Applications

- Isolated DC-DC and AC-to-DC power supplies in server, telecom, and industry
- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers

Functional Block Diagram

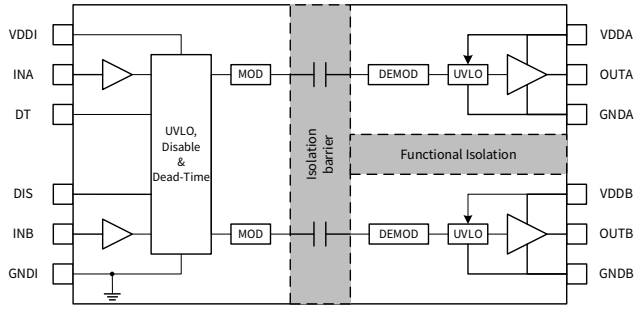


Figure 0.1 NSI6602 Block Diagram

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1. Pin Configuration and Functions

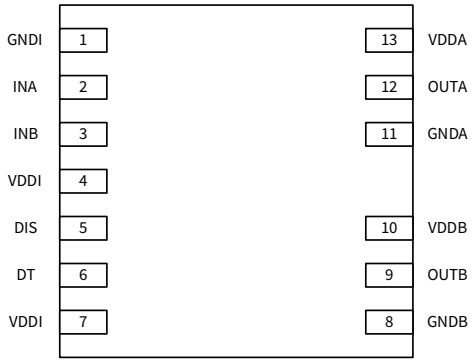

Figure 1.1 NSI6602 LGA13 Package

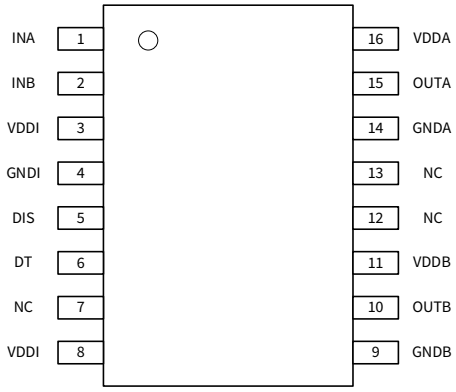

Figure 1.2 NSI6602 SOW16 Package

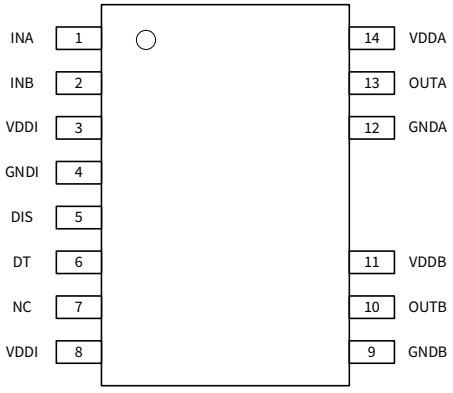

Figure 1.3 NSI6602 SOW14 Package

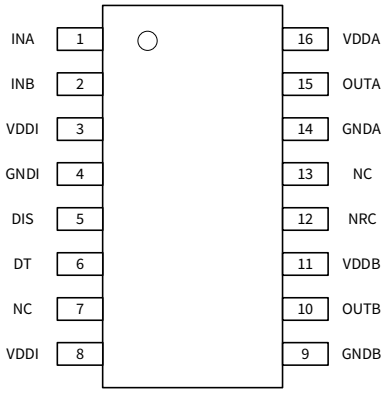

Figure 1.4 NSI6602 SOP16 Package

Table 1.1 NSI6602 Pin Configuration and Description

PIN NO.				SYMBOL	FUNCTION
LGA13	SOW16	SOP16	SOW14		
1	4	4	4	GND	Input-side ground reference.
2	1	1	1	INA	TTL/CMOS compatible input signal for channel A with internal pull down to GND. It is recommended to connect this pin to GND if not used.
3	2	2	2	INB	TTL/CMOS compatible input signal for channel B with internal pull down to GND. It is recommended to connect this pin to GND if not used.
4, 7	3, 8	3, 8	3, 8	VDDI	Input-side supply voltage. It is recommended to place a bypass capacitor from this pin to GND as close as possible.
5	5	5	5	DISABLE	Disables the isolator inputs and driver outputs if asserted high, enables if asserted low or left open. It is recommended to connect this pin to GND if not used.
6	6	6	6	DT	Programmable deadtime control. To allow the outputs overlapping by connecting DT to VDDI. Place a 1kΩ to 200kΩ resistor (R_{DT}) between DT and GND to adjust deadtime following: t_{DT} (ns) = 10 x R_{DT} (kΩ). It is recommended to parallel a low ESR capacitor, e.g., 2.2nF or above.
8	9	9	9	GNDB	Ground for output channel B
9	10	10	10	OUTB	Output gate driver for channel B
10	11	11	11	VDDB	Supply voltage for channel B
11	14	14	12	GNDA	Ground for output channel A
12	15	15	13	OUTA	Output gate driver for channel A
13	16	16	14	VDDA	Supply voltage for channel A
/	7,12,13	7, 13	7	NC	Not connected
/	/	12	/	NRC	Internally connected to GNDB, not recommend connecting in circuit.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI to GNDI	-0.3	6	V
Output Side Supply Voltage	VDDA to GNDA, VDDB to GNDB	-0.3	30	V
Input Signal Voltage	INA, INB, DIS, DT to GNDI	-0.3	V_{VDDI}+0.3	V
	INA, INB, DIS, DT to GNDI, Transient for 50ns	-5	V_{VDDI}+0.3	V
Output Signal Voltage	OUTA to GNDA, OUTB to GNDB	-0.3	V_{VDDA}+0.3	V

Parameters	Symbol	Min	Max	Unit
			V_{VDDB}+0.3	
	OUTA to GNDA, OUTB to GNDB, Transient for 200ns	-2	V_{VDDA}+0.3 V_{VDDB}+0.3	V
Channel A to Channel B Voltage	GNDA to GNDB in LGA13 package		700	V
	GNDA to GNDB in SOP16&SOW16 package		1500	V
	GNDA to GNDB in SOW14 package		1850	V
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD RATINGS

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±4000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI to GNDI	3	5.5	V
Driver Side Supply Voltage	VDDA to GNDA, VDDB to GNDB (NSI6602A)	7	25	V
	VDDA to GNDA, VDDB to GNDB (NSI6602B)	9.4	25	V
	VDDA to GNDA, VDDB to GNDB (NSI6602C)	14.2	25	V
Input Signal Voltage	INA, INB, DIS, DT	0	V_{VDDI}	V
Ambient Temperature	T_a	-40	125	°C

5. Thermal Information

Parameters	Symbol	LGA13	SOW16/SOW14	SOP16	Unit
Junction-to-ambient thermal resistance[1)]	R_{JA}	209.5	97.0	150.5	°C/W
Junction-to-case(top) thermal resistance[2)]	$R_{JC(top)}$	48.4	23.3	21.2	°C/W
Junction-to-top characterization parameter[3)]	Ψ_{JT}	41.8	35.8	52.3	°C/W
Junction-to-board characterization parameter[3)]	Ψ_{JB}	31.9	39.0	55.6	°C/W

1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.
2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by traNSIent dual interface test method described in JESD51-14.
3) Obtained by Simulating in an environment described in JESD51-2a.

6. Specifications

6.1. Electrical Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=12V for NSI6602A/B, VDDA=VDDB=15V for NSI6602C, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at Ta=25℃

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Input Side Supply						
VDDI Quiescent Current	I_{VDDIQ}		0.75	2	mA	INA=0, INB=0
VDDI Operating Current	I_{VDDI}		1.8		mA	Input frequency 500kHz, $C_{OUTA/B}$=15pF
VDDI UVLO Rising Threshold	V_{VDDI_ON}	2.35	2.55	2.75	V	
VDDI UVLO Falling Threshold	V_{VDDI_OFF}	2.15	2.35	2.55	V	
VDDI UVLO Hysteresis	V_{VDDI_HYS}		0.2		V	
Output Side Supply						
Output Side Supply Voltage	V_{VDDA}, V_{VDDB}			25	V	Minimum defined by UVLO
VDDA/B Quiescent Current, per Channel	I_{VDDAQ}, I_{VDDBQ}		1.6	2.5	mA	INA=0, INB=0, VDDx=12V for 6V,8V UVLO; VDDx=15V for 13V UVLO
VDDA/B Operation Current, per Channel	I_{VDDA}, I_{VDDB}		3.2		mA	100pF, 500kHz, VDDx=12V for 6V,8V UVLO; VDDx=15V for 13V UVLO
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}	5.7	6.15	6.5	V	NSI6602A (6V)
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF}, V_{VDDB_OFF}	5.4	5.85	6.2	V	
VDDA/B UVLO Hysteresis	V_{VDDA_HYS}, V_{VDDB_HYS}		0.3		V	
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}	8.1	8.5	8.9	V	NSI6602B (8V)
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF}, V_{VDDB_OFF}	7.6	8.0	8.4	V	
VDDA/B UVLO Hysteresis	V_{VDDA_HYS}, V_{VDDB_HYS}		0.5		V	
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}	12.7	13.2	13.7	V	NSI6602C (13V)
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF}, V_{VDDB_OFF}	11.7	12.2	12.7	V	
VDDA/B UVLO Hysteresis	V_{VDDA_HYS}, V_{VDDB_HYS}		1		V	
Input Side Characteristic						
Input Pin Pull Down Resistance, INA, INB	R_{INA_PD}, R_{INB_PD}		100		kΩ	
Input Pin Pull Down Resistance, DIS (EN)	R_{DIS_PD}		100		kΩ	
Logic High Input Threshold	V_{INA_H}, V_{INB_H}, V_{DIS_H}		1.7	2	V	

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Logic Low Input Threshold	V_{INA_L}, V_{INB_L}, V_{DIS_L}	0.8	1.1		V	
Input Hysteresis	V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}		0.6		V	
Output Side Characteristic						
Logic High Output Voltage	V_{VDDA}-V_{OUTA_H}, V_{VDDB}-V_{OUTB_H}		0.34		V	I_{out} = 100mA
Logic Low Output Voltage	V_{OUTA_L}, V_{OUTB_L}		55		mV	I_{out} = -100mA
Output Source Resistance [1]	R_{OUTA_H}, R_{OUTB_H}		3.4		Ω	I_{out} = 100mA
Output Sink Resistance	R_{OUTA_L}, R_{OUTB_L}		0.55		Ω	I_{out} = -100mA
Peak Output Source Current	I_{OUTA+}, I_{OUTB+}		4		A	
Peak Output Sink Current	I_{OUTA-}, I_{OUTB-}		6		A	

1) The output source structure features a P-channel MOSFET and an N-channel MOSFET in parallel. The on-resistance of this N-channel MOSFET is approximately 1.1Ω .

6.2. Switching Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=12V for NSI6602A/B, VDDA=VDDB=15V for NSI6602C, Ta=-40℃ to 125℃.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Pulse Width	t_{PWmin}		10	15	ns	$C_{OUTA/B}$ = 0 pF
Propagation Delay	t_{PDHL}, t_{PDLH}	10	25	35	ns	
Pulse Width Distortion $\lvert t_{PDLH}-t_{PDHL}\rvert$	t_{PWD}			6	ns	
Channel to Channel Delay Matching	t_{DMLH}, t_{DMHL}			5	ns	
Programmed Deadtime	t_{DT}	160	200	240	ns	t_{DT}(ns)=10*R(kΩ); Test for R = 20kΩ
Output Rise Time (20% to 80%)	t_R		7	16	ns	$C_{OUTA/B}$=1.8nF, verified by design
Output Fall Time (90% to 10%)	t_F		6	12	ns	$C_{OUTA/B}$=1.8nF, verified by design
Shutdown Time from Disable True	t_{DIS}			40	ns	
Recovery Time from Disable False	t_{EN}			40	ns	
VDDI Power-up Time Delay (Time from VDDI = VDDI_ON to OUTA/B = INA/B)	t_{start_VDDI}		8.5	15	μs	INA or INB tied to VDDI
VDDA/B Power-up Time Delay (Time from VDDA/B = 2V to OUTA/B = INA/B)	t_{start_VDDA}, t_{start_VDDB}		18	30	μs	INA or INB tied to VDDI $C_{OUTA/B}$=1.8nF
Common Mode Transient Immunity	CMTI	100	150		kV/μs	verified by design

6.3. Typical Performance Characteristics

VDDI = 3.3 V, VDDA=VDDB=12V for NSI6602A/B, VDDA=VDDB=15V for NSI6602C, TA = 25°C. Output has no load unless otherwise noted.

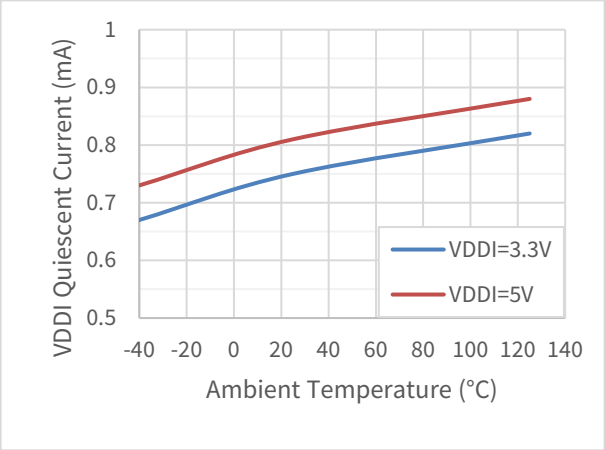

Figure 6.1 VDDI Quiescent Current vs Temperature

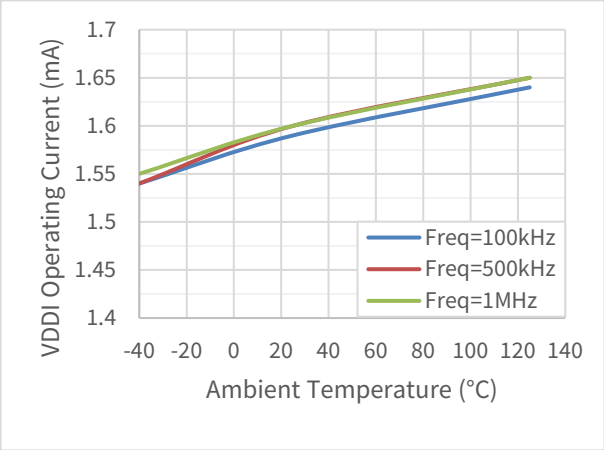

Figure 6.2 VDDI Operating Current vs Temperature

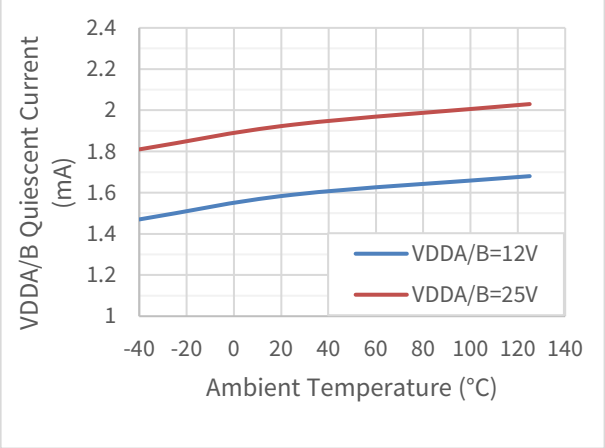

Figure 6.3 VDDA/B Quiescent Current vs Temperature

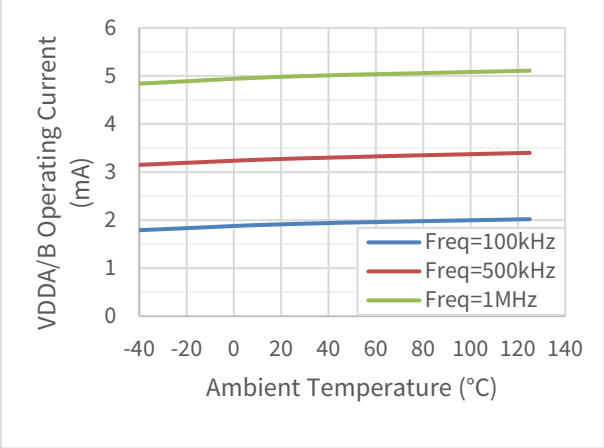

Figure 6.4 VDDA/B Operating Current vs Temperature

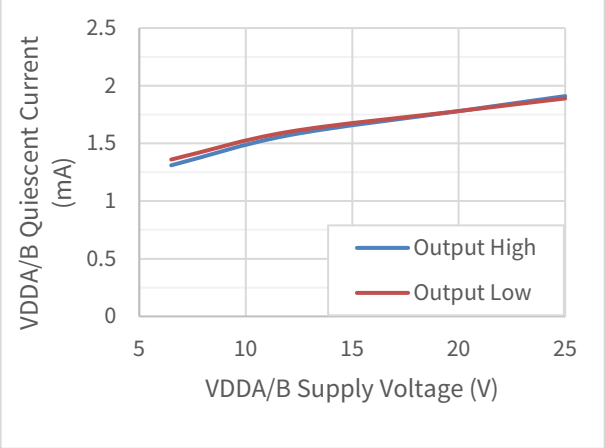

Figure 6.5 VDDA/B Quiescent Current vs Supply Voltage

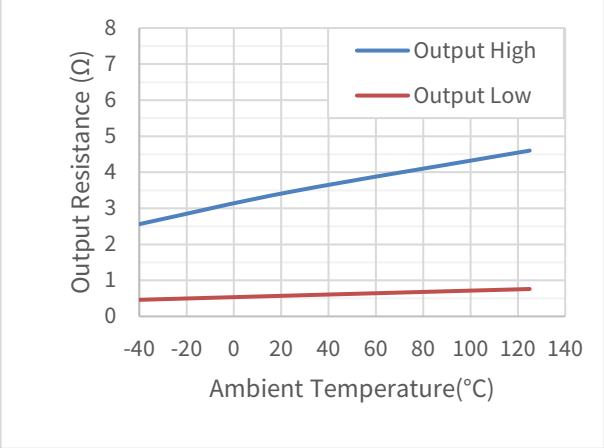

Figure 6.6 Output Resistance vs Temperature

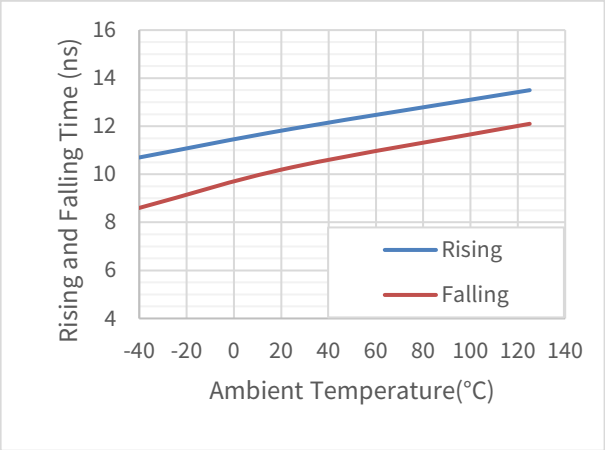

Figure 6.7 Typical Rise Time & Fall Time vs Temperature

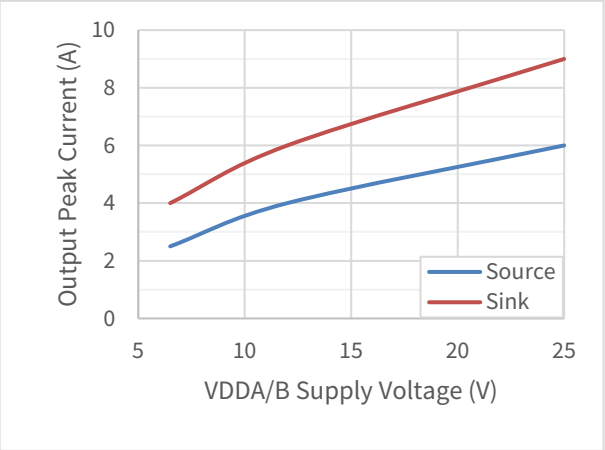

Figure 6.8 Output Peak Current vs VDDA/B Supply Voltage

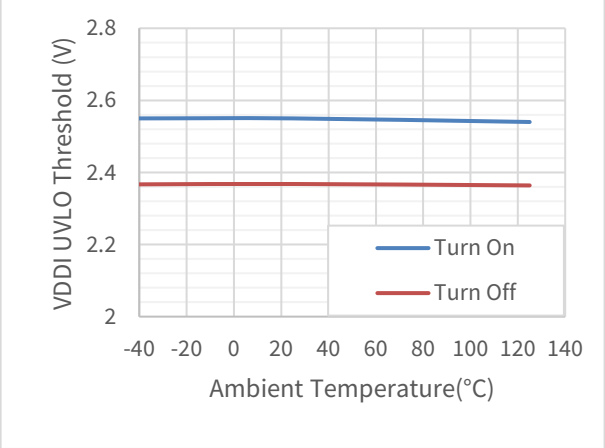

Figure 6.9 VDDI UVLO Threshold vs Temperature

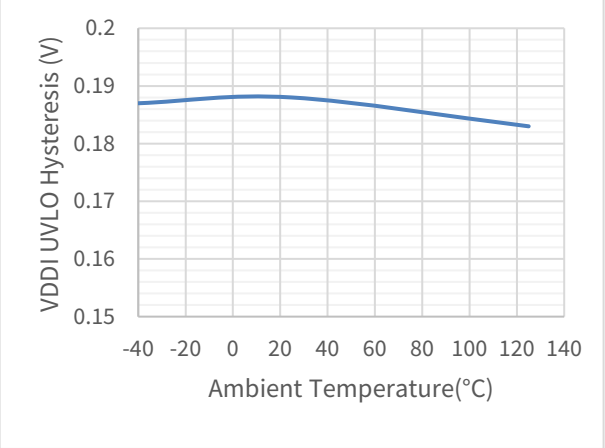

Figure 6.10 VDDI UVLO Hysteresis vs Temperature

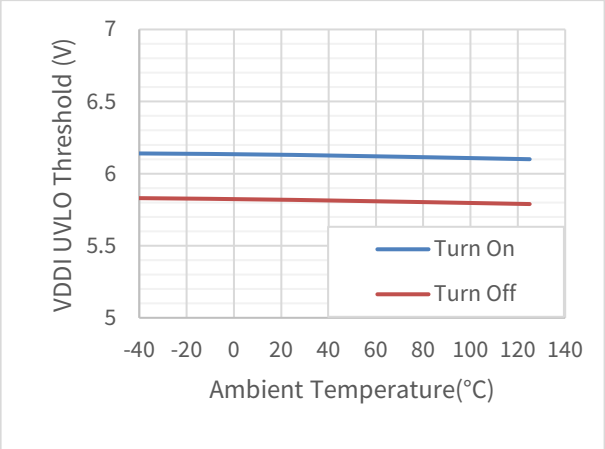

Figure 6.11 6V VDDA/B UVLO Threshold vs Temperature

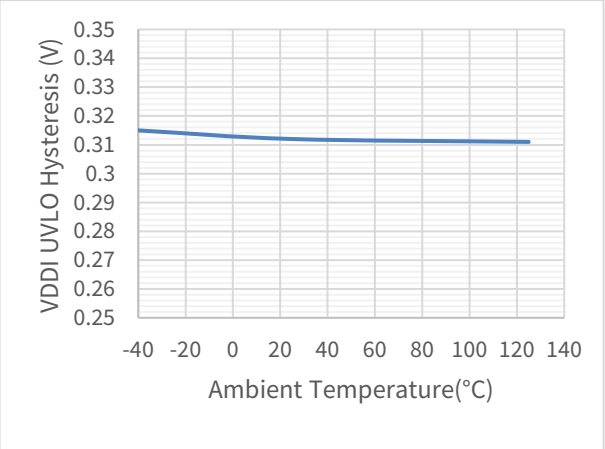

Figure 6.12 6V VDDA/B UVLO Hysteresis vs Temperature

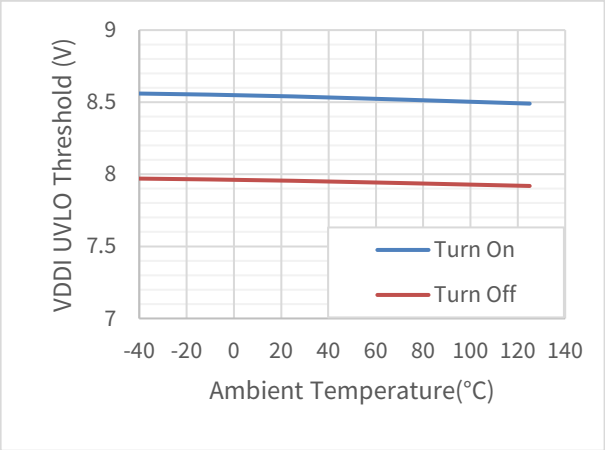

Figure 6.13 8V VDDA/B UVLO Threshold vs Temperature

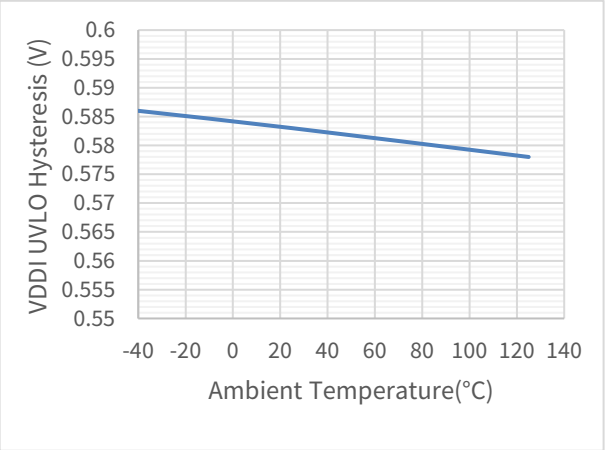

Figure 6.14 8V VDDA/B UVLO Hysteresis vs Temperature

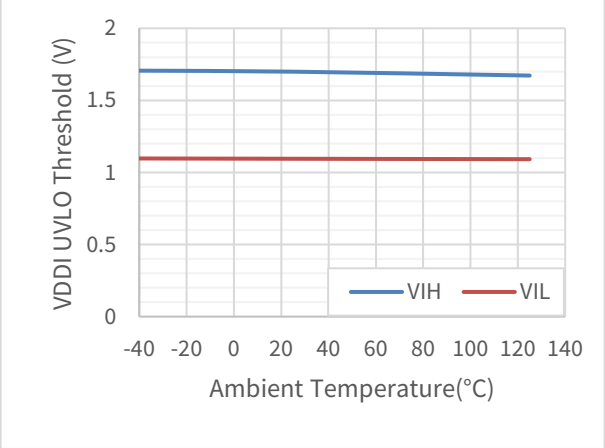

Figure 6.15 INA/INB/DIS Threshold vs Temperature

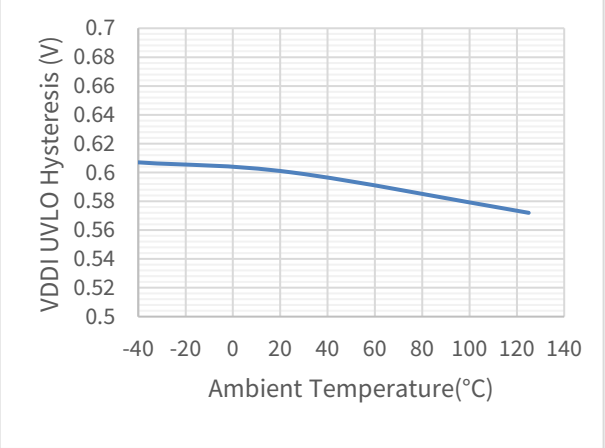

Figure 6.16 INA/INB/DIS Hysteresis vs Temperature

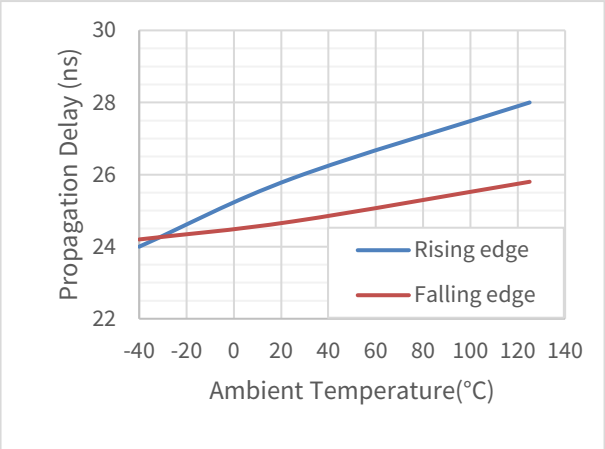

Figure 6.17 Propagation Delay vs Temperature

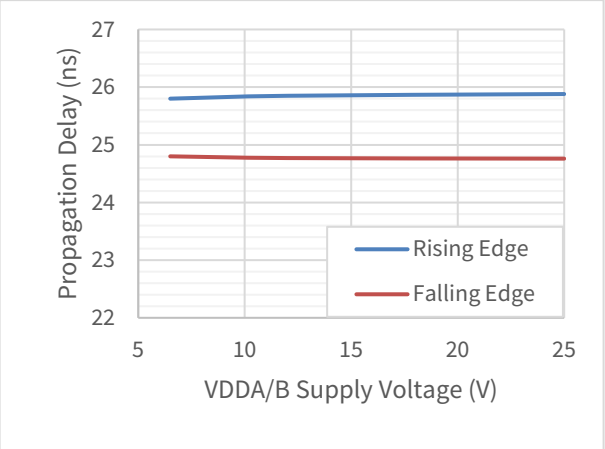

Figure 6.18 Propagation Delay vs VDDA/B

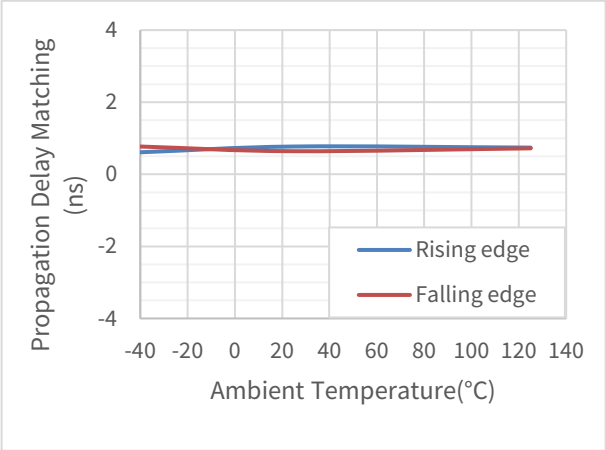

Figure 6.19 Propagation Delay Matching vs Temperature

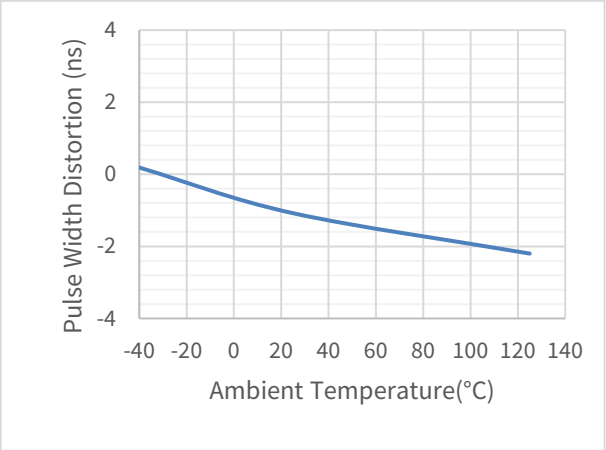

Figure 6.20 Pulse Width Distortion vs Temperature

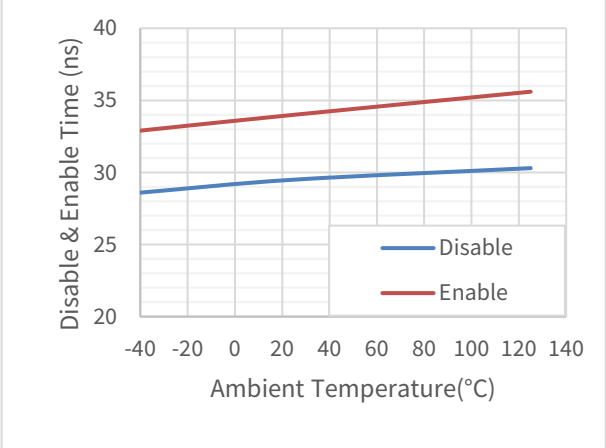

Figure 6.21 Disable & Enable Time vs Temperature

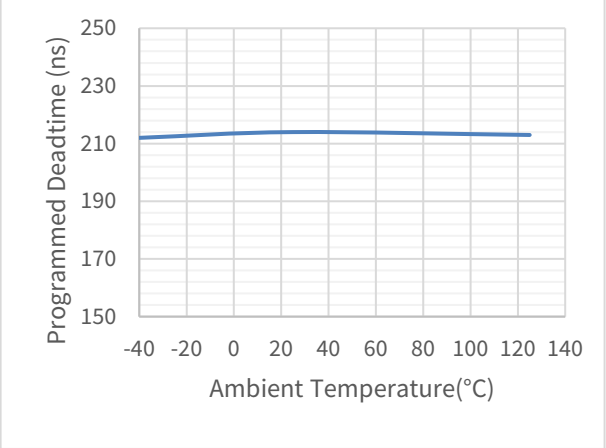

Figure 6.22 Deadtime (RDT=20kΩ) vs Temperature

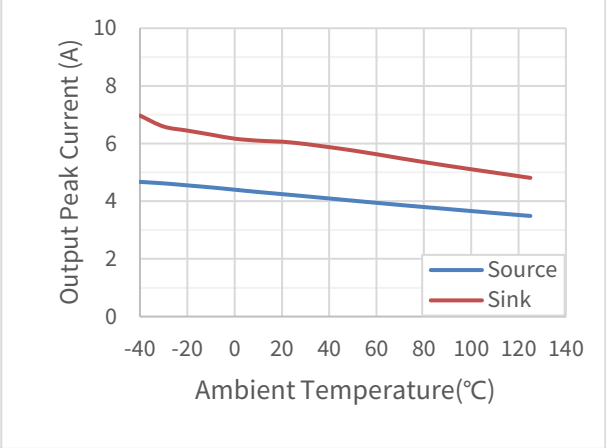

Figure 6.23 Output Peak Current vs Temperature

6.4. Parameter Measurement Information

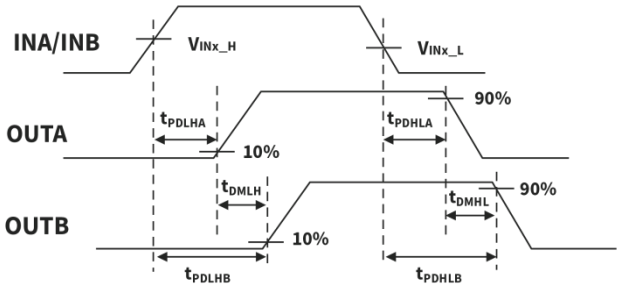

Figure 6.24 Propagation Delay and Channel to Channel Delay Match Time, connect DT to VDDI

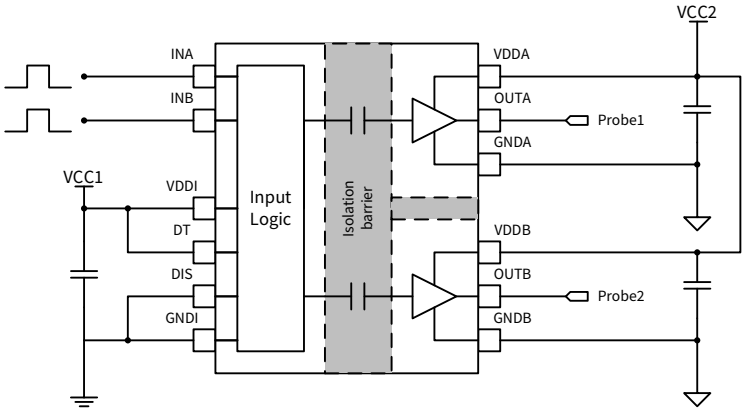

Figure 6.25 Channel to Channel Delay Match Test Circuit

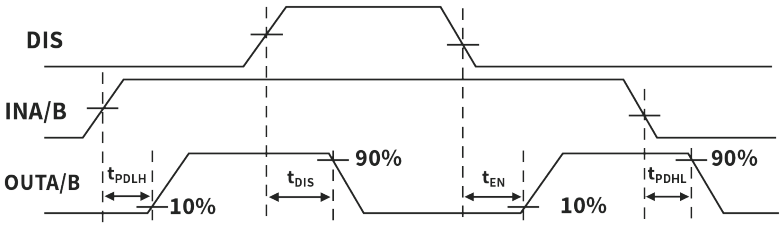

Figure 6.26 Disable Time and Enable Time

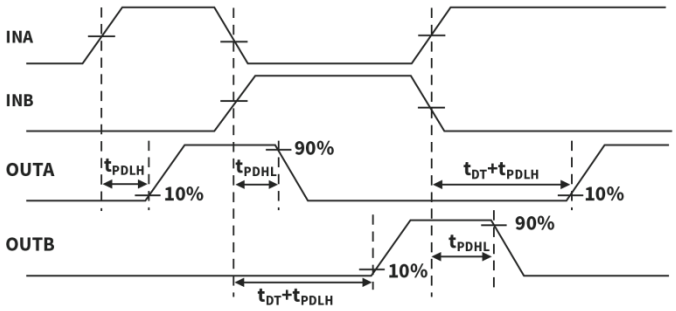

Figure 6.27 Deadtime, Determined by RDT

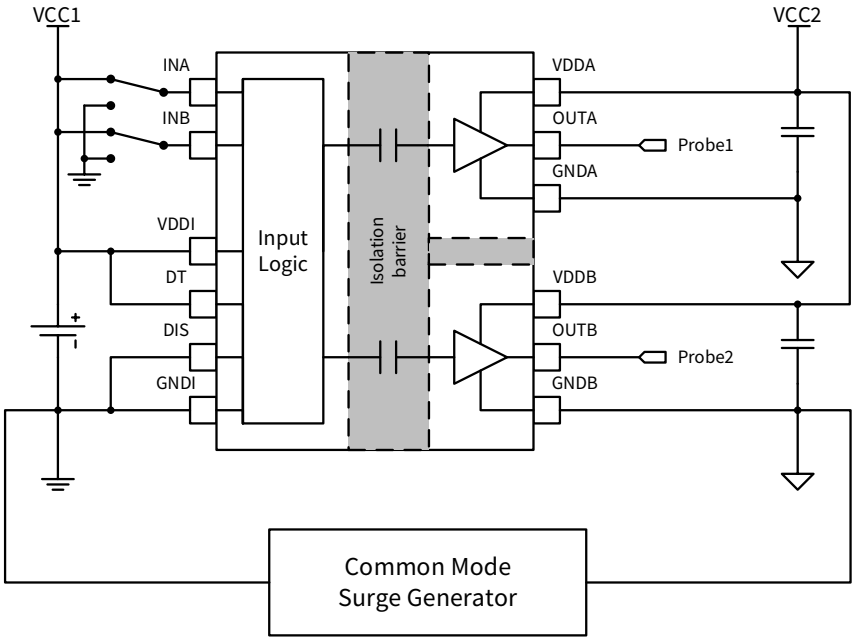

Figure 6.28 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation Characteristics

Description	Test Condition	Symbol	Value			Unit
			LGA 13	SOW16/14	SOP16	
Min. External Air Gap (Clearance)		CLR	3.5	8	4	mm
Min. External Tracking (Creepage)		CPG	3.5	8	4	mm
Distance through the Insulation		DTI	32			μm
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600			V
Material Group	IEC 60664-1		I			
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms		I to III	I to IV	I to IV	
	For Rated Mains Voltage ≤ 300Vrms		I to II	I to IV	I to III	
	For Rated Mains Voltage ≤ 600Vrms		I	I to IV	I to II	
	For Rated Mains Voltage ≤ 1000Vrms		/	I to III	/	
Climatic Category			40/125/21			
Pollution Degree	per DIN VDE 0110, Table 1		2			
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	560	1000	700	V_{RMS}
	DC voltage		792	1414	990	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	792	1414	990	V_{peak}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} =60s, $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s	q_{pd}	/	<5	/	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s, $V_{pd(m)}$=1.6*V_{IORM}, t_m=10s		/		/	pC
	Method b, routine test (100% production) and preconditioning (type test); V_{ini}=1.2*V_{IOTM}, t_{ini}=1s, $V_{pd(m)}$=1.875*V_{IORM},t_m=1s（method b1）or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)		/		/	pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} =60s, $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s	q_{pd}	<5	/	<5	pC