

FEATURES

- Maximizes Power Efficiency
- Eliminates Thermal Design Problems
- DC to 600Hz
- 9V to 72V Operating Voltage Range
- $I_Q = 1.5\text{mA}$ (Typical)
- Maximizes Available Voltage
- Available in 8-Lead (3mm × 3mm) DFN and 12-Lead MSOP Packages

APPLICATIONS

- Security Cameras
- Terrestrial or Airborne Power Distribution Systems
- Power-over-Ethernet Powered Device with a Secondary Input
- Polarity-Agnostic Power Input
- Diode Bridge Replacement

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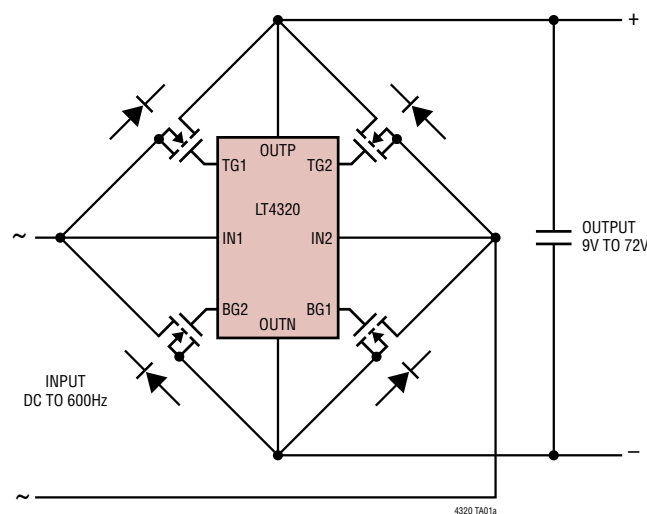
DESCRIPTION

The **LT[®]4320/LT4320-1** are ideal diode bridge controllers that drive four N-channel MOSFETs, supporting voltage rectification from DC to 600Hz. By maximizing available voltage and reducing power dissipation (see thermograph comparison below), the ideal diode bridge simplifies power supply design and reduces power supply cost, especially in low voltage applications.

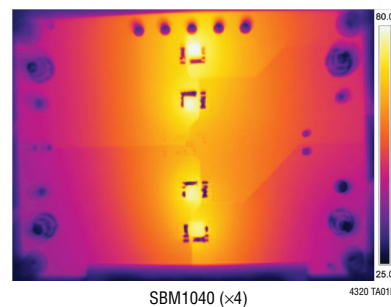
An ideal diode bridge also eliminates thermal design problems, costly heat sinks, and greatly reduces PC board area. The LT4320's internal charge pump supports an all-NMOS design, which eliminates larger and more costly PMOS switches. If the power source fails or is shorted, a fast turn-off minimizes reverse current transients.

The LT4320 is designed for DC to 60Hz voltage rectification, while the LT4320-1 is designed for DC to 600Hz voltage rectification. Higher frequencies of operation are possible depending on MOSFET size and operating load current.

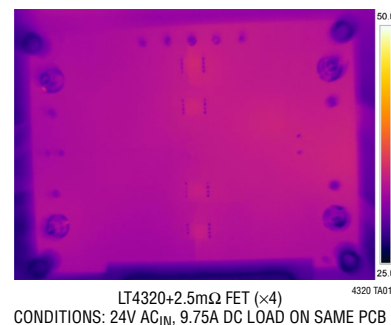
TYPICAL APPLICATION



Thermograph of Passive Diode Bridge



Thermograph of LT4320
Driving Four MOSFETs



Temperature Rise (°C)

CURRENT (A)	MOSFET 2.5mΩ	DIODE SBM 1040
2	0.6	15
4	3.5	32
6	6.7	49
8	11	66
10	16	84

DC Input, On Same PCB

LT4320/LT4320-1

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages

IN1, IN2..... -3V to 80V
OUTP -0.3V to 80V

Output Voltages (Note 3)

BG1, BG2, TG1, TG2..... -0.3V to 80V
TG1-IN1, TG2-IN2..... -0.3V to 12V

Operating Junction Temperature Range

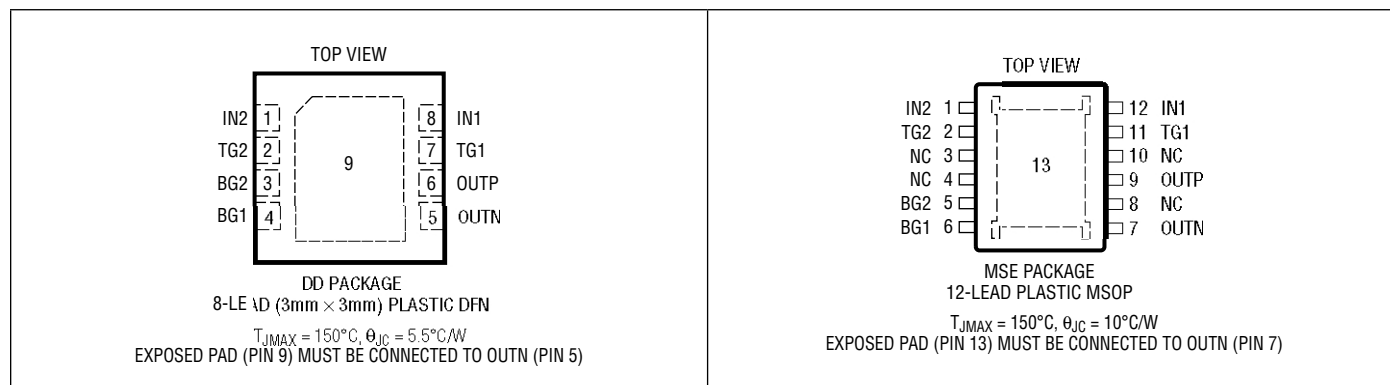
LT4320I..... -40°C to 85°C

Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10 sec)

MSE Package..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	OPERATING JUNCTION TEMPERATURE RANGE
LT4320IDD#PBF	LT4320IDD#TRPBF	LGCV	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LT4320IDD-1#PBF	LT4320IDD-1#TRPBF	LGCW	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LT4320IMSE#PBF	LT4320IMSE#TRPBF	4320	12-Lead Plastic MSOP	-40°C to 85°C
LT4320IMSE-1#PBF	LT4320IMSE-1#TRPBF	43201	12-Lead Plastic MSOP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 2)

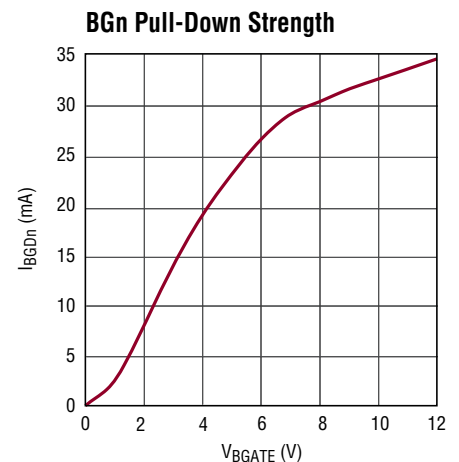
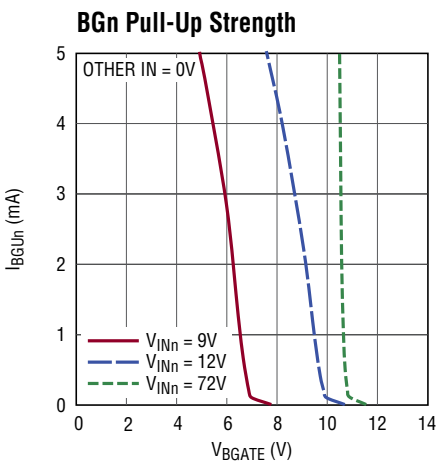
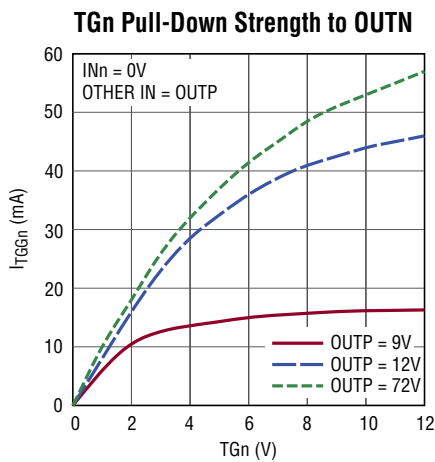
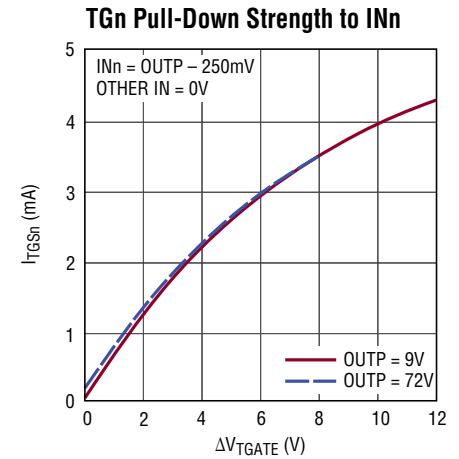
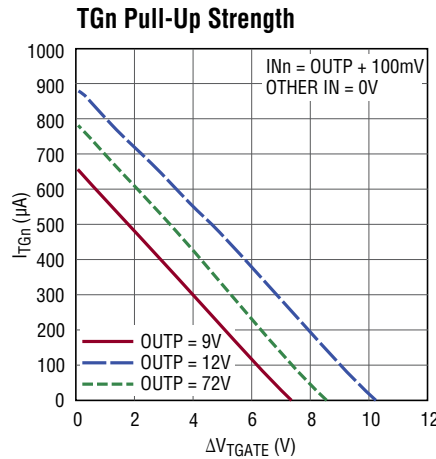
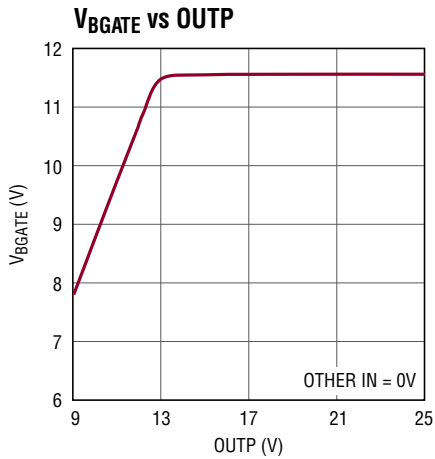
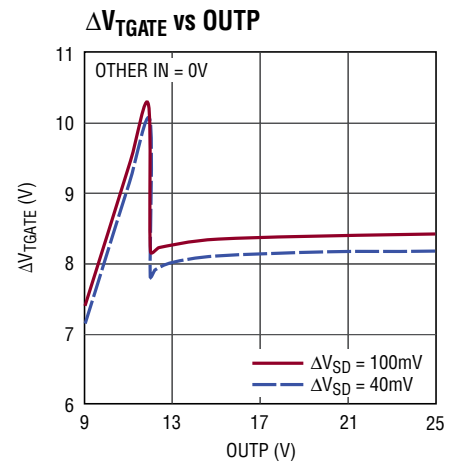
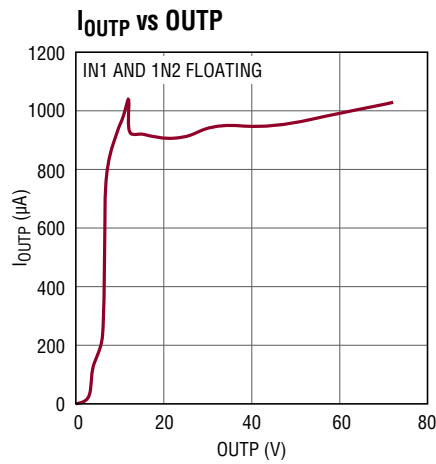
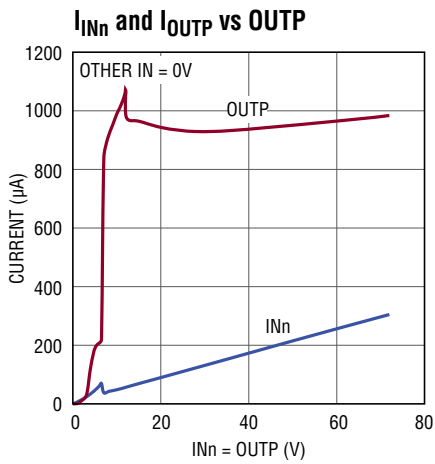
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	OUTP Voltage Range		●	9		72	V
	OUTP Undervoltage Lockout (UVLO) Threshold	INn = OUTP, Other IN = 0V	●	6.2	6.6	7.0	V
V_{INT}	INn Turn-On/Off Threshold	OUTP = 9V, Other IN = 0V	●	1.3		3.7	V
I_{OUTP}	OUTP Pin Current	INn = OUTP + $\Delta V_{SD(MAX)}$ + 5mV, Other IN = 0V	●		1.0	1.5	mA
I_{INn}	INn Pin Current at 9V at 72V	INn = OUTP + $\Delta V_{SD(MAX)}$ + 5mV, Other IN = 0V	● ●		44 0.3	63 0.4	μA mA
ΔV_{SD}	Topside Source-Drain Regulation Voltage (INn – OUTP) LT4320 LT4320-1		● ●	8 26	20 40	35 55	mV mV
ΔV_{TGATE}	Top Gate Drive (TGn – INn)	INn = OUTP + $\Delta V_{SD(MAX)}$ + 5mV, 10 μA Out of TGn, Other IN = 0V	●	6.6		10.8	V
V_{BGATE}	Bottom Gate Drive (BGn)	INn = OUTP, 10 μA Out of BGn, Other IN = 0V	●	7.0		12	V
I_{TGUn}	Top Gate Pull-Up Current	TGn – INn = 0V, INn = OUTP + 0.1V TGn – INn = 5V, INn = OUTP + 0.1V Current Flows Out of TGn, Other IN = 0V	● ●	425 120			μA μA
I_{TGSn}	Top Gate Pull-Down Current to INn	TGn – INn = 5V, INn = OUTP – 0.25V Current Flows Into TGn, Other IN = 0V	●	1.25			mA
I_{TGGn}	Top Gate Pull-Down Current to OUTN	INn = 0V, Other IN = OUTP = 9.0V, TGn = 5V Current Flows Into TGn	●	6.0			mA
I_{BGUn}	Bottom Gate Pull-Up Current	BGn = 5V; INn = OUTP = 9.0V, Other IN = 0V Current Flows Out of BGn	●	1.9			mA
I_{BGDn}	Bottom Gate Pull-Down Current	BGn = 5V; INn = 0V, Other IN = OUTP = 9.0V Current Flows Into BGn	●	12.5			mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Unless otherwise specified, exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are referenced to OUTN = 0V unless otherwise specified.

Note 3: Externally forced voltage absolute maximums. The LT4320 may exceed these limits during normal operation.

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS (DFN/MSOP)

IN2 (Pin 1/Pin 1): Bridge Rectifier Input. IN2 connects to the external NMOS transistors MTG2 source, MBG1 drain and the power input.

TG2 (Pin 2/Pin 2): Topside Gate Driver Output. TG2 pin drives MTG2 gate.

BG2 (Pin 3/Pin 5): Bottom-Side Gate Driver Output. BG2 pin drives MBG2 gate.

BG1 (Pin 4/Pin 6): Bottom-Side Gate Driver Output. BG1 pin drives MBG1 gate.

OUTN (Pin 5/Pin 7): OUTN is the rectified negative output voltage, and connects to the sources of MBG1 and MBG2.

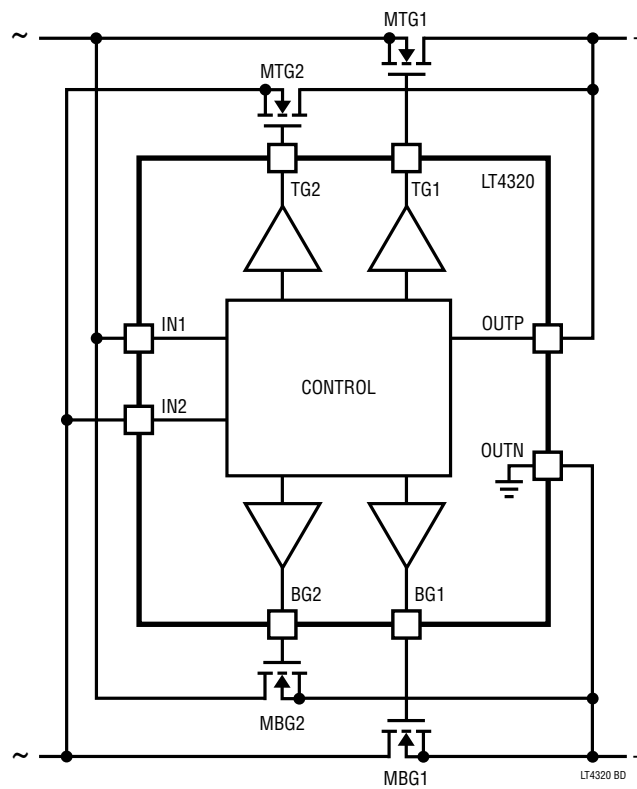
OUTP (Pin 6/Pin 9): OUTP is the rectified positive output voltage that powers the LT4320 and connects to the drains of MTG1 and MTG2.

TG1 (Pin 7/Pin 11): Topside Gate Driver Output. TG1 pin drives MTG1 gate.

IN1 (Pin 8/Pin 12): Bridge Rectifier Input. IN1 connects to the external NMOS transistors MTG1 source, MBG2 drain, and the power input.

NC (Pins 3, 4, 8, 10, MSOP Only): No Connections. Not internally connected.

Exposed Pad (Pin 9/Pin 13): Exposed Pad. Must be connected to OUTN.



OPERATION

Electronic systems that receive power from an AC power source or a DC polarity-agnostic power source often employ a 4-diode rectifier. The traditional diode bridge comes with an efficiency loss due to the voltage drop generated across two conducting diodes. The voltage drop reduces the available supply voltage and dissipates significant power especially in low voltage applications.

By maximizing available voltage and reducing power dissipation, the ideal diode bridge simplifies power supply design and reduces power supply cost. An ideal diode

bridge also eliminates thermal design problems, costly heat sinks, and greatly reduces PC board area.

The LT4320 is designed for DC to 60Hz voltage rectification, while the LT4320-1 is designed for DC to 600Hz voltage rectification. Higher frequencies of operation are possible depending on MOSFET size and operating load current.

Figure 2 presents sample waveforms illustrating the gate pins in an AC voltage rectification design.

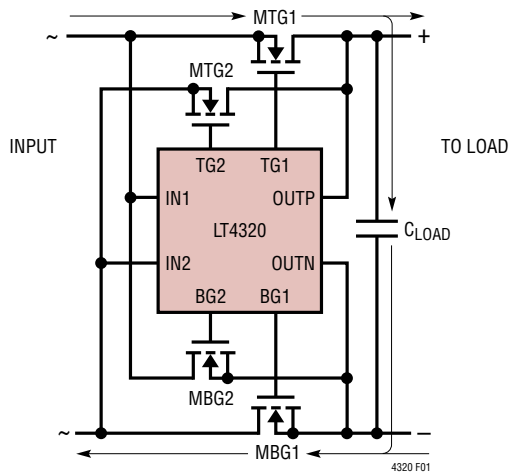


Figure 1. LT4320 with Four N-Channel MOSFETs, Illustrating Current Flow When IN1 Is Positive

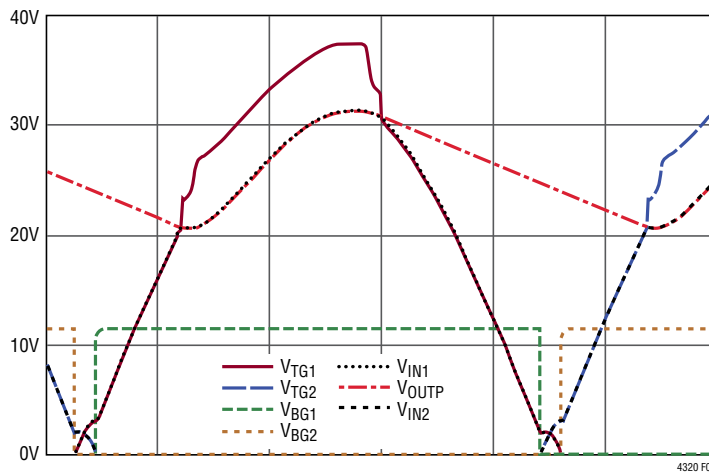


Figure 2. 24V AC Sample Waveform

APPLICATIONS INFORMATION

MOSFET Selection

A good starting point is to reduce the power dissipation of the ideal bridge to 1/10 that of a diode rectifier bridge. Given the average output load current, I_{AVG} , select $R_{DS(ON)}$ to be:

$$R_{DS(ON)} = \frac{70mV}{I_{AVG}} \text{ for a DC power input}$$

or

$$R_{DS(ON)} = \frac{70mV}{3 \cdot I_{AVG}} \text{ for an AC power input}$$

In the AC power input calculation, $3 \cdot I_{AVG}$ assumes the duration of current conduction occupies 1/3 of the AC period.

Select the maximum allowable drain-source voltage, V_{DSS} , to be higher than the maximum input voltage.

Design Example

For a 24W, 12V DC/24V AC application, $I_{AVG} = 2A$ for 12V DC. To cover the 12V DC case:

$$R_{DS(ON)} = \frac{70mV}{2A} = 35m\Omega$$

For the 24V AC operation, $I_{AVG} = 1A$. To cover the 24V AC case:

$$R_{DS(ON)} = \frac{70mV}{3 \cdot 1A} = 23m\Omega$$

This provides a starting range of $R_{DS(ON)}$ values to choose from.

Ensure the MOSFET can handle a continuous current of $3 \cdot I_{AVG}$ to cover the expected peak currents during AC rectification. That is, select $I_D \geq 3A$. Since a 24V AC waveform can reach 34V peak, select a MOSFET with $V_{DSS} \gg 34V$. A good choice of V_{DSS} is 60V in a 24V AC application.

Other Considerations in MOSFET Selection

Choose the lowest available total gate charge, Q_G , and correspondingly the lowest C_{ISS} , C_{OSS} , and C_{RSS} . Choosing a lower gate capacitance while meeting $R_{DS(ON)}$ speeds up the response time for full enhancement, regulation, turn-off, and input shorting events.

$V_{GS(th)}$ must be a minimum of 2V or higher. A gate threshold voltage lower than 2V is not recommended since too much time is needed to discharge the gate below the threshold and halt current conduction during a hot plug or input short event.

C_{LOAD} Selection

A 1 μ F ceramic and a 10 μ F minimum electrolytic capacitor must be placed across the OUTP and OUTN pins with the 1 μ F ceramic placed as close to the LT4320 as possible. Downstream power needs and voltage ripple tolerance determine how much additional capacitance between OUTP and OUTN is required. C_{LOAD} in the hundreds to thousands of microfarads is common.

A good starting point is selecting C_{LOAD} such that:

$$C_{LOAD} \geq I_{AVG} / (V_{RIPPLE} \cdot 2 \cdot \text{Freq})$$

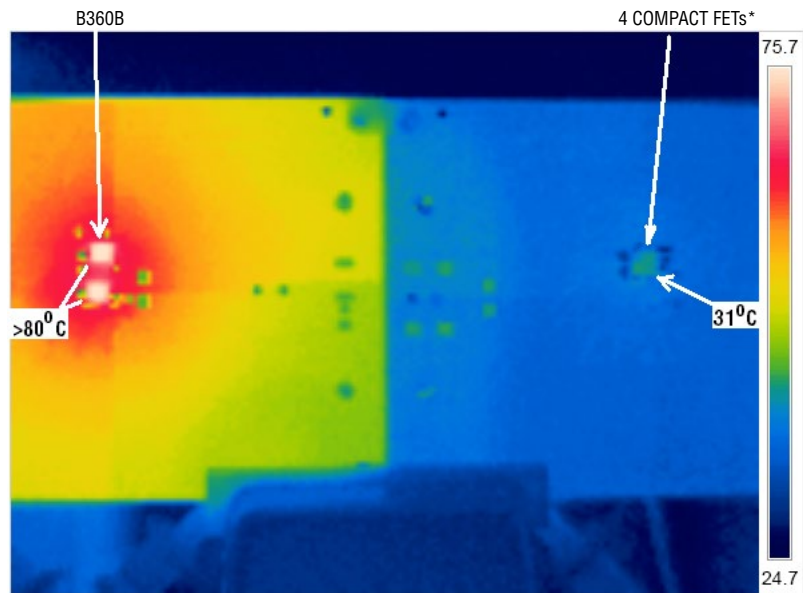
where I_{AVG} is the average output load current, V_{RIPPLE} is the maximum tolerable output ripple voltage, and Freq is the frequency of the input AC source. For example, in a 60Hz, 24VAC application where the load current is 1A and the tolerable ripple is 15V, choose $C_{LOAD} \geq 1A / (15V \cdot 2 \cdot 60Hz) = 556\mu F$.

C_{LOAD} must also be selected so that the rectified output voltage, OUTP-OUTN, must be within the LT4320/LT4320-1 specified OUTP voltage range.

Transient Voltage Suppressor

For applications that may encounter brief overvoltage events higher than the LT4320 absolute maximum rating, install a unidirectional transient voltage suppressor (TVS) between the OUTP and OUTN pins as close as possible to the LT4320.

TYPICAL APPLICATIONS



CONDITION: 13VDC_{IN} , 3A LOAD ON SAME PCB

*19m Ω , 60V EACH FET

Figure 3. Thermograph: B360B vs LT4320 +4 Compact FETs

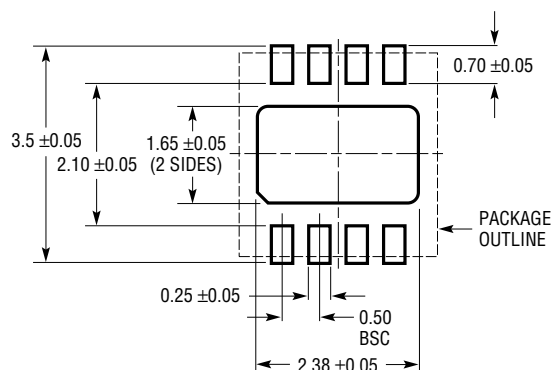


Figure 4. Demonstration Circuit 1902A Used in Figure 3 Thermograph

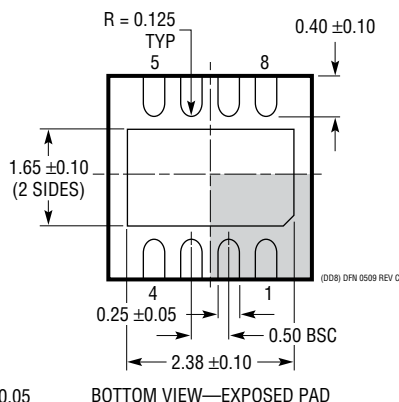
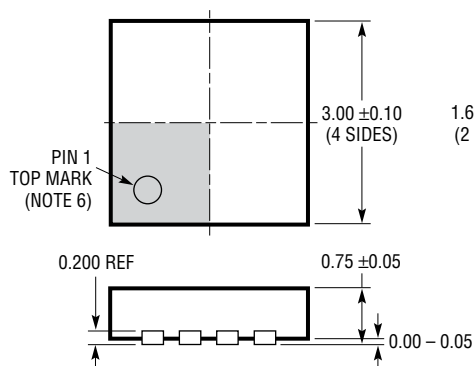
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

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