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# Part Ⅰ

# Electronic Technology

## Unit 1

### 1.1 Bipolar Junction Transistors

Today, industrial electronic systems employ several devices that are described by the term transistor. Each type of transistor has different characteristics and operational conditions that are used to distinguish it from others. In the first part of this discussion, we are concerned with the bipolar junction transistor. Structurally, this transistor is described as bipolar because it has two different current-carrier polarities. Holes are positive current carriers, whereas electrons are negative current carriers. Two distinct kinds of semiconductor crystals are connected together by a common element. The structure of this device is similar to that of two diodes connected back to back, with one crystal being common to both junctions. The center material is usually made thinner than the two outside pieces. Figure 1.1 shows the crystal structure, element names, and schematic symbols of two distinct types of bipolar transistors.

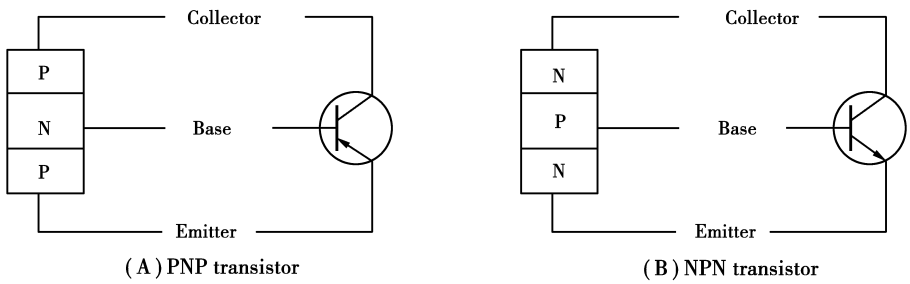



Fig. 1.1 PNP and NPN transistors

A bipolar transistor is primarily used as an amplifying device that regulates the amount

of current that passes through it. Current from the energy source enters the emitter, flows through the base region, and exits through the collector. Variations in collector current are usually identified as the output of a transistor. Collector current is controlled by a small change in base current. This relationship is described as current gain or beta. Expressed mathematically,

$$\text{Current gain} = \frac{\text{collector-current}}{\text{base-current}}$$

$$(\text{Beta}) = \frac{I_C}{\Delta I_B}$$

The Greek letter delta of this formula indicates a change value. This is used to denote the response of a transistor when ac values are applied. Conditions of this type are called dynamic characteristics. Omission of the delta sign in a formula denotes dc or static operating conditions.

All the current entering a transistor at the emitter is identified as emitter current, or $I_E$. The collector current, or $I_C$, is always somewhat less than $I_E$. The difference between $I_E$ and $I_C$ is due to base current. Mathematically, this is base current ($I_B$) = emitter current − collector current

$$I_B = I_E - I_C$$

Example 1-1: Determine the base current of a bipolar transistor with an $I_E$ of 11 mA and an $I_C$ of 10.95 mA.

Solution:

$$I_B = I_E - I_C = 11\ \text{mA} - 10.95\ \text{mA} = 0.05\ \text{mA or } 0.05 \times 10^{-3}\text{A}$$

Fig. 1.2 shows the circuit connections of a simple NPN silicon transistor. Operation of this circuit is based on a forward-biased emitter-base junction and a reverse-biased collector. Forward biasing of the emitter-base junction is accomplished by connecting the negative side of the dc source to the emitter and the positive side through $R_B$ to the base. Reverse biasing of the collector occurs when it is connected to the positive side of the source through resistor $R_L$. Collector current through $R_L$ is controlled by the forward-bias voltage of the emitter-base junction.

In the operation of a single PN diode junction, forward biasing causes conduction and reverse biasing causes nonconduction. In a transistor, this rule does not apply directly because two junctions are involved. For example, when the emitter-base junction is forward biased, it causes a large amount of $I_E$ to enter the base region. Reverse biasing of the base-collector junction would ordinarily restrict this current. But due to the thin base structure, $I_E$ will immediately enter into the collector when it reaches the base area. Ultimately, this current passes through the collector and appears as collector current $I_C$ or output current. Forward biasing of the emitter-base junction therefore alters or reduces the reverse biasing effect of the base-collector junction in normal transistor operation.

A transistor is primarily classified as a current-operating device. This means that the

output or collector $I_C$ will occur only when the emitter-base junction is forward biased and producing base current. When the base current ceases, collector current stops and the transistor become nonconductive. This condition is called *cut off* on the other hand, if an excessive amount of base current occurs, the transistor is driven into *saturation*. When this condition occurs, a further increase in $I_B$ will not cause a corresponding change in $I_C$. When amplitude control is being achieved, a transistor is rarely operated in the saturation region. When a transistor is used as a switch, it usually operates in the saturation region.

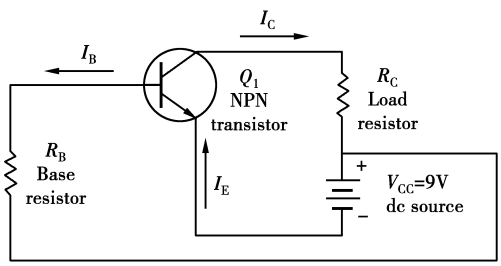



Fig. 1.2 NPN transistor circuits

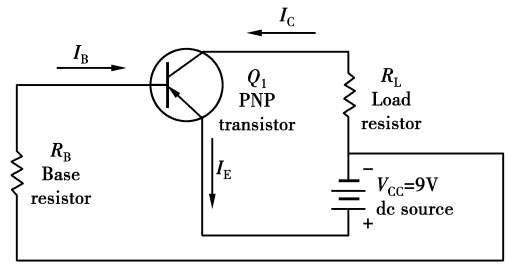



Fig. 1.3 PNP transistor circuits

The transistor amplifier circuit of Figure 1.3 is a PNP counterpart of the previous NPN circuit. The battery of this circuit is connected in a reverse direction in order to achieve proper biasing. Performance is basically the same as that of the NPN circuit. Currents $I_C$, $I_B$, and $I_E$ are represented in this diagram by arrows. The emitter current of this circuit still provides the largest current value. The composite of $I_C$ plus $I_B$ also equals $I_E$ in this circuit.

**WORDS AND TERMS**

bipolar *a.* 双极的,双向的
carrier *n.* 载流子
polarity *n.* 极性
positive *a.* 正的,(电)阳性的
negative *a.* 负的,(电)阴性的
semiconductor *n.* 半导体
crystal *n.* 结晶,晶体,晶粒
symbol *n.* 符号,记号,象征
emitter *n.* 发射极
collector *n.* 集电极
current gain *n.* 电流增益
base *n.* 基极
beta *n.* 希腊字母 "$\beta$"
Greek *a.* 希腊的,希腊语的
delta *n.* 希腊字母"$\Delta,\delta$"
denote *v.* 表示,意味着
formula(*pl.* -s 或 formulae)*n.* 公式
forward-biased 正偏置的,正偏压的
reverse-biased 反偏置的,反偏压的

## 1.2 UJT Thyristors and SCRs

The term thyristor refers to a rather general classification of solid-state devices that are used as electronic switches. Thyristors can be two-, three-, or four-terminal devices. In this section we are concerned with the conductivity capabilities of these devices. Devices placed in this classification operate through a type of regenerative feedback. When conduction is initiated, the device will latch or hold in its *on state*. Momentarily removing or reducing the energy level of the source will cause nonconduction or switching to the *off state*. In general,

a unidirectional thyristor is classified as a voltage-controlled switch.

Thyristors should not be confused with bipolar junction transistors or field-effect transistors. BJTs and FETs are both capable of performing switching operations. As a rule, these devices are not as efficient as a thyristor and do not have the power-handling capability. Thyristors are used as power control devices, whereas transistors are primarily used in amplifying applications.

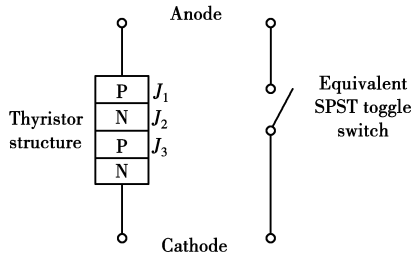
A variety of unidirectional thyristors is now being used in industrial electronic applications. One of the first to be developed was the silicon-controlled rectifier (SCR). The SCR was designed as a solid-state counterpart of the thyratron gaseous tube. The term thyristor was derived from the words thyratron-transistor. An SCR is classified as a reverse blocking triode thyristor. This means that the device has conductivity in only one direction. When its anode and cathode are reverse biased, the device will not conduct. The silicon-controlled switch (SCS) and the programmable unijunction transistor (PUT) are two other thyristors of this classification. A Shockley diode is classified as a reverse blocking diode thyristor.

The crystal structure of a thyristor is unique when compared with other solid-state devices. Most thyristors are classified as PNPN devices. This type of structure consists of four alternately doped semiconductor layers and three PN junctions. The number of terminals attached to the structure is based on the function of the device. The two outer terminals are usually called the anode and cathode. Conduction between these two terminals is the same in nearly all thyristors.

The basic structure of a four-layer thyristor is shown in Figure 1.4. Notice that the anode terminal is connected to the P region on one end of the structure. The cathode is connected to the N region on the other end. Three junctions are formed between the top and bottom terminals. Conduction between the anode-cathode is similar to that of a mechanical toggle switch. This means that the device must have two operational states. In its on state the three junctions are low resistant. The off state has an infinite resistance between the anode-cathode.

A unique feature of the thyristor structure is its latching characteristic. Latching refers to a condition that holds the device in its on state after conduction has been initiated. Removal of the original actuating signal does not necessarily cause conduction to stop. This action permits the thyristor to be used as an electronic switching device. When the device has been triggered, it usually takes a different procedure for it to be turned off. Switching techniques vary a great deal in thyristors. Diode thyristors change states due to a change in anode-cathode voltage. State changes in a three-element device are initiated by an independent triggering signal.

Description of the operation of a basic PNPN thyristor is often simplified by the two-transistor anology. This method divides the PNPN structure into two imaginary transistors. Junctions $J_1$ and $J_2$ form a PNP transistor, while $J_2$ and $J_3$ form an NPN device. The $J_2$



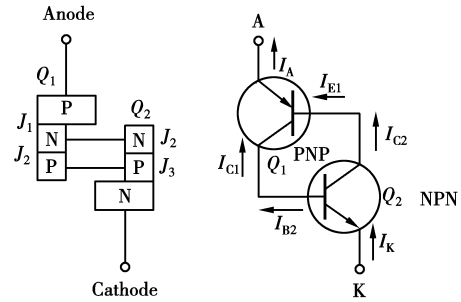




Fig. 1.4 Four-layer thyristor structure Fig. 1.5 Two-transistor equivalent of a PNPN structure

junction is common to both transistor structures. See the two-transistor equivalent of the PNPN structure in Figure 1.5. Note also the schematic symbol representation of the same structure.

Assume now that a thyristor is connected to an energy source and a load resistor. Figure 1.6 (A) shows the positive side of the source connected through $R_L$ to the anode and the negative side to the cathode. Connected in this manner, junctions $J_1$ and $J_3$ are forward biased and $J_2$ is reverse biased. This means that $J_2$ will have an infinite resistance, while $J_1$ and $J_3$ are low resistant. $J_2$ will therefore have practically all of $V_S$ appearing across it, while $J_1$ and $J_3$ will have zero voltage. Very little current will flow through the structure. This means that $I_A = I_K$ with a current value of approximately zero. This condition will exist as long as $V_{AK}$ is below the breakdown voltage of $J_2$ junction.

Refer now to the two-transistor analogy of the thyristor structure in Figure 1.6 (B). Connected in this manner, the emitter-base (E-B) junctions of $Q_1$ and $Q_2$ are both slightly forward biased by the source. The E-B junction of $Q_1$ is the equivalent of $J_1$, and E-B of $Q_2$ is representative of $J_3$. The $J_2$ junction is equivalent to the collection-base (C-B) junctions of both $Q_1$ and $Q_2$. These two junctions are both reverse biased. Connected in this manner, the two transistors are properly biased for conduction. However, the two E-B junctions have practically no forward bias voltage. This will permit very little or practically no current to flow through the structure. A thyristor connected in this manner is considered to be in its off or nonconductive state.

Note the element current designations for the two-transistor equivalent circuit of Figure 1.6 (B). The emitter current of $Q_1$ is representative of the anode current ($I_A$). $I_{B1}$ is indicative of the base current of $Q_1$. $I_{B1}$ is determined by the expression

$$I_{B1} = (1-\alpha_1)\, I_A - I_{CBO1}$$

where $\alpha_1$ = current gain of $Q_1$

$I_A = I_{E1}$

$I_{CBO1}$ = collector-emitter leakage current of $Q_1$

For transistor $Q_2$, the emitter current $I_{E2}$ is equal to the cathode current ($I_K$). The base current of $Q_2$ is designated as $I_{B2}$. The collector current of $Q_1$ is equal in value to the base current of $Q_2$. $I_{C1}$ therefore equals $I_{B2}$. The collector current ($I_{C2}$) can be determined by the

formula

$$I_{C2} = (\alpha_2) + I_{CBO2}$$

where $\alpha_2$ = current gain of $Q_2$

$$I_K = I_{E2}$$

$I_{CBO2}$ = collector-emitter leakage current of $Q_2$

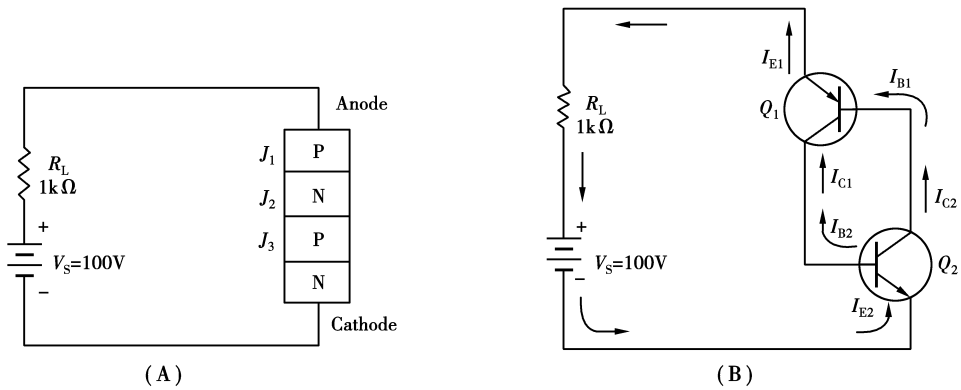



Fig. 1.6 Thyristor connected to an energy source

Note that $I_{C2}$ of $Q_2$ and $I_{B1}$ of $Q_1$ are of the same value. This permits the two previous expressions to be equated. The combined expression then becomes

$$I_{B1} = I_{C2}$$

or

$$(1-\alpha_1)\ I_A - I_{CBO2} = (\alpha_2)\ I_K + I_{CBO2}$$

Combining the two expressions permits us to solve for either $I_A$ or $I_K$. This is given by the formula

$$I_A \text{ or } I_K = \frac{I_{CBO1} + I_{CBO2}}{1-(\alpha_1 Q_1 + \alpha_2 Q_2)}$$

The combined $I_A = I_K$ expression is an extremely important concept in the operation of all thyristors. We will use this expression to show how a thyristor responds in its nonconductive state. A small modification of the alpha values will cause a thyristor to change into its conductive state.

**WORDS AND TERMS**

UJT [unijunction transistor] 单结晶体管
thyristor *n.* 半导体开关元件,晶闸管(闸流晶体管),可控硅整流器
SCR [selicon controlled rectifier] 可控硅(半导体可控硅整流器)
gaseous *a.* 气体的,气态的
blocking *n.* 封锁,阻断,中断
triode *n.* [无]三极管
FET (field effect transistor) 场效应晶体管
counterpart *n.* 对应物,配对物,副本
thyratron *n.* [无]闸流管
term *n.* 术语,学期,期间,项
terminal *n.* 端子,接头,引线
conductivity *n.* 导电性,电导率

anode *n*. 阳极，正极
cathode *n*. 阴极，负极
doped *a*. 掺杂质的
removal *n*. 移动，排除，除去
trigger *n*. 触发器，触发脉冲，启动装置
classification *n*. 分类，分级，等级，类别
regenerative *a*. 再生的，新生的，反馈的
feedback *n*. [无] 反馈
initiate *v*. 启动，开始
latch *v*. 封锁

### 1.3 专业英语概述

随着科学技术的飞速发展，科技用语、专业词汇、专用语汇和词汇、日常用语和词汇在科技语言环境中的特殊含义等等，必然大量出现在各个专业的英语话语和书刊中，形成一种与基础英语、日常生活英语有很大差别的英语语言，这就是科技英语。科技英语又因为各个不同的专业而形成很多小的门类，如医学专业英语、建筑专业英语、电子专业英语等等。本书要讲述的是自动化专业英语的一些特点和要点。

根据现行的教学大纲，大学生进入三年级后便开始开设专业英语课程。学习专业英语需要具备两个基础条件，一是较为扎实的英语基础，基本掌握英语常用语法和 4 000 以上的词汇量；二是一定程度的本学科专业知识技能。掌握专业英语技能是大学基础英语学习的主要目的之一，专业英文资料的阅读与翻译能力直接关系到学生的求职和毕业后的工作能力。随着国际间科学技术交流的日益扩大，互联网的进一步应用和发展，专业英语必然拥有更为重要的意义并受到更多的重视。

与基础英语相比，专业英语有着许多受本专业影响的词语特征以及与日常用语迥然不同的独特的含义，如：

The boot is a small routine. Generally, the boot is stored on the first sector (or two) of a disk.

（错误译法）靴子是一个小的日常工作。一般来说，靴子储藏在唱片的第一（或第一，二）个地段上。

（正确译法）引导程序是一小段程序。一般来说，引导程序存放在磁盘的第一（或第一，二）个扇区上。

所以，不能因为基础英语水平较高就忽视专业英语的学习，仅靠日常用语进行望文生义的理解不仅会闹笑话，甚至有可能造成事故。

同时，专业英语在结构上有三多，长句多、被动语态多、名词化结构多，这些会给理解和翻译带来很多困难；由于涉及许多科技内容和专业知识，专业英语往往极其复杂深奥，艰涩难懂。所以，只有在努力学好专业知识的前提下，再经过刻苦的专业英语训练，才能完成从基础英语到专业英语的过渡，达到英语学以致用的目的。

在听说读写译方面，专业英语侧重于“读”和“译”，要求通过大量的阅读达到对原文的正确理解和翻译，在读和译的基础上，对听、说、写进行必要的训练；由于专业英语的翻译经常直接应用于科研工作或工程技术，因而对“译”的质量具有更高的要求，如果翻译上失之毫厘，科研或工程中就可能谬以千里，造成极大的损失。

专业英语是十分重要、不可或缺的课程之一，学好专业英语将会获益终生。

# Unit 2

## 2.1 Operational Amplifiers

The internal construction of an op-amp is quite complex and usually contains a large number of discrete components. A person working with an op-amp does not ordinarily need to be concerned with its internal construction. It is helpful, however, to have some general understanding of what the internal circuitry accomplishes. This permits the user to see how the device performs and indicates some of its limitations as a functioning unit.

The internal circuitry of an op-amp can be divided into three functional units. Figure 1.7 shows a simplified diagram of the internal functions or an op-amp. Notice that each function is enclosed in a triangle. Electronic schematics use the triangle to denote the amplification function. This diagram shows that the op-amp has three basic amplification functions. These functions are generally called stages of amplification. A stage of amplification contains one or more active devices and all the associated components needed to achieve amplification.

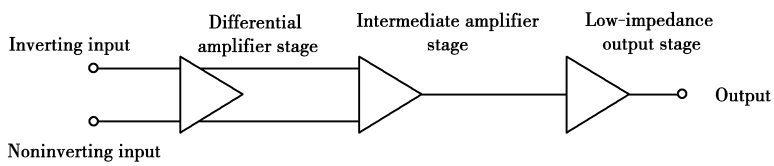



Fig. 1.7 Op-amp diagram

The first stage or input of an op-amp is usually a differential amplifier. This amplifier has two inputs, which are labeled $V_1$ and $V_2$. It provides high gain of the signal difference supplied to the two inputs and low gain for common signals applied to both inputs simultaneously. The input impedance is high to any applied signal. The output of the amplifier is generally two signals of equal amplitude and 180° out of phase. This could be described as a push-pull input and output.

One or more intermediate stages of amplification follow the differential amplifier. Figure 1.7 shows an op-amp with only one intermediate stage. Functionally, this amplifier is designed to shift the operating point to a zero level at the output and has high current and voltage gain capabilities. Increased gain is needed to drive the output stage without loading down the input. The intermediate stage generally has two inputs and a single-ended output.

The output stage of an op-amp has a rather low output impedance and is responsible for developing the current needed to drive an external load. Its input impedance must be great enough that it does not load down the output of the intermediate amplifier. The output stage can be an emitter-follower amplifier or two transistors connected in a complementary-symmetry configuration. Voltage gain is rather low in this stage with a sizable amount of

current gain.

A differential amplifier is the key or operational basis of most op-amps. This amplifier is best described as having two identical or balanced transistors sharing a single emitter resistor. Each transistor has an input and an output. A schematic diagram of a simplified differential amplifier is shown in Figure 1.8. Notice that the circuit is energized by a dual-polarity or split-power supply. The source leads are labeled $+V_{CC}$ and $-V_{CC}$ and measured with respect to a common ground lead.

Operation of a differential amplifier is based on its response to input signals applied to the base. Grounding one base and applying an input signal to the other base produces two output signals. These signals have the same amplitude but are inverted 180°. This type of input causes the amplifier to respond in its differential mode of operation.

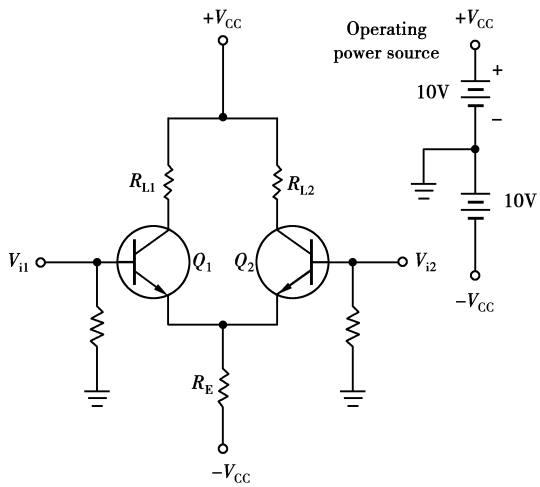



Fig. 1.8 Simplified differential amplifier

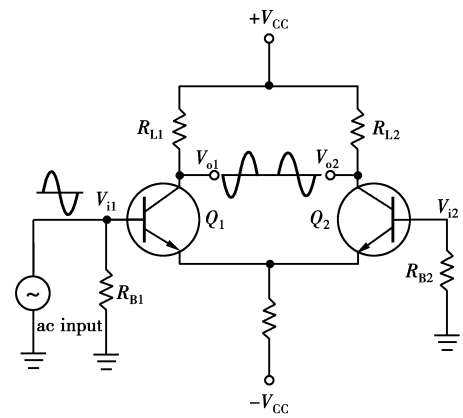



Fig. 1.9 AC differential amplifier

When two signals of equal amplitude and polarity are applied to each base at the same time, the resulting output is zero. This type of input causes a difference or canceling voltage to appear across the commonly connected emitter resistor. In a sense, the differential amplifier responds as a balanced bridge to identical input signals. There is no output when the circuit is balanced and output when it is unbalanced. This is called the common-mode condition of operation. A differential amplifier is designed to reject signals common to both inputs. The term common-mode rejection ratio (CMRR) is used to describe this action of the amplifier. CMRR is a unique characteristic of the differential amplifier. Undesirable noise, interference, or ac hum can be rejected by this operating condition.

Figure 1.9 shows a simplified schematic of a differential amplifier connected for differential mode operation. In this circuit an input signal is applied to the base of $Q_1$, and the base of $Q_2$ is left open or in a floating state. This condition causes signals to be developed at both outputs and across the emitter resistor. The emitter signal, as indicated, is in phase with the input. The two output signals are out of phase with each other and have a

substantial degree of amplification. Output $V_{o1}$ is out of phase with the input and $V_{o2}$ is in phase.

A differential amplifier will produce two output signals when only one input signal is applied. Coupling of the input signal from $Q_1$ to $Q_2$ is accomplished through the emitter resistor. The positive alternation of the input signal, for example, causes increased forward bias of $Q_1$. This causes an increase in the conduction of $Q_1$. With more $I_E$, there is a greater voltage developed across the emitter resistor. This in turn causes both emitters to be less negative. The conduction of $Q_1$ is not appreciably influenced by this voltage because it has an external signal applied to its input. $Q_2$ is, however, directly influenced by the reduced negative voltage to its emitter. This causes the conduction of $Q_2$ to be reduced. A reduction in current through $Q_2$ causes less voltage drop across $R_{L2}$ and the collector voltage to swing in the positive direction. In effect, an input signal applied to the base of $Q_1$ reduces the $V_E$ of $Q_2$, which in turn increases the value of the output voltage $V_{o2}$, An input signal is therefore coupled to $Q_2$ by the commonly connected emitter resistor.

The negative alternation of the input signal causes a reversal of the action just described. $Q_1$, for example, will be less conductive and $Q_2$ will have increased conduction. This action causes a reduction of $I_C$ through $Q_1$ and an increase swing in the value of $V_{o1}$. Increased conduction of $Q_2$ causes a corresponding reduction in $V_{o2}$. The two output signals continue to be 180° out of phase. In effect, both alternations of the input appear in the output. A differential amplifier connected in the differential mode will develop two output signals that are reflective of the entire input signal.

Differential amplifiers respond in primarily the same way when the inputs are reversed. In this case, an input signal is applied to the base of $Q_2$ with the base of $Q_1$ open or floating. $V_{o2}$ is out of phase with the input and $V_{o1}$ is in phase. The amplitude or output signal level of the amplifier is still based on the signal difference between the two inputs. With only one signal applied to the input at a time, the amplifier sees a very large differential input and develops a sizable output voltage.

The differential amplifier of Figure 1.9 is rarely used in op-amp construction today. Ordinarily, the resistance of $R_E$ needs to be quite large in order to have good coupling and common-mode rejection capabilities. Large resistance values are rather difficult to fabricate in IC construction. $R_E$ can, however, be replaced with a transistor. This transistor and its associated components are called a constant-current source.

**WORDS AND TERMS**

op-amp (operational amplifiers) *n.* 运算放大器
triangle *n.* 三角形
differential amplifier 差动放大器
impedance *n.* 阻抗
push-pull *a.* 推挽(式)的
dual-polarity *n.* 双极(性)
invert *v.* 反向,反转
common-mode rejection ratio (CMRR) *n.* 共模抑制比率
substantial *a.* 大的,大量的,物质的

intermediate *a*. 中间的
single-ended *a*. 单端的，单向的
emitter-follower amplifier *n*. 射极跟随放大器
complementary-symmetry *a*. 互补对称的
couple *v*. 耦合，结合
reversal *v*. 反向，反转，换相
resistance *n*. 电阻
constant-current source *n*. 恒流源

## 2.2 Single-phase Rectification

The simplest system for converting alternating current to direct current is single-phase rectification. A single-phase rectifier changes alternating current to pulsating direct current. This process can be accomplished by using either semiconductors, vacuum tubes, gaseous tubes, or rotary converters. The most common and economical method in industry today is the use of low-cost silicon rectifiers. Since semiconductors are so prevalent in industry today, it is desirable to review the action of a semiconductor diode before we look at specific rectifier circuits.

We know that certain materials (conductors) conduct electrical current easily and other materials (insulators) do not. Between these two extremes are other materials that are neither good conductors nor good insulators. These materials, such as silicon and germanium, have characteristics between those of conductors and insulators.

Silicon and germanium are crystalline materials whose electrical characteristics can easily be altered in the manufacturing process. Elements called impurities are added to pure silicon or germanium to form either N-type or P-type materials. These materials are used in various combinations to form many types of semiconductors, such as diodes, transistors, silicon-controlled rectifiers, triacs, and diacs. An N-type material possesses an abundance of electrons or negative charge carriers that do not take pat in covalent bonding. A P-type material has an excess of positive charge carriers or holes that are not influenced by covalent bonding. By controlling the impurities added to silicon, these conditions can be altered.

The most basic semiconductor device is the diode, which performs the function of rectification. A diode is merely a PN junction device formed by adjacent P-and N-type materials, as shown in Figure 1.10(A). The junction formed by the adjacent P-and N-type materials allows current to pass in one direction but offers a high resistance to current in the other direction. This device is called a junction diode. Some PN junction diodes are shown in Figure 1.10(C).

The current carriers of a PN junction diode are in a state of equilibrium when an external potential is not applied. It is possible that, due to temperature, some electrons will cross the junction from the N-type region to the P-type region. Likewise, some holes will diffuse from the P-type region to the N-type region. After this diffusion has taken place, an electrical barrier is developed between the two regions. Thus the further movement of charge carriers is prohibited and the diode is in a state of equilibrium.

In an electronic power supply, diodes are connected to an ac source of electrical energy. The instantaneous polarity of the potential connected to each terminal of the diode determines

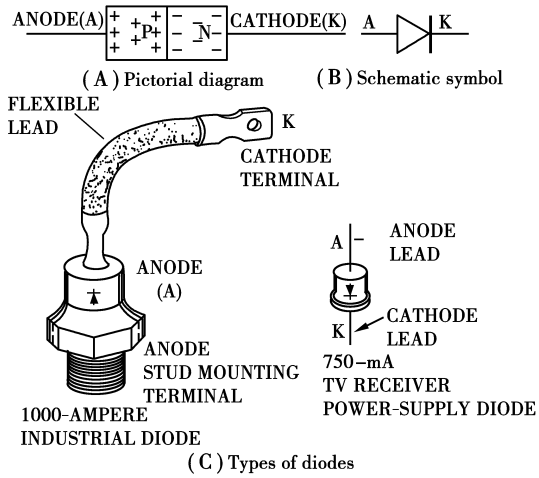



Fig. 1.10 PN junction diodes

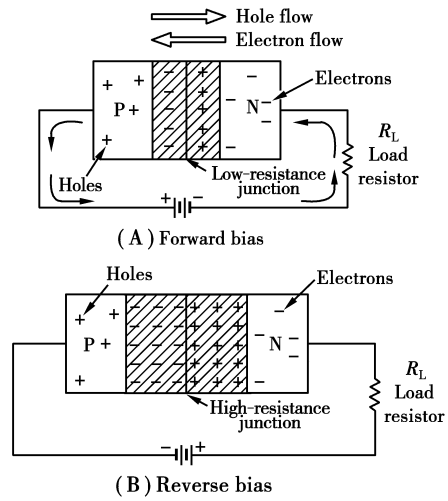



Fig. 1.11 Forward and reverse bias of a PN junction diode

the action performed by the diode. To best see the basic operation of a rectifier, a simple dc circuit is connected to a silicon diode. Figure 1.11 shows a battery used as the energy source and a resistor as the load device. The polarity of the battery is used to bias the diode.

With the positive battery terminal connected to the P-type material and the negative battery terminal connected to the N-type material, the diode is said to be forward biased. During forward bias, as shown in Figure 1.11(A), a low-resistance PN junction is developed. The low-resistance junction permits electrons in the N-type material to drift into the P region since they are attracted by the positive terminal of the battery. Likewise, holes drift in the opposite direction into the N region since they are attracted by the negative battery terminal. The continuous movement of electrons and holes constitutes an electrical current when a diode is forward biased.

If we reverse the battery polarity, as shown in Figure 1.11(B), the diode is said to be reverse biased. Electrons in the N-type material are pulled away from the junction by the positive battery terminal, and holes are drawn away from the junction by the negative terminal of the battery. The area near the junction develops an electrical barrier that blocks the movement of charge carriers. Only a very slight current, which is barely measurable, flows in the reverse-biased condition. Since the PN diode conducts while forward biased and does not conduct while reverse biased, it exhibits the properties of a rectifier.

A single-phase, half wave rectifier circuit, shown in Figure 1.12, converts an alternating current into a pulsating direct current. Let us assume that during the positive alternation of the ac cycle the anode of the diode is positive. The diode will then conduct since it is forward biased and the junction resistance is low. The positive alternation of the ac will then appear across the load device (represented by a resistor).

During the negative alteration of the ac cycle, the anode of the diode becomes negative.

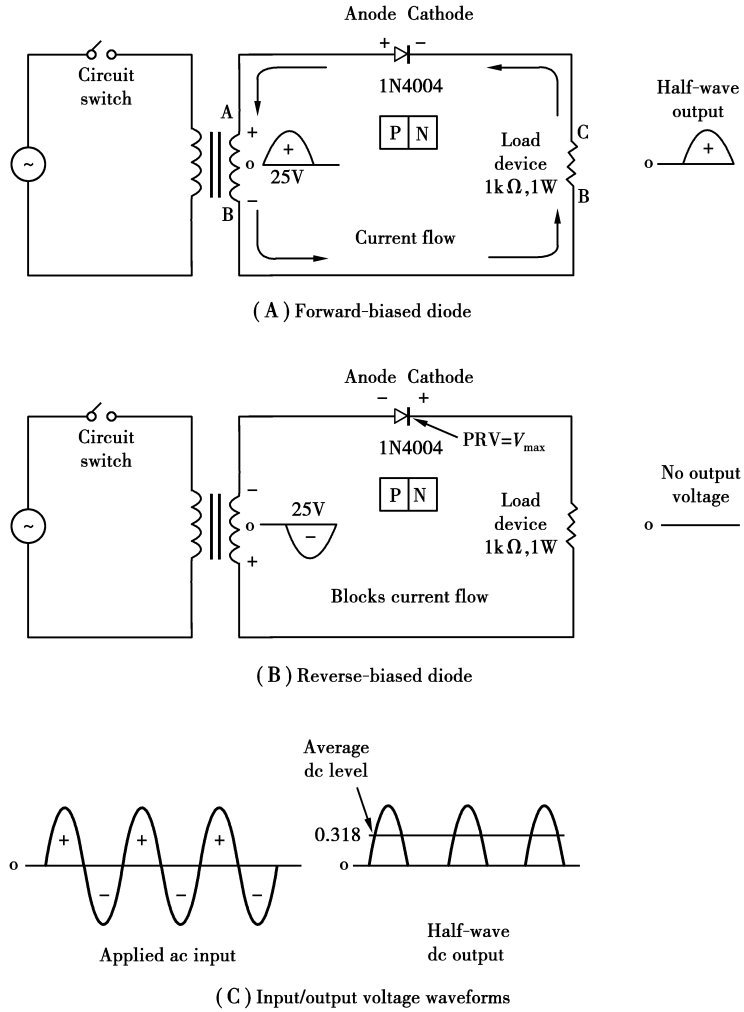



Fig. 1.12 Single-phase, half-wave rectifier circuit

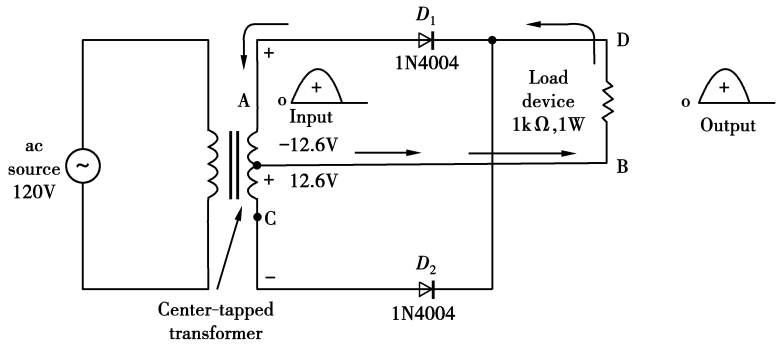
The diode is now reverse biased and no significant current will flow through the load device. Therefore, no voltage will appear across the load. The input and resulting output waveforms of the half wave rectifier circuit are shown in Figure 1.12 (C). The pulsating direct current of the output has an average dc level. The average value of the pulsating dc produced by single-phase, half wave rectification is expressed as

$$V_{dc}=0.318\times V_{max}$$

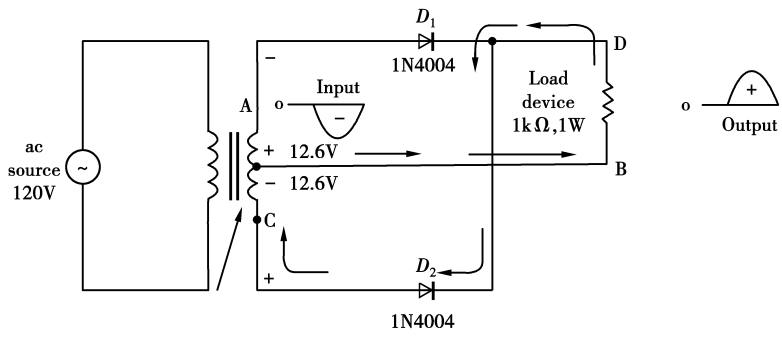
where $V_{dc}$ = average value of rectified voltage

$V_{max}$ = peak (maximum) value of applied ac voltage

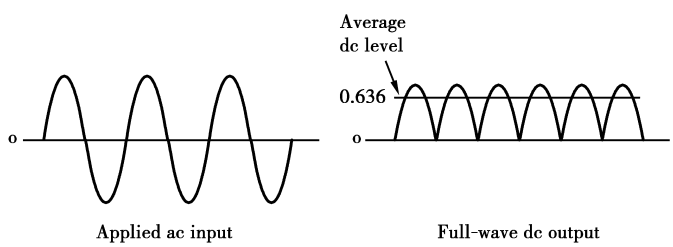
Certain diode ratings should be considered for half wave rectifier circuits. The maximum forward current ($I_{max}$) is the largest current that can flow through the diode while it is forward biased without damaging the device. The peak inverse voltage ($P_{iv}$) or peak reverse voltage ($P_{rv}$) is the maximum voltage across the diode while it is reverse biased. For the half wave rectifier, the maximum voltage developed across the diode is $V_{max}$ of the applied ac. As




(A) Diode $D_1$ forward biased




(B) Diode $D_2$ forward biased




(C) Input/output voltage waveforms

Fig. 1.13 Single-phase, full-wave rectifier circuit

shown in the preceding formula, the $P_{rv}$ of a diode used in a half-wave circuit must be much larger than the dc voltage developed.

To obtain a purer form of dc energy, it is possible to improve on half-wave rectification systems. Figure 1.13 shows a single-phase, full-wave rectifier circuit that uses two diodes and produces a dc output voltage during each alternation of the ac input. The rectified output of the full-wave rectifier has twice the dc voltage level of the half-wave rectifier.

The full-wave rectifier utilizes a center-tapped transformer to transfer ac source voltage to the diode rectifier circuit. During the positive alternation of the ac source voltage, the instantaneous charges on the transformer secondary are as shown in Figure 1.13 (A). The peak voltage ($V_{max}$) is developed across each half of the transformer secondary. At this time,

diode $D_1$ is forward biased and diode $D_2$ is reverse biased. Therefore, conduction occurs from the center tap, through the load device, through $D_1$, and back to the outer terminal of the transformer secondary. The positive half-cycle is developed across the load as shown.

During the negative alternation of the ac source voltage, diode $D_1$ is reverse biased and diode $D_2$ is forward biased by the instantaneous charges shown in Figure 1.13 (B). The current path is from the center tap, through the load device, through $D_2$, and back to the outer terminal of the transformer secondary. The negative alternation is also produced across the load, developing a full-wave output as illustrated in the waveforms in Figure 1.13 (C).

Each diode in a full-wave rectifier circuit must have a $P_{rv}$ rating of twice the value of the peak voltage developed at the output, since twice the peak voltage ($2\ V_{max}$) is present across the diode when it is reverse biased. The average voltage for a full-wave rectifier circuit is

$$V_{dc} = 2(0.318 \times V_{max}) = 0.636 \times V_{max}$$

This type of rectifier circuit produces twice the dc voltage output of a half wave rectifier circuit. Its construction requires a center-tapped transformer and two diodes that have a peak. rating of twice the peak value of applied ac voltage.

**WORDS AND TERMS**

| | |
|---|---|
| single-phase rectification 单相整流 | adjacent *a*. 接近的,毗连的,邻接的 |
| pulsate *v*. 脉动,波动 | equilibrium *n*. 平衡,均衡,相称 |
| vacuum tube 真空管,电子管 | potential *n*. 势能,位能 |
| rotary *a*. 旋转的,转动的,循环的 | diffuse *v*. 扩散,渗出 |
| prevalent 流行的,盛行的,普遍的 | barrier *n*. 栅栏,屏障,势垒 |
| conductor *n*. 导体 | prohibit *v*. 阻止,禁止 |
| insulator *n*. 绝缘体 | instantaneous *a*. 瞬时的,立即的 |
| germanium *n*. 锗 | battery *n*. 电池,蓄电池 |
| impurity *n*. 杂质 | drift *n*. 漂移 |
| triac *n*. 三端双向可控硅开关元件 | half wave 半波 |
| diac *n*. 双向开关二极管 | peak value 峰值 |
| covalent *a*. 共价的 | center-tapped transformer 带中间抽头的变压器 |
| charge *n*. 电荷 | hole *n*. 空穴 |

### 2.3 专业英语的翻译标准

翻译标准是指导翻译的准绳,也是衡量译文质量的尺度。我国清末新兴资产阶级的启蒙思想家严复第一个提出了“信、达、雅”的翻译标准。随着科学技术的不断进步和翻译工作的不断发展,翻译标准也发生了一些新的变化,人们对不同类型的文章和作品提出了不同的要求和标准。文学作品的翻译和科技作品的翻译对“信”、“达”、“雅”的侧重和处理会有所不同。本书要讲的是自动化专业英语的翻译标准。专业英语翻译标准可以概括为“忠实、通顺”4个字。

所谓忠实,主要是指忠实于原作品的内容。必须把原作品完整而准确地表达出来,不得有任何篡改、歪曲、遗漏和增删,特别是原作品中的专业术语、概念、逻辑关系等,来不得半点疏忽。同时要兼顾原作品的专业语言、专业文体和专业风格。

所谓通顺，是指译文语言必须通顺流畅，符合汉语规范。译文必须是明白畅晓的专业语言，没有逐词死译、硬译的现象，没有言语晦涩的现象，没有文理不通、结构混乱、逻辑不清的现象。

忠实和通顺是相辅相成、辩证统一的。忠实而不通顺，读者不易理解，也就谈不上忠实；通顺而不忠实，脱离原作的概念和逻辑关系，通顺也失去了意义。所以，既要防止对忠实的片面理解，一味追求形式上的对应，造成逐字翻译，产生“形式主义”；也要防止片面理解通顺的要求，过分强调译文的流畅而脱离原文的内容，添枝加叶，造成“自由主义”。

# Unit 3

## 3.1 Binary Numbering System

Practically all electronic digital systems in operation today are of the binary type. This type of system has 2 as its base or radix. The largest digital value that can be expressed in a specific place by this system is the number 1. Essentially, this means that only the numbers 0 or 1 are used in the binary system. Electronically, the value of zero can be expressed as a very low voltage value or no voltage. The number 1 can then be indicated by some voltage-value assignment larger than or more significant than zero. Binary systems that use this voltage-value assignment are described as having positive logic. Negative logic by comparison has voltage assigned to the zero and no voltage assigned to the number 1. In the discussion that follows, only positive logic will be used.

The two operational states of a binary system, one and zero, can be considered as natural circuit conditions. When a circuit is turned off or has no voltage applied, it is considered to be in the off or 0 state. An electrical circuit that has voltage applied or is operational, is therefore considered to be on or in the 1 state. A binary digit can therefore be either a 1 or a 0. The term bit is commonly used to describe this condition. A bit is a shortened version of the words binary digit.

The basic principles of numbering that are used by the decimal or base 10 numbers apply in general to binary numbers. The radix of the binary system, for example, is 2. This means that only the digits 0 and 1 can be used to express a specific place value. The first place to the left of the starting point, or, in this case, the binary point, represents the unit's or 1's location. Places that follow to the left of the binary point refer to the powers of 2. Some of the digital values of numbers to the left of the binary point are $2^0=1$, $2^1=2$, $2^2=4$, $2^3=8$, $2^4=16$, $2^5=32$, $2^6=64$, $2^7=128$, and so on.

As a general rule, when different numbering systems are used in a discussion, they must incorporate a subscript number to identify the base of the numbering system being used. The number $110_{.2}$ is a typical expression of this type. This would be described as one-one-zero instead of the decimal equivalent of one hundred and ten.

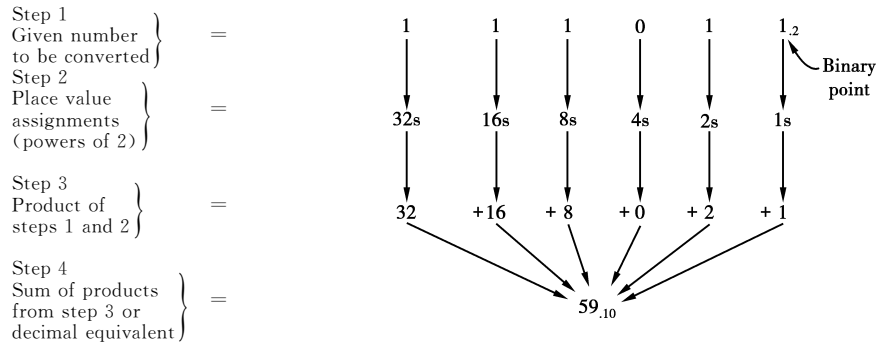



Fig. 1.14 Conversion of a binary number to a decimal

The number $110_{.2}$ is equivalent to six to the base ten, or $6_{.10}$. Starting at the first digit to the left of the binary point, this number would have place value of $0\times2^0+1\times2^1+1\times2^2$ or $0+2_{.10}+4_{.10}=6_{.10}$. The conversion of a binary number to an equivalent decimal number is shown by steps in Figure 1.14.

A simplified version of the binary-to-decimal conversion process is shown in Figure 1.14. In this method of conversion, write down the binary number first. Starting at the binary point, indicate the decimal equivalent powers-of-2 numbers for each binary place location where a 1 is indicated. For each zero in the binary number, leave a blank space or indicate a zero. Add the place value assignments and record the decimal equivalent. Practice this method on several binary numbers until you are proficient in this conversion process.

The conversion of a decimal number to a binary equivalent is achieved by repetitive steps of division by the number 2. When the quotient is even with no remainder, a 0 is recorded. When the quotient has a remainder, a 1 is recorded. The steps needed to convert a decimal number to binary number are shown in Figure 1.15.

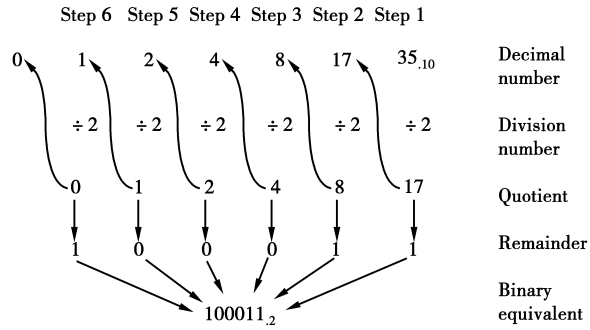



Fig. 1.15 Conversion of a decimal number to a binary number

The conversion process, in this case, is achieved by writing down the decimal number ($35_{10}$). Divide this number by the base of the system, or 2. Record the quotient and remainder as indicated. Move the quotient of step 1 to step 2 and repeat the process. The division process continues until the quotient becomes zero. The binary equivalent is simply the remainder values in their last-to-first placement order. You may want to practice this

process on several numbers to gain some degree of proficiency.

| | | | |
|---|---|---|---|
| Given decimal number | | $329._{10}$ | |
| **Step** 1<br>Grouping of digits | (3) | (2) | (9) |
| **Step** 2<br>Conversion of each digit to binary group | (0011) | (0010) | (1001) |
| **Step** 3<br>Combine group values | | $0011/0010/1001._{BCD}$ | |

Fig. 1.16 Converting a decimal number to a BCD number

When large numbers are to be indicated by binary numbers, they become somewhat awkward and difficult to use. For this reason, the binary coded decimal method of counting was devised. In this type of system, four binary digits are used to represent each decimal digit. To illustrate this procedure, we have selected the number $392._{10}$ to be converted to a binary coded decimal or BCD number. In straight binary numbers, $392._{10}=101,001,001._{2}$

To apply the BCD conversion process, the base 10 number is first divided into discrete digits according to place values (see Figure 1.16). The number $392._{10}$ therefore equals the digits 3-2-9. Converting each digit to binary would permit us to display this number as $0011—0010—1001._{BCD}$. Decimal numbers up to $999._{10}$ could be displayed and quickly interpreted by this process with only 12 binary numbers. The dash line between each group of digits is extremely important when displaying BCD numbers.

The largest digit to be displayed by any group of BCD numbers is 9. This means that six digits of a number coding group are not being used at all in this system. Because of this the octal, or base 8, and the hexadecimal, or base 16, systems were devised. Digital systems still process numbers in binary form but usually display them in BCD, octal, or hexadecimal values.

**WORDS AND TERMS**

binary *n.* 二进制
radix *n.* 根值,基数
assignment *n.* 分派,分配
bit *n.* 位
digit *n.* 数字,位数,计算单位
decimal *n.* 十进制
quotient *n.* 商数
divide *v.* (算术)除
BCD(Binary-Coded Decimal) 二-十进制码,BCD 码
proficiency *n.* 熟练,精通
hexadecimal *n.* 十六进制

### 3.2 Binary Logic Functions

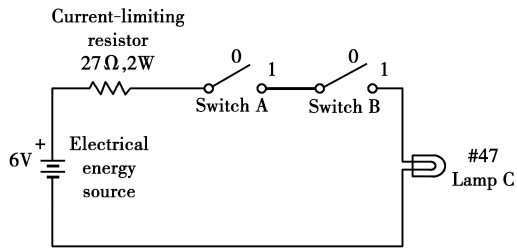
Any bistable circuit that is used to make a series of decisions based on two-state input conditions is called a binary logic circuit. Three basic circuits of this type have been developed to make simple logic decisions: the AND circuit, the OR circuit, and the NOT circuit. The logic decision made by each circuit is unique and very important in digital system operations.

Electronic circuits designed to perform specific logic functions are commonly called gates. This term refers to the capability of a circuit to pass or block specific digital signals. A simple if-then type of sentence is often used to describe the basic operation of a logic gate. For example, if the inputs applied to an AND gate are all 1, then the output will be 1. If a 1 is applied to any input of an OR gate, then the output will be 1. If any input is applied to a NOT gate, then the output will be reversed.

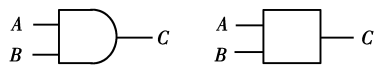
The fundamental operation of a digital system is based directly on gate applications. Technicians working with digital systems must therefore be very familiar with each basic gate function. The input-output characteristics and operation of basic logic gates will serve as the basis of our next discussion.

**AND Gates**

An AND gate is designed to have two or more inputs and one output. Essentially, if all inputs are in the 1 state simultaneously, then a 1 will appear in the output. Figure 1.17 shows a simple switch-lamp analogy of the AND gate, its symbol, and an operational table. In Figure 1.17 (A), when a switch is turned on it represents a 1 condition, while off represents a 0. The lamp also displays this same condition by being a 1 when it is on and 0 when turned off. Note that the switches are labeled A and B while the output lamp is C.




(A) Simple AND gate circuit




ANS symbol NEMA symbol

(B) AND gate symbols

| Switch A | Switch B | Lamp C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

(C) AND gate truth table

Fig. 1.17 AND gate information

The operational characteristics of a gate are usually simplified by describing the input-output relationship in a table. The table in Figure 1.17 (C) shows the 1or 0 alternatives at the input and the corresponding output that will occur as a result of this input. As a rule, such a description of a gate is called a truth table. Essentially, it shows the predictable operating conditions of a logic circuit.

Each input to an AND gate has two operational states of 1 and 0. A two-input AND gate would therefore have $2^2$, or 4, possible combinations that would influence the output. A three-input gate would have $2^3$, or 8, combinations, while a four input would have $2^4$, or 16, combinations. These combinations are normally placed in the truth table in binary

progression order. For a two-input gate, this would be 00, 01, 10, and 11, which shows the binary count of 0, 1, 2, and 3 in order.

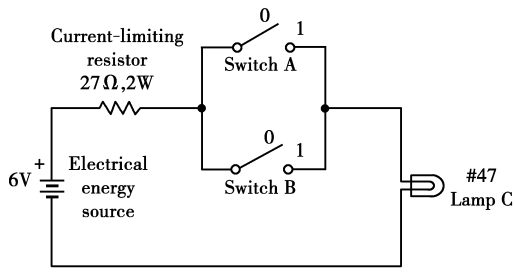
Functionally, the AND gate of Figure 1.17 (A) will only produce a 1 output when switches A and B are both l. Mathematically, this action is described as A · B = C. This expression shows the multiplication operation. In a punch-press operation, this type of gate will not actuate the drive motor until the operator presses the L push button with the left hand and the R button with the right hand at the same time.

The symbol representations of an AND gate shown in Figure1.17 (B) are very common. The square symbol is a typical National Electrical Manufacturer's Association (NEMA) representation; the round diagram is the American National Standard (ANS) symbol.

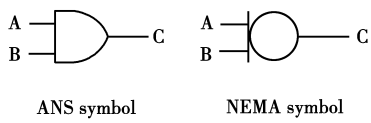
**OR Gates**

An OR gate is designed to have two or more inputs and a single output. Like the AND gate, each input to the OR gate has two possible states: 1 or 0. The output of this gate will produce a 1 when either or both inputs are 1. Figure 1.18 shows a simple lamp-switch analogy of the OR gate, its symbol, and a truth table.

Functionally, an OR gate will produce a 1 output when both switches are l or when either switch A or B is a 1. Mathematically, this action is described as A + B = C. This expression shows OR addition. Applications of this gate are used to make logic decisions as to whether or not a 1 appears at either input. The over-head or dome-lamp system of an automobile is controlled by an OR type of circuit. Individual door switches and the dash panel switch all control the lamp from a different location.




(A) Simple OR gate circuit




ANS symbol NEMA symbol

(B) OR gate symbols

| Switch A | Switch B | Lamp C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

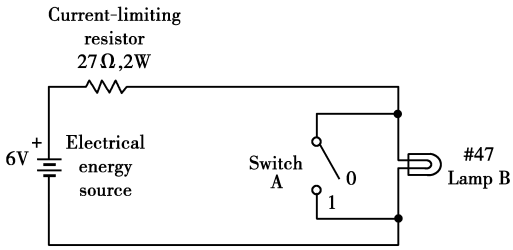
(C)OR gate truth table

Fig. 1.18 OR gate information

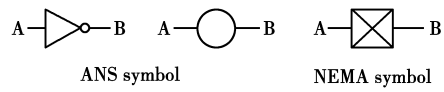
**NOT Gates**

A NOT gate has a single input and a single output, which makes it unique compared with the AND and OR gates. The output of a NOT gate is designed so that it will be opposite to that of the input state. Figure 1.19 shows a simple switch-controlled NOT gate,

its symbol, and truth table. Note that when the SPST switch is on or in the 1 state it shorts out the lamp. Likewise, placing the switch in the off condition causes the lamp to be on or in the 1 state. NOT gates are also called inverters. The significance of a NOT gate should be rather apparent after the following discussion of gates.




(A) Simple NOT gate circuit




ANS symbol NEMA symbol

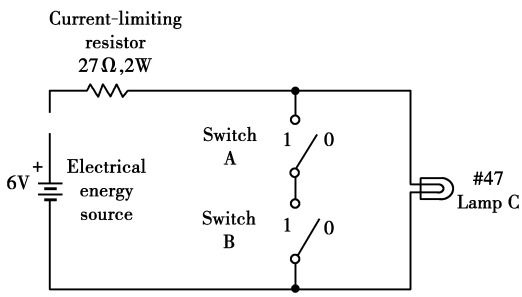
(B) NOT gate symbols

| Switch A | Lamp B |
|---|---|
| 0 | 1 |
| 1 | 0 |

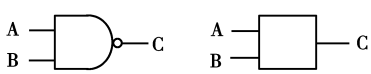
(C) NOT gate truth table

Fig. 1.19 NOT gate information

When a NOT gate is combined with an AND gate or an OR gate, it is called a combination logic function. A NOT-AND gate is normally called a NAND gate. This gate is an inverted AND gate, or simply NOT an AND gate. Figure 1.20 shows a simple switch-lamp circuit analogy of this gate, along with its symbol and truth table.




(A) NAND gate circuit



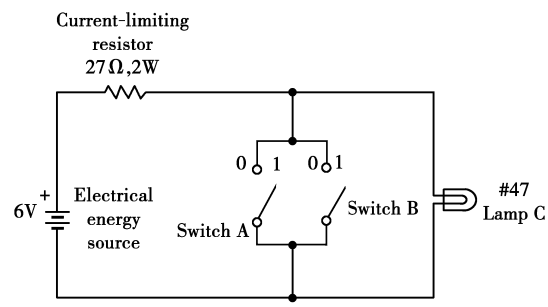

ANS symbol NEMA symbol

(B) NAND gate symbols

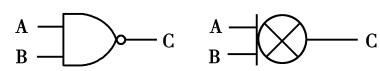
| Switch A | Switch B | Lamp C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(C) NAND gate truth table

Fig. 1.20 NAND gate information




(A) NOR gate circuit




ANS symbol NEMA symbol

(B) NOR gate symbols

| Switch A | Switch B | Lamp C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

(C) NOR gate truth table

Fig. 1.21 NOR gate information

The NAND gate is an inversion of the AND gate. When switches A and B are both on or in the 1 state, the lamp C is off. When either or both switches are off, the lamp C is in the on or l state. Mathematically, the operation of a NAND gate is expressed as $A \times B = C$. The

bar over C denotes the inversion or negative function of the gate. A combination NOT-OR or NOR gate produces a negation of the OR function. Figure 1.21 shows a simple switch-lamp circuit analogy of this gate, along with its symbol and truth table. Mathematically, the operation of a NOR gate is expressed as $A+B=\overline{C}$. A 1 will only appear in its output when A is 0 and B is 0.

**WORDS AND TERMS**

bistable circuit *n.* 双稳态电路
binary logic circuit *n.* 二进制逻辑电路
simultaneously *ad.* 同时(发生)地
analogy *n.* 类似,相似
alternative *n.* 两者挑一,选择,替换物
corresponding *a.* 相应的,符合的,对应的
truth table *n.* 真值表
multiplication *n.* (数)乘法
punch-press *n.* 冲床
actuate *v.* 开动(机器等)
motor *n.* 电动机
square *n.* 正方形,矩形
dome *n.* 圆顶,拱顶,(流线型)罩
dash panel 仪表板,控制板
button *n.* 按钮

### 3.3 专业英语的翻译过程

专业英语的翻译过程是正确理解原文和创造性地用汉语语言再现原文的过程,大体上可分为理解、表达和校核3个阶段。

在专业英语的翻译实践中,理解是表达的前提,不能正确地理解就谈不上确切地表达。但理解与表达通常是互相联系、互相促进的统一过程,不能截然分开。当译者在理解的时候,往往会自觉或不自觉地挑选表达词句;当译者在表达的时候,他又进一步加深了理解。在处理一个句子、一个段落、一篇文章时,译者往往要从英语到汉语、从汉语到英语,反复推敲,仔细研究,才能找到理想的译文。

1. 理解过程

理解主要通过专业知识和原文的上下文来进行。译者必须从专业的角度按照上下文的关系来探求正确的译法。所谓上下文可以指一个句子、一个段落,也可以指一章、一节以至全文或全书。对原文做透彻的理解是确切翻译的基础和关键。为了透彻的理解原文,必须注意以下几点:

(1)理解原文句法结构和惯用短语;

(2)理解专业术语和概念;

(3)理解逻辑关系;

(4)理解原文的专业表述方式。

2. 表达过程

表达过程就是译者把自己从原文所理解的内容用汉语重新表达出来。表达的好坏主要决定于对原文理解的深度以及对汉语语言的修养程度。

表达是理解的结果,但理解正确并不意味着必然能正确表达。在表达上还有许多具体方法和具体问题要解决。

3. 校核过程

校核是理解与表达的进一步深化,是对原文内容进一步核实以及对译文语言进一步推敲

的过程。翻译时尽管十分细心，但译文中仍然会有错、漏、别字或字句欠妥的地方。因此校核也是使译文能符合忠实、通顺的翻译标准所必不可少的环节。校核过程一般应特别注意以下几点：

(1)校核译文在专业术语、技术参数、公式等方面有无错漏；

(2)校核译文的重点词句有无错漏；

(3)修改译文不够恰当的句子、词组和词；

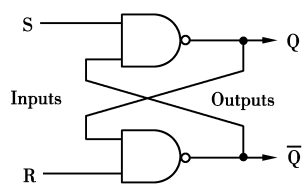
(4)校核译文的标点符号有无错漏。

# Unit 4

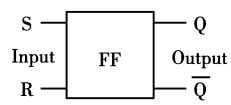
## 4.1 Flip-Flops

Flip-flops are commonly used to generate signals, shape waves, and achieve division. In addition to these operations, a flip-flop may also be used as a memory device. In this capacity, it can be made to hold an output state even when the input is completely removed. It can also be made to change its output when an appropriate input signal occurs.

The reset-set or RS flip-flop of Figure 1.22 is a typical digital system control device. The logic diagrams, ANS symbol, and truth table of the flip-flop are shown in the figure. Note that the truth table for this device is somewhat more complicated than that of a simple logic gate. For example, it must show the different states of the device before an input pulse occurs and then show how it changes after the input has arrived. Note that two of the operating conditions produce an unpredictable output. In this state of operation, the first arriving pulse will produce an output only by coincidence.




(A) Logic diagram with NAND gates




(B) ANS symbol

Unpredictable

| Applied inputs | | Previous outputs | | Resulting outputs | |
|---|---|---|---|---|---|
| S | R | Q | $\overline{Q}$ | Q | $\overline{Q}$ |
| 0 | 0 | 1 | 0 | 1/0 | 0/1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0/1 | 1/0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |

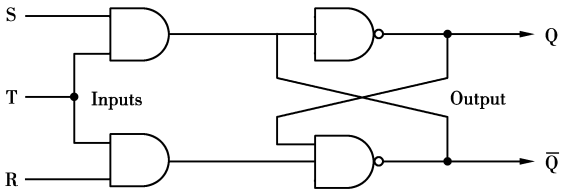
Unpredictable

(C)RS flip-flop truth table

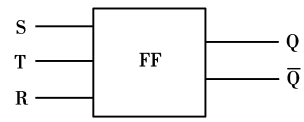
Fig. 1.22 RS flip-flop information

In many digital system applications, flip-flops must be set and cleared at specific times with respect to other operating circuits. This type of operation can be achieved by manipulating flip-flops in step with a clock pulse. In this case, the appropriate RS inputs and

clock pulse must all be present in order to cause a state change. A device of this type is called an RS triggered flip-flop or simply an RST flip-flop.




(A) Logic diagram of RST flip-flop




(B) ANS symbol

| Applied inputs | | | Previous outputs | | Resulting outputs | |
|---|---|---|---|---|---|---|
| S | R | T | Q | $\overline{Q}$ | Q | $\overline{Q}$ |
| 0 | 0 | 0 | 1 | 0 | 1/0 | 0/1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0/1 | 1/0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |

Unpredictable

(C) RST flip-flop truth table

Fig. 1.23 RST flip-flop

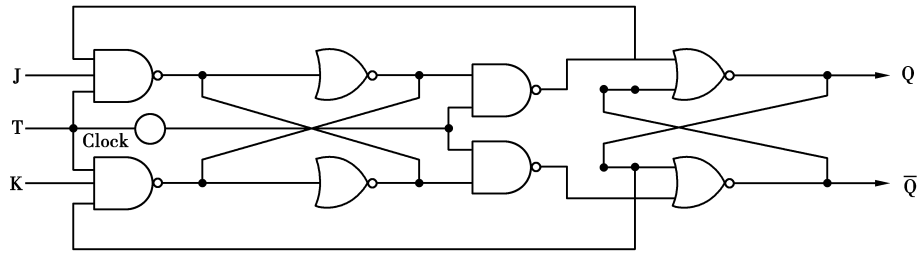
The truth table of an RST flip-flop is basically the same as that of the RS flip-flop of Figure 1.22. It will only initiate a state change when the clock pulse arrives at the T input. A two-input AND gate is simply added to the set and reset inputs to accomplish this operation. Figure 1.23 shows this modification, the corresponding ANS logic symbol, and the truth table for the RST flip-flop.

Another important flip-flop device that is commonly used in digital systems is the JK flip-flop. This device is somewhat unusual because it has no unpredictable output states. It can be set by applying a 1 to the J input and can be cleared by feeding a 1 to the K input. A 1 signal applied to both J and K inputs simultaneously causes the output to change states or toggle. A 0 applied to both inputs at the same time does not initiate a state change. The inputs of a JK flip-flop are controlled directly by clock pulse application.

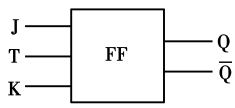
Figure 1.24 shows a logic diagram, ANS symbol, and truth table for the JK flip-flop. Notice that there are no unpredictable output states for this device. Several versions or modifications of the basic JK flip-flop are available today. These include devices with preset and preclear inputs that can be used to establish sequential operations at a precise moment. Flip-flops are commonly used as the basic logic element for counting operations, temporary memory, and sequential switching operations.

One of the most versatile and important logic devices of a digital system is the counter. This device, as a general rule, can be employed to count a wide variety of objects in a number of different digital system applications. While this device may be called upon to count an endless number of objects, it essentially counts only one thing, electronic pulses. These pulses may be produced electronically by a clock mechanism, electromechanically, photoelectrically, acoustically, or by a number of other processes. The basic operation of the counter, however, is completely independent of the pulse generator.

A common application of the digital counter is used to count numerical information in




(A) Logic diagram of JK flip-flop




(B) ANS symbol

| Applied inputs | | | Previous outputs | | Resulting output | |
|---|---|---|---|---|---|---|
| J | K | T | Q | $\overline{Q}$ | Q | $\overline{Q}$ |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 |

Toggle state

(C) JK flip-flop truth table

Fig. 1.24 JK flip-flop information

binary form. This type of device simply employs a number of flip-flops connected so that the Q output of the first device drives the trigger or clock input of the next device. Each flip-flop therefore has a divide-by-2 function.

Figure 1.25 shows JK flip-flops connected to achieve binary counting. The counter in Figure 1.25(A) is commonly called a binary ripple counter. Each flip-flop in this circuit has the J and K inputs held at a logic 1 level. Each clock pulse applied to the input of $FF_1$ will then cause a change in state. The flip-flops only trigger on the negative-going part of the clock pulse. The output of $FF_1$ will therefore alternate between 1 and 0 with each pulse. A 1 output will appear at Q of $FF_1$ for every two input pulses. This means that each flip-flop has a divide-by-2 function. Five flip-flops connected in this manner will produce a $2^5$, or 32, count. The largest count in this case is $1111_{.2}$; that is, $31_{.10}$ occurs when each Q output is 1. The next applied pulse clears the counters so that 0 appears at all the Q outputs.

By grouping three flip-flops together [Figure 1.25 (B)], it is possible to develop the units part of a binary coded octal or BCO counter. Therefore, $111_{.2}$ would be used to represent the seven count or seven units of an octal counter. Two groups of three flip-flops connected in this manner would produce a maximum count of $111\text{-}111_{.2}$, which represents $77_{.8}$. or $63_{.10}$.

By placing four flip-flops together in a group [Figure 1.25 (C)], it is possible to develop the units part of a binary coded hexadecimal or BCH counter. Thus $1111_{.2}$ would be

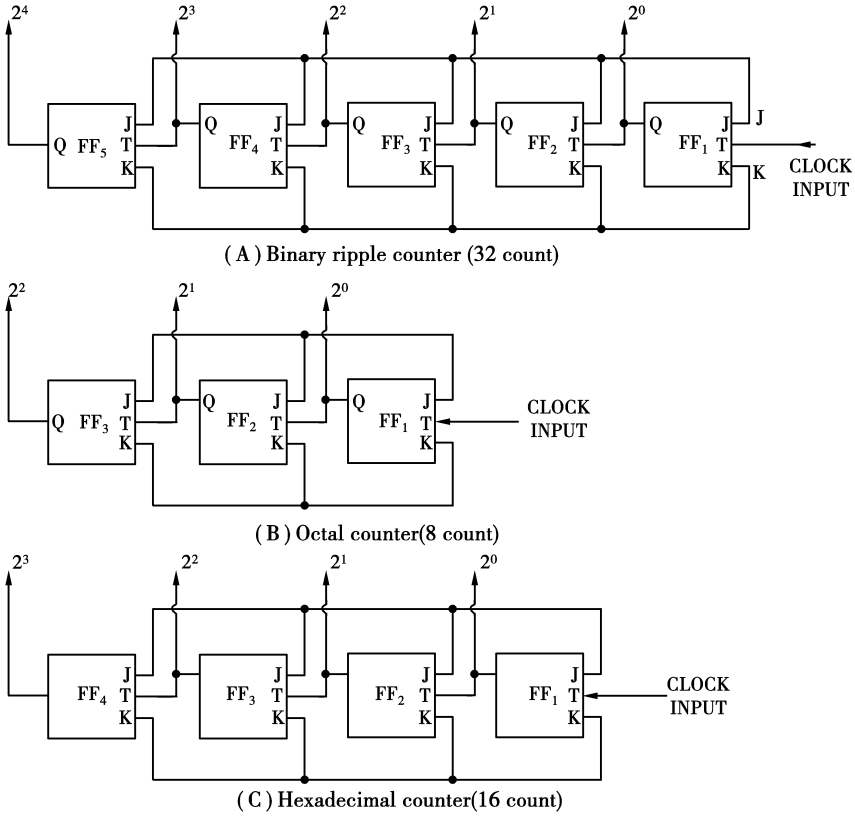



Fig. 1.25 Digital counters achieved with JK flip-flop

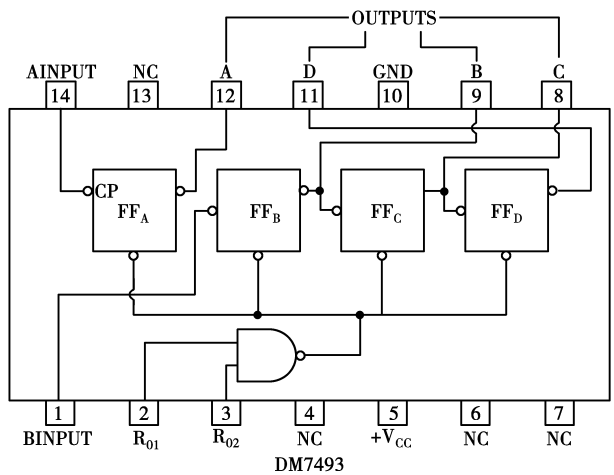



Fig. 1.26 Four-bit binary counter IC

used to represent $F_{.16}$ or $15_{.10}$. Two groups of four flip-flops could be used to produce a maximum count of $1111\text{-}1111_{.2}$, which would represent $FF_{.16}$ or $225_{.10}$. Each succeeding group of four flip-flops would be used to raise the counting possibility to the next 16.

Binary counters that contain four interconnected flip-flops are commonly built on one IC

chip. Figure 1.26 shows the logic connections of a 4-bit binary counter. When used as a 4-bit counter, the $FF_A$ will now produce a maximum count of $1111_{.2}$ or $15_{.10}$. By disconnecting $FF_A$ from $FF_B$, and applying the clock to $FF_B$ input, we have a 3-bit or BCO counter. The outputs of flip-flops $FF_A$ through $FF_D$ are labeled A, B, C, and D, respectively.

**WORDS AND TERMS**

flip-flop *n.* 双稳态多谐振荡器,触发器
memory *n.* 存储器
manipulate *v.* 操纵,处置
clock pulse 时钟脉冲
modification *n.* 修改,改变,改进型
toggle *n.* 反复电路
mechanism *n.* 机械装置,机构
electromechanical *a.* 机电的
photoelectrical *a.* 光电的
acoustical *a.* 听觉的,声学的
toggle flip-flop *n.* 反转触发器
preset *v.a.* 预调(的),预置(的)
sequential *a.* 连续的,有序的,结果的
versatile *a.* 通用的,多用途的,易变的
counter *n.* 计数器
endless *a.* 不断的,环状的
pulse generator 脉冲发生器
numerical *a.* 数字的,数值的
ripple *n.* 脉动,波动
IC chip *n.* 集成电路芯片

### 4.2 Digital System Decoding

Before a display device can be effectively used to develop a digital number, it must receive an appropriate actuating signal from the counter. The counter output signal in this case normally contains information in binary form. This information must therefore be decoded in such a way that it will energize a display when a specific number occurs. Decoding of this type is achieved by a number of four-input gates connected to the A, B, C, and D outputs of a BCD counter. When an appropriate combination of binary number signals appears at the input of the decoder, the output will energize a display device by grounding a specific number or bar segment. In a strict sense, the manual switches of the previous display devices can be replaced by an automatically controlled decoder.

Two distinct types of decoders are available today to drive display devices used in digital systems. The discrete number type of display requires a decoder that has 10 distinct output signals in order to be energized properly (Figure 1.27). Only one output must be energized at a time. The seven-segment type of display device is energized by two or more signals at a time. When the number 8 is displayed, all segments must be energized at one time. This necessitates an entirely different type of decoder circuit. The basic method of driving specific gates, however, is very similar for both types of decoders.

The logic diagram of a BCD-to-decimal decoder is shown in Figure 1.28. This entire circuit is conveniently built on a single IC chip and produced in either a dual in-line or flat-package housing. In this IC, the A, B, C, and D inputs are either inverted once or twice before being applied to their respective NAND gates. When an appropriate input number combination is applied, it causes the corresponding NAND gate to be actuated. A zero or ground output then appears at its output. This, in turn, energized the appropriate cathode of

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