Accelerator Functional Unit Developer's Guide for Intel® FPGA Programmable Acceleration Card

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **1.2 and 2.0.1**

 **Online Version**

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Contents

1. About this Document

This document serves as a hardware developers guide for developing Accelerator Functional Units (AFUs) for the Intel Acceleration Stack for Intel Xeon® CPU with FPGAs product, hereafter referred to as the Acceleration Stack.

1.1. Intended Audience

The intended audience consists of FPGA RTL designers developing AFUs for the Acceleration Stack on the Intel FPGA Programmable Acceleration Card (Intel FPGA PAC) and the hardware platforms (referred to as Intel FPGA PAC throughout this document).

1.2. Conventions

Table 1. Document Conventions

Convention	Description
#	Precedes a command that indicates the command is to be entered as root.
$	Indicates a command is to be entered as a user.
`This font`	Filenames, commands, and keywords are printed in this font. Long command lines are printed in this font. Although long command lines may wrap to the next line, the return is not part of the command; do not press enter.
<variable_name>	Indicates the placeholder text that appears between the angle brackets must be replaced with an appropriate value. Do not enter the angle brackets.

1.3. Acronym List for Accelerator Functional Unit Developer's Guide

Table 2. Acronyms

Acronyms	Expansion	Description
AFU	Accelerator Functional Unit	Hardware Accelerator implemented in FPGA logic which offloads a computational operation for an application from the CPU to improve performance.
AF	Accelerator Function	Compiled Hardware Accelerator image implemented in FPGA logic that accelerates an application. An AFU and associated AFs may also be referred to as GBS (Green-Bits, Green BitStream)

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Acronyms	Expansion	Description
		in the Acceleration Stack installation directory tree and in source code comments.
API	Application Programming Interface	A set of subroutine definitions, protocols, and tools for building software applications.
ASE	AFU Simulation Environment	Co-simulation environment that allows you to use the same host application and AF in a simulation environment. ASE is part of the Intel Acceleration Stack for FPGAs.
CCI-P	Core Cache Interface	CCI-P is the standard interface AFUs use to communicate with the host.
FIU	FPGA Interface Unit	FIU is a platform interface layer that acts as a bridge between platform interfaces like PCIe*, UPI and AFU-side interfaces such as CCI-P.
FIM	FPGA Interface Manager	The FPGA hardware containing the FPGA Interface Unit (FIU) and external interfaces for memory, networking, etc. The FIM may also be referred to as BBS (Blue-Bits, Blue BitStream) in the Acceleration Stack installation directory tree and in source code comments. The Accelerator Function (AF) interfaces with the FIM at run time.
NLB	Native Loopback	The NLB performs reads and writes to the CCI-P link to test connectivity and throughput.
OPAE	Open Programmable Acceleration Engine	The OPAE is a software framework for managing and accessing AFs.
PR	Partial Reconfiguration	The ability to dynamically reconfigure a portion of an FPGA while the remaining FPGA design continues to function.
TCP	Transmission Control Protocol	TCP is a standard Internet protocol that defines how to establish and maintain a network conversation through which application programs can exchange data.
PIM	Platform Interface Manager	An abstraction layer for managing top-level device ports and system-provided clock crossing.
HSSI	High Speed Serial Interface	Reference to the multi-gigabit serial transceiver I/O in the FIM and the corresponding interface to the AFU.

1.4. Acceleration Glossary

Table 3. Acceleration Stack for Intel Xeon CPU with FPGAs Glossary

Term	Abbreviation	Description
Intel Acceleration Stack for Intel Xeon CPU with FPGAs	Acceleration Stack	A collection of software, firmware and tools that provides performance-optimized connectivity between an Intel FPGA and an Intel Xeon processor.
Intel FPGA Programmable Acceleration Card (Intel FPGA PAC)	Intel FPGA PAC	PCIe FPGA accelerator card. Contains an FPGA Interface Manager (FIM) that pairs with an Intel Xeon processor over the PCIe bus.

1.5. Related Documentation

Table 4. Item Description

Item	Description
Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA	This document describes the Acceleration Stack and provides instructions for hardware and software installation and setup required for development with the stack.
Intel Acceleration Stack Quick Start Guide for Intel FPGA Programmable Acceleration Card D5005	This document describes the Acceleration Stack and provides instructions for hardware and software installation and setup required for development with the stack.
Acceleration Stack for Intel Xeon CPU with FPGAs Core Cache Interface (CCI-P) Reference Manual	This document describes the CCI-P protocol and requirements placed on AFUs.
Networking Interface for Open Programmable Acceleration Engine: Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA	This document describes the HSSI device interface offered by the Intel PAC with Intel Arria 10 GX FPGA hardware platform and the OPAE tools and driver features that support the network port feature.
Networking Interface for Open Programmable Acceleration Engine: Intel FPGA Programmable Acceleration Card D5005	This document describes the HSSI device interface offered by the Intel FPGA PAC D5005 platform and the OPAE tools and driver features that support the network port feature.
Intel Accelerator Functional Unit Simulation Environment User Guide	This document provides instructions on how to use the Intel Accelerator Functional Unit Simulation Environment.
Open Programmable Acceleration Engine (OPAE) Tools Guide	This user guide documents the utilities provided in the Open Programmable Acceleration Engine (OPAE) software component of the Acceleration Stack.

2. Introduction

2.1. Getting Started with AFU Development

Depending on which Intel FPGA PAC you are using, please refer to one of the following Quick Start Guides:

- If you are using Intel PAC with Intel Arria® 10 GX FPGA, refer to the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*.
- If you are using Intel FPGA PAC D5005, refer to the *Intel Acceleration Stack Quick Start Guide for Intel FPGA Programmable Acceleration Card D5005*.

The *Quick Start Guide* provides an overview of the Acceleration Stack and provides instruction for installation and setup of hardware and software components of the stack, including the OPAE SDK used to develop AFUs and generate loadable AF images. It is essential to familiarize yourself with the concepts developed for the Acceleration Stack and to complete the installation and setup procedures covered in the *Quick Start Guide*.

This guide for AFU development builds on the concepts and environment setup established in the *Quick Start Guide*.

Related Information

- Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA
- Intel Acceleration Stack Quick Start Guide for Intel FPGA Programmable Acceleration Card D5005

2.1.1. Development Environment References

The `OPAE_PLATFORM_ROOT` environment variable points to the OPAE SDK installation as detailed in the *Quick Start Guide*.

2.1.2. FPGA Tools and IP Requirements

You need to download the Intel Acceleration Stack for Development to generate the Accelerator Functions (AFs).

The Intel Acceleration Stack for Development installer includes licenses for the following software and IPs required for the generation of the AFs:

- Intel Quartus® Prime Pro Edition software

  Note: For information on compatible version of the software for each platform, refer to the platform specific *Release Notes*.
- Intel FPGA PCI Express SR-IOV Block IP license
- Network IP license

You do not need to purchase the license separately for these IPs.

For requirements when using the ASE for AFU functional verification, refer to the *Intel Accelerator Functional Unit Simulation Environment User Guide*.

Related Information

- Intel Accelerator Functional Unit Simulation Environment User Guide
- Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 1.2 Release Notes
- Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 2.0 Release Notes: For the Intel FPGA Programmable Acceleration Card D5005
- Installing the Intel Acceleration Stack Development Package on the Host Machine

2.2. Base Knowledge and Skills Prerequisites

The Acceleration Stack is a framework and toolset to leverage FPGA technology Most of the platform-level complexity has been abstracted away for the AFU developer by the FPGA Interface Manager (FIM) in the FPGA static region. This guide assumes the following FPGA logic design-related knowledge and skills:

- Familiarity with PR compilation flows, including the Intel Quartus Prime Pro Edition PR flow, concepts of physical and logical partitioning in the FPGA, module boundary best practices, and resource restrictions.

  The hardware compilation flow automates management of the partial reconfiguration region.
- Knowledge and skills in static timing closure, including familiarity and skill with the Timing Analyzer tool in Intel Quartus Prime Pro Edition, applying timing constraints, Synopsys* Design Constraints (`.sdc`) language and Tcl scripting, and design methods to close timing on critical paths.
- Knowledge and skills with industry standard RTL simulation tools supported by the Acceleration Stack. For more information, refer to the *Intel Accelerator Functional Unit (AFU) Simulation Environment (ASE) User Guide*.

Related Information

Intel Accelerator Functional Unit Simulation Environment User Guide