F-Tile DisplayPort Intel® FPGA IP Design Example User Guide

Updated for Quartus® Prime Design Suite: **24.1**

IP Version: **20.0.1**

Online Version
Send Feedback

UG-20347

709308
2024.06.06

Contents

1. DisplayPort Intel® FPGA IP Design Example Quick Start Guide

The DisplayPort Intel® FPGA IP design examples for Agilex™ 7 F-Tile devices feature a preliminary simulation testbench and a hardware design that supports compilation and hardware testing.

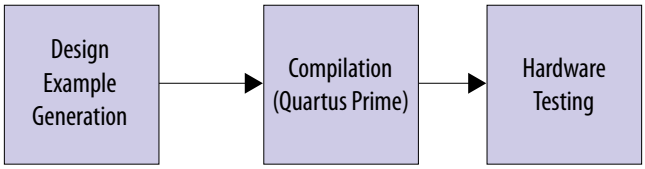
The DisplayPort Intel FPGA IP offers the following design examples:

- DisplayPort SST parallel loopback without a Pixel Clock Recovery (PCR) module
- DisplayPort SST parallel loopback with AXIS Video Interface
- DisplayPort SST RX-only
- DisplayPort SST TX-only

When you generate a design example, the parameter editor automatically creates the files necessary to simulate, compile, and test the design in hardware.

Note: A design example might not be enabled if the selected IP options are incompatible with the example design. For example, if the DisplayPort Source is enabled, then the RX-only design will not be available. Refer to the *DisplayPort Intel FPGA IP Design Example Parameters for Intel Agilex 7 F-Tile Device* table for the required IP settings.

Figure 1. Development Stages



Related Information

- DisplayPort Intel FPGA IP Design Example Parameters on page 7
- DisplayPort Intel FPGA IP User Guide
- Migrating to Intel Quartus Prime Pro Edition

1.1. Directory Structure

Figure 2. Directory Structure

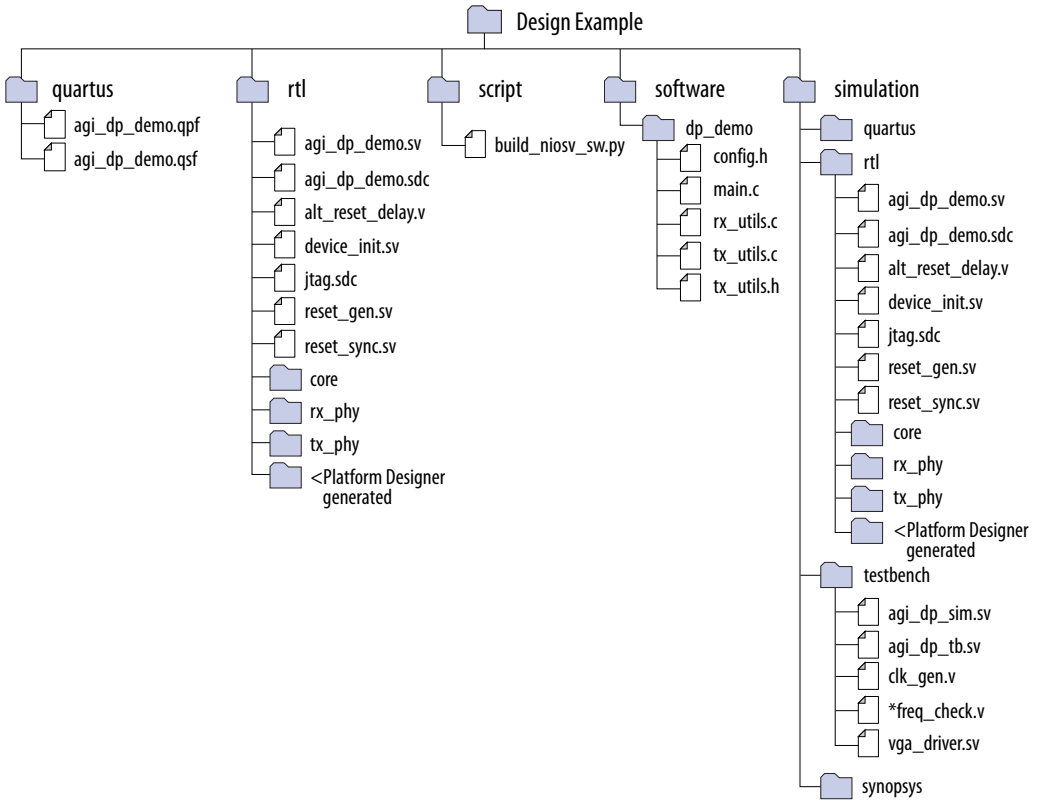


Table 1. Design Example Components

Folders	Files
rtl/core	dp_core.ip
	dp_rx.ip
	dp_tx.ip
rtl/rx_phy	dp_gxb_rx/ ((DP PMA UX building block)
	dp_rx_data_fifo.ip
	rx_top_phy.sv
rtl/tx_phy	dp_gxb_rx/ ((DP PMA UX building block)
	dp_tx_data_fifo.ip
	dp_tx_data_fifo.ip

1.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the design example:

Hardware

- Agilex 7 I-Series SoC Development Kit
- DisplayPort Source GPU
- DisplayPort Sink (Monitor)
- Bitec DisplayPort FMC daughter card Revision 8C or 8D
- DisplayPort cables

Software

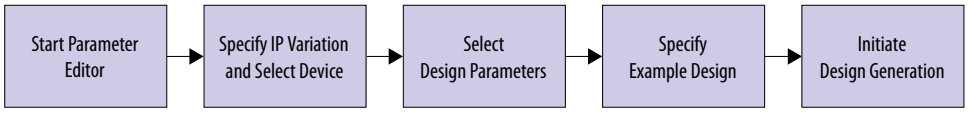
- Quartus® Prime Pro Edition
- Ashling RiscFree* integrated development environment (IDE) for Intel FPGAs

1.3. Generating the Design

Use the DisplayPort Intel FPGA IP parameter editor in Quartus Prime software to generate the design example.

Note: You need a Nios® V evaluation license. Refer to the *Nios V Processor Licensing* topic in the *Nios V Embedded Processor Design Handbook*.

Figure 3. Generating the Design Flow



1. To generate an example design, follow these steps:
   - For Quartus Prime Pro Edition running in a Windows environment:
     a. Open "Nios V Command Shell" from the Windows search path.
     b. Run "**quartus**" in Nios V Command Shell to open Quartus Prime Pro Edition.
   - For Quartus Prime Pro Edition running in a Linux environment:
     a. cd to **<Quartus installation path>/niosv/bin** and run "**niosv-shell**".
     b. Run "**quartus**" to open Quartus Prime Pro Edition.
2. Select **Tools ➤ IP Catalog**, and select Agilex 7 F-Tile as the target device family.
   Note: The design example only supports Agilex 7 F-Tile devices.
3. In the IP Catalog, locate and double-click **DisplayPort Intel FPGA IP**. The **New IP Variation** window appears.
4. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named <your_ip>.ip.
5. Select an Agilex 7 F-Tile device in the **Device** field, or keep the default Quartus Prime software device selection.

6. Click OK. The parameter editor appears.
7. Configure the desired parameters for both TX and RX.

   Note: The Nios V software has the capability to read and print out the DisplayPort Main Stream Attribute (MSA) information in the Nios V terminal. To read or print the MSA information, turn on the Enable GPU Control parameter.
8. Under the Design Example tab, select **DisplayPort SST Parallel Loopback Without PCR**, **DisplayPort SST Parallel Loopback with AXIS Video Interface**, **DisplayPort SST TX-only**, or **DisplayPort SST RX-only**.
9. Select **Synthesis** to generate the hardware design example.
10. For **Target Development Kit**, select Agilex 7 I-Series SoC Development Kit FA or Agilex 7 I-Series SoC Development Kit FB. This causes the target device selected in step 4 to change to match the device on the development kit.
    - For Agilex 7 I-Series SoC Development Kit FA, the default device is AGIB027R31B1E1V.
    - For Agilex 7 I-Series SoC Development Kit FB, the default device is AGIB027R31B1E1VAA.
11. Click **Generate Example Design**.

Related Information

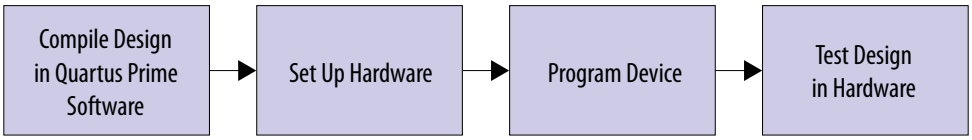
Nios V Embedded Processor Design Handbook
Provides information about Nios V processor licensing.

1.4. Simulating the Design

Simulation is not yet supported in this release.

1.5. Compiling and Testing the Design

Figure 4. Compiling and Simulating the Design



To compile and run a demonstration test on the hardware example design, follow these steps:

1. Ensure hardware example design generation is complete.
2. Launch the Quartus Prime Pro Edition software and open `<project>/quartus/agi_dp_demo.qpf`.
3. Click **Processing ➤ Start Compilation**.
4. After successful compilation, the Quartus Prime Pro Edition software generates a .sof file in your specified directory.
5. Connect the DisplayPort RX connector on the Bitec daughter card to an external DisplayPort source, such as the graphics card on a PC.
6. Connect the DisplayPort TX connector on the Bitec daughter card to a DisplayPort sink device, such as a video analyzer or a PC monitor.

7. Ensure all switches on the development board are in default position.
8. Configure Clock Controller GUI **Si5391A OUT6** to **150 MHz**.
9. Configure the selected Agilex 7 F-Tile device on the development board using the generated .sof file (Tools ➤ Programmer).
10. The DisplayPort sink device displays the video generated from the video source.

Related Information

Agilex 7 I-Series FPGA Development Kit User Guide

1.5.1. Regenerating ELF File

By default, the ELF file is generated when you generate the dynamic design example. However, in some cases, you need to regenerate the ELF file if you modify the software file or regenerate the `dp_core.qsys` file. Regenerating the `dp_core.qsys` file updates the `.sopcinfo` file, which requires you to regenerate the ELF file.

1. Go to <*project directory*>`/software` and edit the code if necessary.
2. Go to <*project directory*>`/script` and execute the following build script:
   - On Windows:
     a. Search and open Nios V Command Shell.
     b. In the Nios V Command Shell, go to <*project directory*>`/script` and execute `quartus_py .\build_niosv_sw.py -d`.
   - On Linux:
     a. Launch a Nios V Shell, $QUARTUS_ROOTDIR/../niosv/bin/niosv-shell.
     b. In the Nios V Shell, go to <*project directory*>`/script` and execute `quartus_py ./build_niosv_sw.py -d`.
3. Make sure an `.elf` file is generated in <*project directory*>`/niosv-software/build`.
4. Download the generated `.elf` file into the FPGA without recompiling the `.sof` file by running the following script:

   `niosv-download`<*project directory*>`/software/dp_demo/*.elf`.
5. Push the reset button on the FPGA board for the new software to take effect.

1.6. DisplayPort Intel FPGA IP Design Example Parameters

Table 2. DisplayPort Intel FPGA IP Design Example QSF constraint for Agilex 7 F-Tile Devices

QSF Constraint	Description
set_global_assignment -name VERILOG_MACRO "__DISPLAYPORT_support__=1"	Enables DisplayPort custom SRC (Soft Reset Controller) flow.

Table 3. DisplayPort Intel FPGA IP Design Example Parameters for Agilex 7 F-Tile Devices

Parameter	Value	Description
Available Design Example		
Select Design	• None • DisplayPort SST Parallel Loopback without PCR • DisplayPort SST Parallel Loopback with AXIS Video Interface • DisplayPort RX-only • DisplayPort TX-only	Select the design example to be generated. • None: No design example is available for the current parameter selection. • DisplayPort SST Parallel Loopback without PCR: This design example demonstrates parallel loopback from DisplayPort sink to DisplayPort source without a Pixel Clock Recovery (PCR) module when you turn on the **Enable Video Input Image Port parameter**. • DisplayPort SST Parallel Loopback with AXIS Video Interface: This design example demonstrates parallel loopback from DisplayPort sink to DisplayPort source with AXIS Video interface when **Enable Active Video Data Protocols** is set to **AXIS-VVP Full**. • DisplayPort RX-only: This example design demonstrates an RX-only design. The **Enable Video Input Image Port** parameter must be disabled. The example design software will report the RX link status. • DisplayPort TX-only: This example design demonstrates a TX-only design. The **Enable Video Input Image Port** parameter must be disabled. The example design software will report the TX link status. The design will output color bars in 1080p format.
Design Example Files		
Simulation	On, Off	Turn on this option to generate the necessary files for the simulation testbench. *Note:* Simulation is not yet supported in this release.
Synthesis	On, Off	Turn on this option to generate the necessary files for Quartus Prime compilation and hardware design.
Generated HDL Format		
Generate File Format	Verilog, VHDL	Select your preferred HDL format for the generated design example fileset. *Note:* This option only determines the format for the generated top level IP files. All other files (e.g. example testbenches and top level files for hardware demonstration) are in Verilog HDL format.
Target Development Kit		
Select Board	• No Development Kit • Agilex 7 I-Series SoC Development Kit FA • Agilex 7 I-Series SoC Development Kit FB • Custom Development Kit	Select the board for the targeted design example.

continued...

Parameter	Value	Description
		• No Development Kit: This option excludes all hardware aspects for the design example. The IP core sets all pin assignments to virtual pins. • Agilex 7 I-Series SoC FPGA Development Kit FA: This option automatically sets the project's target device to the AGIB027R31B1E1V. You may change the target device using the **Change Target Device** parameter, but Intel strongly recommends that you **do not override the target device**. If you require a different device, select the Custom Development Kit option. The IP core sets all pin assignments according to the development kit. • Agilex 7 I-Series SoC FPGA Development Kit FB: This option automatically sets the project's target device to the AGIB027R31B1E1VAA. You may change the target device using the **Change Target Device** parameter, but Intel strongly recommends that you **do not override the target device**. If you require a different device, select the Custom Development Kit option. The IP core sets all pin assignments according to the development kit. • Custom Development Kit: This option allows the design example to be tested on a third-party development kit with an Intel FPGA. The project's target device will be set using the target device of the current project. You are required to modify the pin assignments.
Target Device		
Change Target Device	On, Off	Turn on this option and select the preferred device variant for the development kit.

Related Information

- DisplayPort Intel FPGA IP Design Example Quick Start Guide on page 3
- DisplayPort Intel FPGA IP User Guide
- Migrating to Intel Quartus Prime Pro Edition