J750 Hardware Specifications

Rev 1.95 4/27/2001

Table of Contents

1. OVERVIEW

The J750 is a 512 or 1024 channel test system, contained entirely in the test head.

1.1 Environmental

20 to 30 degrees C and 40-60 % humidity non-condensing .

A temperature change of 5 Degrees C will require internal re-calibration.

1.2 Channel count

The minimum system configuration is 64 channels. The system is expandable in 64 channel increments. The maximum system is either 512 channels or 1024 channels, depending on tester model.

2. Vector Rate

The base vector rate for the system in normal mode allows full functionality on all channels at 100Mhz.

A special "extended" mode provides additional capabilities when the vector rate is restricted to 50MHz. Multiplexing pairs of channels doubles the extended mode data rate to 100 Mhz with full functionality but lower channel count.

3. Channel Specifications

A Spice™ model will be available upon request. The measurement convention is: Positive current flows into the device under test from the tester. Negative current flows out of the device under test. Thus IOL is always positive, and IOH is negative. The level names correspond to the device usage, thus the Device Voltage Input Low is the tester's drive low level.

Level change settling time: 1.28ms, for Channel Levels

3.1 VIL and VIH Driver Levels

3.1.1 Voltage ranges

	Range	Resolution	Accuracy
Vil	-1 to +6V	1mv	± 15 mV
Vih	0 to +7.1V	1mv	± 15 mV

Minimum Difference: Vih >= (Vil + 0.1)

DC Output Current Hi Source/Low Sink 35 mA min.

Dynamic drive current 100ma Typ.

3.1.2 Output Impedance

VIH/VIL > 1V from either voltage rail 50 ohms, ± 2.5 ohms

VIH/VIL < 1V from either voltage rail 50 ohms, ± 5 ohms typ.

Measured at current 30 mA.

3.1.3 Minimum Pulse Width

Voltage Swing	Minimum pulse width	Typical Rise/Fall Time
1 V swing	2 ns	1.0 ns
3 V swing	3 ns	1.9 ns
5 V swing	4.5 ns	2.8 ns

3.1.4 Waveform Fidelity

From 1ns to 15 ns after transition. < (5% ± 50mv)

From 15 ns to 5 us after transition. < (0.5% delta V ± 20 mV)

Transition is defined as the 80% point on the drive waveform.

Valid when levels are more than 1 volt from either rail.

3.1.5 Rise/Fall Time

1V swing (20%-80%) 1.0 ns ± 200 pS

3V swing (20%-80%) 1.9 ns ± 300 pS

5V swing (20%-80%) 2.8 ns ± 400 pS

Valid when levels are more than 1 volt from either rail.

When swinging within 1 volt of a rail the edge transition time increases by 500 ps typically

3.2 COMPARATOR SPECIFICATIONS

3.2.1 VOL and VOH Comparator Levels

	Range	Resolution	Accuracy
Vol	0 to +5V	1mv	± 15 mV
Voh	0 to +5V	1mv	± 15 mV

Minimum Difference: Voh >= (Vol + 30mv)

The comparators will switch from –1.3 to +7v, but timing and level accuracy is not specified.

Inputs are protected by schottky diodes. This provides current protection of: 200 mA nominal

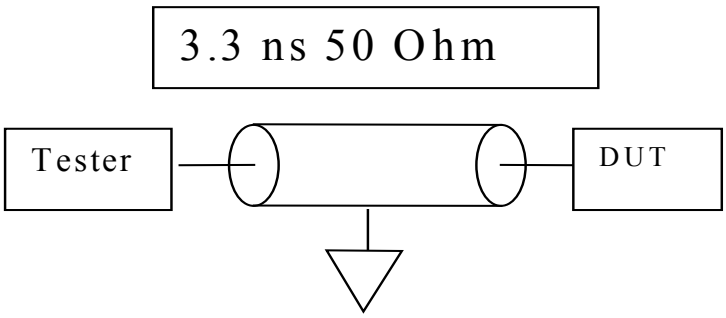
3.2.2 Input Leakage

Leakage < ±2 uA

With IOH/IOL current loads are disabled.

3.2.3 Device Loading

The device loading is most accurately modeled as a transmission line from the device under test to the channel card's pin electronics.



Standard Channel and High Voltage Channel

50 ohm transmission line from Pogo-pin to Channel Card 3.3 ns typical

Excess Inductance at the comparator 5.8 nH typical

Excess Capacitance at the comparator 2.5 pF typical

Excess Inductance or Capacitance is inductance or capacitance which is not part of the 50 ohm environment and therefore causes a reflection.

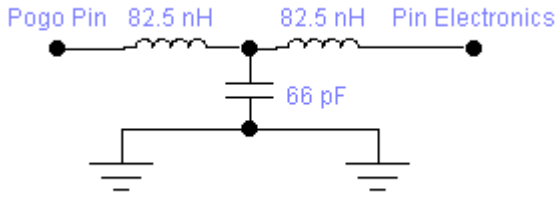
The path from the Pogo-pins to the DUT on the user DIB will add transmission line length.

50 ohm PCB trace is roughly 0.166 ns/inch as measured by a 50ps risetime TDR waveform.

3.2.4 Slow Risetime Loading

For device rise times >10 ns, the transmission line can be modeled as lumped elements:

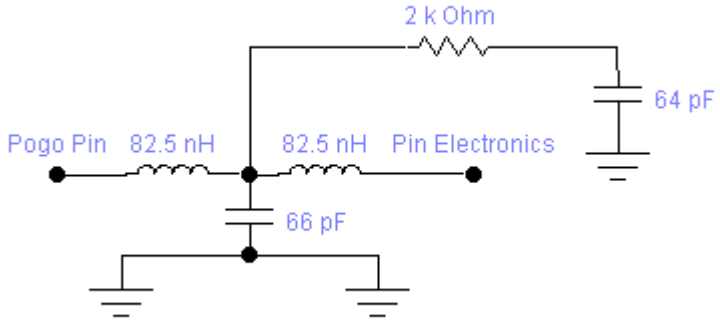
Standard Channel



Total capacitance on the path: 66pf typical

Total inductance in series with the path 175 nH typical

High Voltage Channel



3.2.5 Comparator Waveform Fidelity

When Driven from a 50ohm source:

From 1ns to 15 ns after transition.	< (10% delta V)
From 15ns to 500ns after transition.	< (0.5% delta V + 20 mV)
Pre-shoot up to 2 ns before transition	< (10% delta V)

Transition is defined as the 80% point on the input waveform.

Valid when levels are more than 1 volt from either rail.

(Driven by a backmatched source, Channel's driver in HIZ)

Input Minimum Pulse Width	2 ns Minimum
Minimum pulse detectable with comparators	2 ns @ 500 mV overdrive
Receiver Hysteresis	2 mV typical

3.3 DYNAMIC LOAD SPECIFICATIONS

3.3.1 IOL and IOH Current Levels

Range	Resolution	Accuracy
50ua to 50ma	5ua	±(0.2% + 50 uA)

3.3.2 Theshhold (Vt) Voltage Levels

Range	Resolution	Accuracy (with no external load)
-1 to +7 volts	1mv	±40mV

The Iload will reach 90% of the programmed current level for Vt = 0.2 volts + abs(Iload) * 10 ohms

Thus if the Iload is set to -10 mA, the VCOM voltage is 0.2 + 10e-3 * 10 = 0.3 volts.

3.3.3 Load Input Resistance, DC

The active load can be used to terminate the channel's transmission line if IOH and IOL are programmed to an appropriately large value and Vt is programmed to the desired termination voltage.

RIload<15 ohms for Iload >4 mA.

3.3.4 Settling Time

IOH/IOL settles to within ±10% of programmed value after transition through Vt. (10 ns typical)

3.4 Voltage Clamps

Level	Range	Resolution	Accuracy

Clamp Low Vcl	-2.6to +5 volts	1mv	±100mV
Clamp High Vch	0 to +7.6 volts	1mv	±100mV

The voltage clamps are used to reduce overshoot when the device drives the tester, yet are always present. On a drive-only pin, they are set to –2.6V and +7.6V at job plan start. The nominal impedance is TBD ohms with the clamp on >10ma. The Vcl (Clamp Low) must be less than or equal to Vch (Clamp High)

3.5 High Voltage Drivers

3.5.1 Channels

High voltage drivers are available on channels 0, 4, 32, 36 of each channel board

3.5.2 Voltage range (Vihh)

Range	Resolution	Accuracy
0 to +16 V	± 33 mV	± 100 mV (Vih, Vil accuracy: ± 20 mV)

3.5.3 Rise Time

Range	Resolution	Accuracy
1us	1us	± 0.5μsec
2 to 16 us	1us	± 1 μsec

3.5.4 Current Limit

Range	Resolution	Accuracy
0 to 100 mA	0.5 mA	± 20 mA

3.5.5 Current Sink Capability

2.5 mA minimum

3.5.6 Maximum Overshoot

0.1 volts

3.5.7 Maximum Source Impedance

6 ohms

4. PIN PARAMETRIC MEASUREMENT UNIT (PPMU)

A four quadrant Force Voltage and Measure Current or Force Current and Measure Voltage parametric measurement circuit is available per-pin. It is connected via a relay to the pogo pin.

Note: Positive current flows from the tester into the DUT.

Level Change settling time 1.28ms, for Forcing levels.

4.1 Voltage Forcing/Measuring (No load)

Range	Resolution (12 bits)	Accuracy
-2 to +7 volts Forcing	2mv	±(0.16% + 14 mV)
-2 to +7 volts Measuring	2mv	±(0.43% + 18 mV)

4.2 Current Forcing Ranges

Range	Resolution (12 bits)	Accuracy
± 2 mA	1 uA	±(0.25% + 17 uA)
±200 uA	100 nA	±(0.2% + 1.7 uA)

4.3 Current Measuring Ranges

Range	Resolution (12 bits)	Accuracy	Time
± 2 mA	1 uA	±(0.58% + 16 uA)	
± 200 uA	100 nA	±(0.52% + 2.1 uA)	
± 20 uA*	10 nA	±(0.51% + 0.16 uA)	1 ms
± 2 uA*	1 nA	±(1.0% + 40 nA)	10 ms
± 200 nA*	100 pA	±(1.4% + 8 nA)	100 ms

* Integrating current measurement ranges

5. TIMING GENERATION

5.1 Clock Generation

The system timing is derived from a 100MHZ clock.

Frequency Accuracy	15 ppm + 5 ppm/year

5.2 Period Generation

Frequency Range	100Hz to 100MHz
Period Range	10ns to 10ms
Resolution	37.2529E-18 Sec (10ns / 2**28)
Number of timing values	32

5.3 Multiple Clocks

When the system is in Extended Mode, each channel can select either C0 (MCG mode) or T0 (normal mode) as its cycle clock. This allows clock channels to operate at a higher rate than data channels. Channels operating in this mode must be drive only.

Clocks-per-period Divider range 1 to 1000

Number of divider values	32

5.4 Edge Generation

5.4.1 Timing Generators per Channel (normal mode)

Up to three edges can be active per cycle per channel. Several of the edges have multiple functions depending on the mode selected for the channel.

5.4.1.1 Drive Cycle Edges

Edge Name	Function
D0	Drive active and if format is surround also go to surround data.
D1	Drive to the data value.
D2	Drive to return or surround data

5.4.1.2 Receive Cycle Edges

Edge Name	Function
D3	Go to HIZ.
R0	Strobe comparator.

5.4.2 Timing Generators per Channel (extended mode)

Up to six edges can be active per cycle per channel. Several of the edges have multiple functions depending on the mode selected for the channel. The period must be greater than or equal 20 ns.

5.4.2.1 Drive or Receive Cycle Edges

Edge Name	Function
D0	Drive active and if format is surround also go to surround data
D1	Drive to the data value.
D2	Drive to return or surround data
D3	Go to HIZ if next cycle is a receive cycle
R0	Open compare window or edge strobe
R1	Close compare window

5.5 Timing Sets

Timing Sets are values referenced by vectors. Each timing set contains a per-pin index of an edge set, and an index to a period value.

5.5.1 Number of timing sets

There are 256 global timing sets or TSETs. Each TSET number selects one of 32 edge sets of timing per channel, and period timing. TSETs can be changed on the fly on each vector. Said another way, the vectors can have 256 unique timing combinations in a single burst. One pin can have 32 unique timing values.

5.5.2 Formatting Capabilities

The whole system is placed in Normal mode or Extended mode for an entire burst. Each cycle is either a drive cycle or a compare cycle. Several drive and compare formats are supported both statically and dynamically.

5.6 Drive Formats

Format Name	Function
NR	Non Return.
RL,SBL	Return To Low, Surround by Low
RH, SBH	Return To High, Surround by High
SBC	Complement Surround
COPY	Repeat the previous cycle's waveform
STAY	Generate no edges
OFF	Disable Driver

The data may be All high, All Low or from the pattern or the complement of the pattern, yielding the following additional formats:

RL + High	Clock High independent of pattern data
RH + Low	Clock Low independent of pattern data
NR + High	Static drive high independent of pattern data
NR + Low	Static drive low independent of pattern data

5.7 Compare Formats

Code	Function
Edge	Compare to Pattern Data, Edge timing
Window	Compare to Pattern Data, Window timing (Extended mode)
Off	Mask Comparator, Inhibits Pass/fail Comparisons

5.8 Pass/Fail Generation

Pass/Fail status will be generated for each compare cycle that has a R0 edge. All other cycles generate a default "Pass" status..

HIGH	Above the high comparator (VOH)
LOW	Below VOL.
MIDBAND	Below VOH and above VOL.
VALID	Above VOH or below VOL.

5.9 Channel Output Initialization

Prior to a pattern burst each channel can be initialized to a user specified condition: Driver LOW, HIGH or HIZ. At the start of a pattern burst the system will initialize all channels to: HIGH, LOW or HIZ depending on what the first vector's pattern data is.

5.10 Edge Range

Minimum	0 ns
Maximum, the smaller of either:	2*(Tester Cycle) (Extended Mode)
Maximum, the smaller of either:	4*(Tester Cycle) (Normal Mode)
or:	10.00us.

5.10.1 Edge Resolution

Edge Resolution	39.0625ps (Guaranteed by design)

5.11 Edge Placement Accuracy

Edge accuracy applies at the device socket. However, the device interface board, DIB, must be time calibrated and the digital signal traces on the DIB must have a 50 ohm impedance.

D1,D2	± 500 ps	
R0 Edge (Edge mode)	± 500 ps	
R0,R1 (Window mode)	± 1000 ps	
D0 Edge	Used as Complement Edge	± 500ps
D0,D3 Edge	Used as HIZ Edge	± 1000 ps

5.11.1 Edge Restrictions

This is the time required between the generation of any edge and the next occurrence of the same edge on the same channel. (ie. D1 to the next D1).

Edge Regeneration time	<10ns

When operating a channel pair in multiplexed mode, the odd channel of the pair must have its edges programmed to occur first in time relative to the even channel's edges. This is required for I/O cycles to properly handle the transitions from drive cycles to receive cycles and vice versa.

6. DIGITAL VECTORS

6.1 Number Of Digital Vectors

Subroutine vector memory SVM	1K x 3 bits/channel
Large vector memory LVM	4 Meg x 3 bits/channel
optional LVM	16 Meg x 3 bits/ channel

The memory architecture consists of a mixture of random access memory and large vector memory. Patterns are automatically split up between the two memories by the system software. Pattern writing and debugging are both performed on a virtual vector pattern space.