摘 要

惯性导航系统也被称为惯性参考系统，它具有相当多的优点，能够在水下等极端的条件下工作，因此惯导在军工中应用广泛。惯性导航技术的核心部分是模数转换器（Analog-to-digital，ADC），模数转换器是连接模拟世界和数字世界的桥梁，模数转换器的精度决定了惯性导航的定位准确度。Sigma-Delta 型 ADC 采用过采样技术，信噪比和转换精度更高，Sigma-Delta 型 ADC 中的数字抽取滤波器主要决定了整个系统的功耗和面积。

本文主要关注 Sigma-Delta 型 ADC 中数字抽取滤波器的设计工作，首先对 Sigma-Delta 型 ADC 的工作原理进行了阐释，着重介绍了数字抽取滤波器的原理和降采样技术。根据前级调制器的设计，滤波器选择了 3 阶 CIC 滤波器级联补偿滤波器的结构，根据字长定理计算出滤波器的输出位宽，设计滤波器的各项性能参数，实现了 Matlab\Simulink 仿真，通过编写 Verilog 代码实现了 RTL 级仿真验证，在 Cadence 平台实现了数模混仿，得到的波形符合设计期望。

本文最终实现 256 倍降采样的数字抽取滤波器，将调制器的一位输出码流还原为 60Hz 信号，实现了良好的高频噪声滤除。本文实现了时钟电路设计，产生了两相不交叠时钟。

关 键 词：Sigma-Delta ADC；数字抽取滤波器；级联积分梳状滤波器；降采样

ABSTRACT

The inertial navigation system is also known as the inertial reference system. It has many advantages and can work under extreme conditions such as underwater. Therefore, the inertial navigation system is widely used in military industry.The core part of the inertial navigation technology is the analog-to-digital converter (ADC). The analog-to-digital converter is a bridge between the analog world and the digital world. The accuracy of the analog-to-digital converter determines the positioning accuracy of inertial navigation.The sigma-delta ADC adopts the over-sampling technology, with higher signal-to-noise ratio and conversion accuracy. The digital extraction filter in the sigma-delta ADC mainly determines the power consumption and area of the whole system.

This focuses on the design of digital extraction filter in sigma-delta ADC. Firstly, the working principle of sigma-delta ADC is explained, and the principle of digital extraction filter and down-sampling technique are emphatically introduced.According to the structure in design of the modulator ,3 order structure of CIC filter cascaded compensation filter is finally selected.According to the law of word length,output bits wide is calculated and various performance parameters of the filter are designed.The simulation of Matlab/Simulink is realized, and through designing the Verilog code the RTL simulation is implemented successfully,and the D/A mixed imitation is realized inthe Cadence platform, and the waveform meets the design expectations.

In this, a digital extraction filter with 256 reduction sampling is finally implemented, and the one-bit output code stream of the modulator is reduced to a 60Hz signal, achieving good high-frequency noise filtering.In this thesis, the clock circuit design is realized, and the two - phase non - overlapping clock is produced.

KEY WORDS: Sigma-Delta ADC; Digital extraction filter; Cascade Integrator Comb; Downsampling

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