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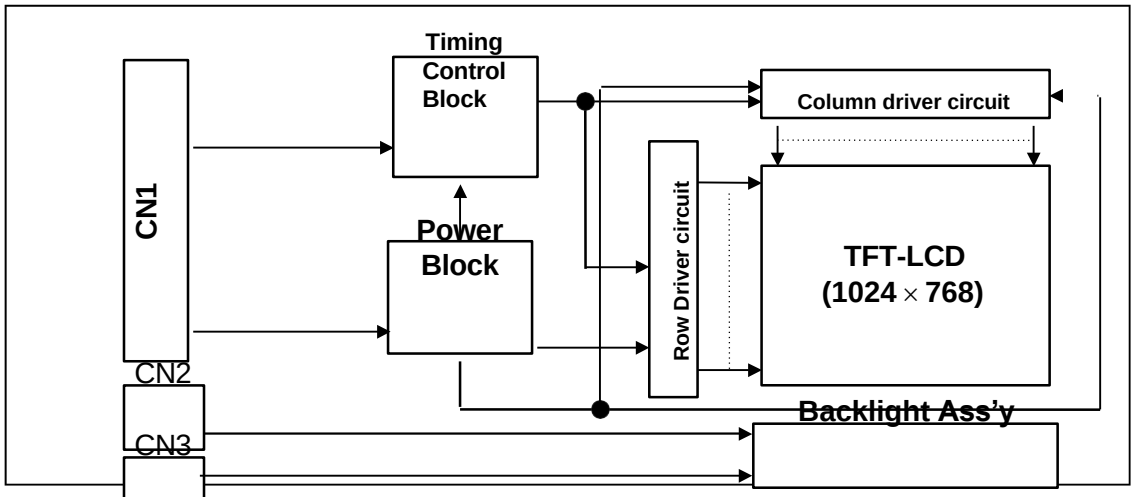
HLD 1511
15.1“ XGA TFT LCD

PRELIMINARY SPECIFICATION

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1. GENERAL DESCRIPTION

The HLD 1511 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp(CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has a 15.1 inchs diagonally measured active display area with XGA resolution (768 vertical by 1024 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors.
The HLD 1511 has been designed to apply the TTL interface method.
The HLD 1511 LCD is intended to support applications where high brightness, wide viewing angle, high color saturation, and high color depth are very important. In combination with the vertical arrangement of the sub-pixels, the HLD 1511 characteristics provide an excellent flat panel display industrial applications.



1.1 General Features

Active screen size	15.1 inches (307.2 x 230.4 mm) diagonal
Outline dimensions	352.0 (H) × 263.5 (V) × 18.5 (D) mm (typ) without user connector
Pixel pitch	0.300 mm × 0.300 mm
Pixel format	1024 horiz. By 768 vert. Pixels RGB stripe arrangement
Color depth	6-bit, 262.144 colors
Luminance,White	250 cd/m^2 (typ)
Power Consumption	2.3 Watts Logic / 9.7 Watts CCFL (typ. with 64 Gray pattern)
Weight	1500g (typ)
Display operating mode	transmissive mode, normally white
Surface treatments	hard coating (3H), anti-glare treatment of the front polarizer

2. ABSOLUTE MAXIMUM RATINGS

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1 ABSOLUTE MAXIMUM RATINGS

Parameter	symbol	Values		Units	Notes
		Min.	Max.		
Power Input Voltage	**V_{CC}**	**-0.5**	**+3.6**	**Vdc**	**at 25°C**
Operating Temperature	**T_{OP}**	**-10**	**+60**	**°C**	**1,2**
Storage Temperature	**T_{ST}**	**-25**	**+70**	**°C**	**1,2**

Note 1: Temperature at 5 mm above display center of LCD Module.
Ta ≤ 40 °C: 90% RH Max.
Ta > 40 °C: Absolute Humidity shall be less than Ta = 40 °C 90 % RH.
These shall be no dew condensation.
Note 2: Humidity Min. 5% RH, Max. 90 % RH

3. ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics

The HLD 1511 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2 ELECTRICAL CHARACTERISTICS:

Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
MODULE:						
Power Supply Input Voltage	V_{CC}	TBD	3.3	TBD	Vdc	
Power Supply Input Current	I_{CC}	-	TBD	TBD	A	1
Power Consumption	P_c	-	2.1	3.3	Watts	1
Input Data Logic Voltage	Vi	TBD	3.3	TBD	Vdc	
LAMP						
Operating Voltage	V_{BL}	585(9mA)	605(8mA)	720(3mA)	V_{RMS}	2
Operating Current	I_{BL}	3.0	8.0	9.0	mA	
Established Starting Voltage	V_{BS}					3
at 25 °C		-	-	1020	V_{RMS}	
at 0 °C		-	-	1400	V_{RMS}	
Operating Frequency	f_{BL}	30	50	60	kHz	
Power Consumption	P_{BL}	-	9.7	10.6	Watts	4
Half Life Time		30,000	-	-	Hrs	5

Note 1: The specified current and power consumption are under the Vcc = 3.3V, 25 °C, fv = 60Hz condition Power supply input current and Typ. Power consumption is measured while 64 gray pattern is displayed. The max. power consumption is measured while full black pattern is displayed.

Note 2: The variance of the voltage is ± 10 %.
Note 3: The transformer output voltage in the inverter must be high considering to the loss of the ballast capacitor in the inverter.
Note 4: The lamp power consumption shown above does not include loss of external inverter.
Note 5: The life time is determined as the time at which brightness of lamp is 50 % compare to that of initial value at the typical lamp current on condition of continuous operating at 25 ± 2 °C.

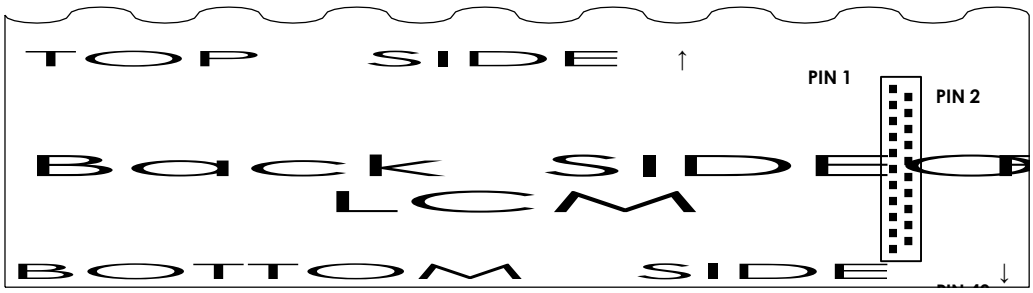
3.2 Interface Connections

This LCD employs three interface connections, a 41 pin connector is used for the module electronics and two connectors, a three pin connector, are used for the integral backlight system.
The electronics interface connector is a model DF9B-41P-1V manufactured by Hirose. The pin configuration for the connector is shown in the table below

Table 4 MODULE CONNECTOR PIN CONFIGURATION

Pin	Symbol	Description	Pin	Symbol	Description
	GND	System Ground. Note 1	2	DCLK	Data Input Clock
	GND	System Ground	4	H_{sync}	H_{sync}. Horizontal Sync Signal
	V_{sync}	V_{sync}. Vertical Sync Signal	6	GND	System Ground
	GND	System Ground	8	GND	System Ground
	R0	Red data 0 (LSB)	10	R1	Red data 1
	R2	Red data 2	12	GND	System Ground
	R3	Red data 3	14	R4	Red data 4
	R5	Red data 5 (MSB)	16	GND	System Ground
17	GND	System Ground	18	GND	System Ground
19	G0	Green data 0 (LSB)	20	G1	Green data 1
21	G2	Green data 2	22	GND	System Ground
23	G3	Green data 3	24	G4	Green data 4
25	G5	Green data 5 (MSB)	26	GND	System Ground
27	GND	System Ground	28	GND	System Ground
29	B0	Blue data 0 (LSB)	30	B1	Blue data 1
31	B2	Blue data 2	32	GND	System Ground
33	B3	Blue data 3	34	B4	Blue data 4
35	B5	Blue data 5 (MSB)	36	GND	System Ground
37	DE	Data Enable Signal	38	V_{DD}	Power Supply for LCD Module
39	V_{DD}	Power Supply for LCD Module	40	V_{DD}	Power Supply for LCD Module
41	V_{DD}	Power Supply for LCD Module			

Note 1: All GND (ground) pins should be connected together and to Vss which should also be connected to the LCD's metal frame.
Note 2: All V_{CC} (power input) pins should be connected together.



The backlight interface connector is a model BHR-03VS-1, manufactured by JST. The mating connector part number is SM02(8.0)B-BHS-1-TB or equivalent. The pin configuration for the connector is shown in the table below.

Table 5 BACKLIGHT CONNECTOR PIN CONFIGURATION

Pin	Symbol	Description	Notes
1	HV	Lamp power input(High)	1
2	NC	No connect	
3	LV	Lamp power input(Low)	

Note 1: The input power terminal(High) is colored pink.

3.3 Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

Table 6 Timing Table

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Dclk	Frequency	t_{CLK}	-	65.0	78.75	Mhz	
	Width-Low	T_{WCL}	5	-	-	ns	
	Width-High	T_{WCH}	5	-	-	ns	
Hsync	Period	t_{HP}	1056	1344	-	t_{CLK}	
	Width-Active	t_{WH}	8	136	-		
	Setup time	t_{HC}	4	-	-	ns	For DCLK
Vsync	Period	t_{VP}	777	806	-	t_{HP}	
	Frequency	f_V	-	60	75	Hz	
	Width-Active	t_{WV}	1	-	-	t_{HP}	
DE (Data Enable)	Horizontal Back Porch	t_{HBP}	8	-	-	t_{CLK}	
	Horizontal Front Porch	t_{HFP}	8	-	-		
	Vertical Back Porch	t_{VBP}	1	-	-	t_{HP}	
	Vertical Front Porch	t_{VFP}	1	-	-		
	Set up time	t_{SI}	5	-	-	ns	For DCLK
	Hold time	t_{HI}	5	-	-	ns	For DCLK
DATA	Set up time	t_{SD}	3.5		-	ns	For DCLK
	Hold time	t_{HD}	3.5	-	-	ns	For DCLK

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