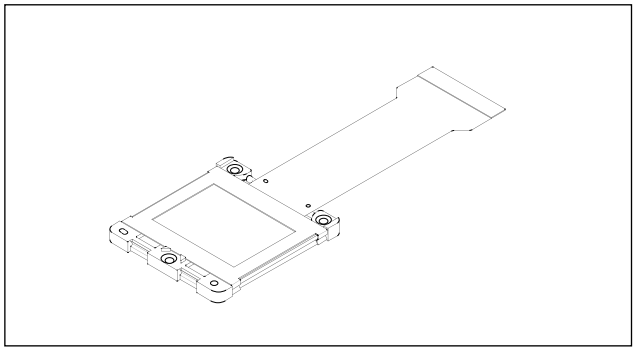
SONY

LCX016AL

3.3cm (1.3-inch) Black-and-White LCD Panel



Description

The LCX016AL is a 3.3cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with a built-in peripheral driving circuit. Use of three LCX016AL panels provides a full-color representation. The striped arrangement suitable for data projectors is capable of displaying fine text and vertical lines.

The adoption of an advanced on-chip black matrix realizes high picture quality without cross talk by incorporating a high luminance screen and cross talk free circuit.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

The panel contains an active area variable circuit which supports Macintosh17*1/SVGA/VGA/PC98*2 data signals by changing the active area according to the type of input signal. In addition, double-speed processed NTSC/PAL can also be supported.

*1 "Macintosh" is a treadmark of Apple Computer, Inc.

*2 "PC98" is a treadmark of NEC Corporation.

Features

- Number of active dots: 519,000 (1.3-inch, 3.3cm in diagonal)
- Accepts the computer requirements of Macintosh17 (832 × 624), SVGA (800 × 600), VGA (640 × 480) and PC98 (640 × 400) platforms
- Supports NTSC (640 × 480) and PAL (762 × 572) by processing the video signal at double speed
- High optical transmittance: 20% (typ.)
- Built-in cross talk free circuit
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function

Element Structure

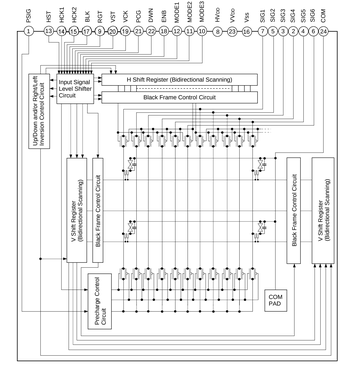
- Dots: 832 (H) × 624 (V) = 519,168
- Built-in peripheral driver using polycrystalline silicon super thin film transistors

Applications

- Liquid crystal data projectors
- Liquid crystal projectors, etc.

E96220-ST

Block Diagram



Absolute Maximum Ratings (V_{SS} = 0V)

• H driver supply voltage	HV_{DD}	–1.0 to +20	V
• V driver supply voltage	VV_{DD}	–1.0 to +20	V
• Common pad voltage	COM	–1.0 to +17	V
• H shift register input pin voltage	HST, HCK1, HCK2, RGT	–1.0 to +17	V
• V shift register input pin voltage	VST, VCK, PCG, BLK, ENB, DWN MODE1, MODE2, MODE3	–1.0 to +17	V
• Video signal input pin voltage	SIG1, SIG2, SIG3, SIG4, SIG5, SIG6, PSIG	–1.0 to +15	V
• Operating temperature	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions (V_{SS} = 0V)

• Supply voltage

HV_{DD} 15.5 ± 0.3V

VV_{DD} 15.5 ± 0.3V

• Input pulse voltage (Vp-p of all input pins except video signal and uniformity improvement signal input pins)

Vin 5.0 ± 0.5V

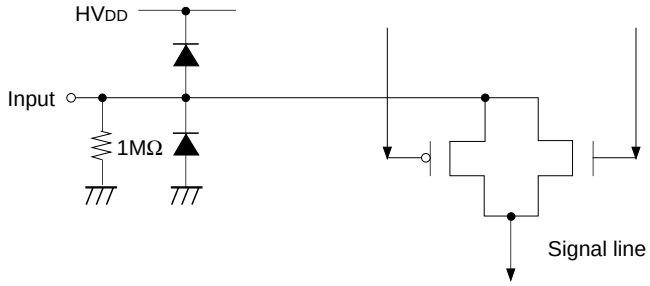
Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	PSIG	Uniformity improvement signal	13	HST	Start pulse for H shift register drive
2	SIG4	Video signal 4 to panel	14	HCK1	Clock pulse for H shift register drive
3	SIG3	Video signal 3 to panel	15	HCK2	Clock pulse for H shift register drive
4	SIG5	Video signal 5 to panel	16	Vss	GND (H, V drivers)
5	SIG2	Video signal 2 to panel	17	BLK	Black Frame display pulse
6	SIG6	Video signal 6 to panel	18	ENB	Enable pulse for gate selection
7	SIG1	Video signal 1 to panel	19	VCK	Clock pulse for V shift register drive
8	HV_{DD}	Power supply for H driver	20	VST	Start pulse for V shift register drive
9	RGT	Drive direction pulse for H shift register (H: normal, L: reverse)	21	PCG	Improvement pulse for uniformity
10	MODE3	Display area switching 3	22	DWN	Drive direction pulse for V shift register (H: normal, L: reverse)
11	MODE2	Display area switching 2	23	VV_{DD}	Power supply for V driver
12	MODE1	Display area switching 1	24	COM	Common voltage of panel

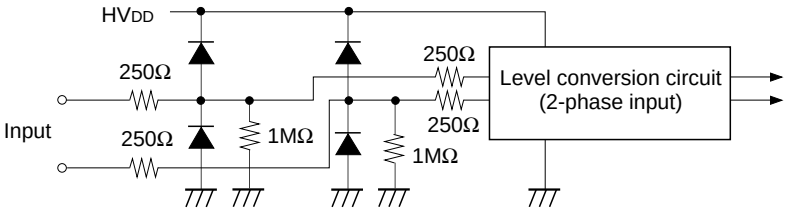
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal inputs. All pins are connected to Vss with a high resistor of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistance value: typ.)

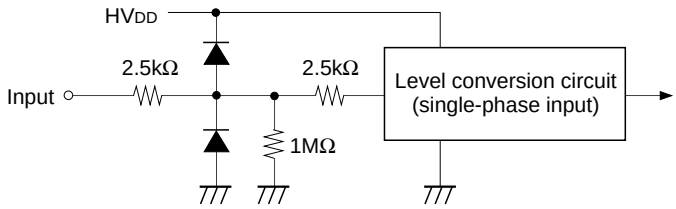
(1) SIG1, SIG2, SIG3, SIG4, SIG5, SIG6, PSIG



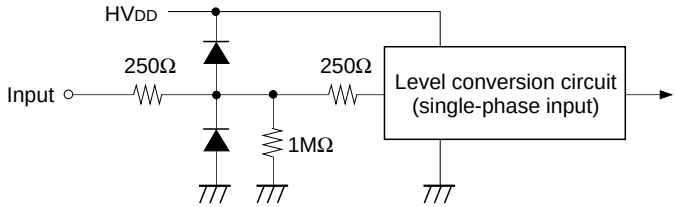
(2) HCK1, HCK2



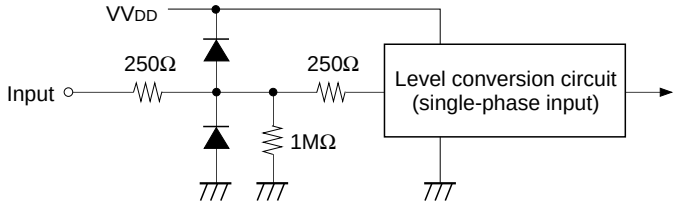
(3) RGT



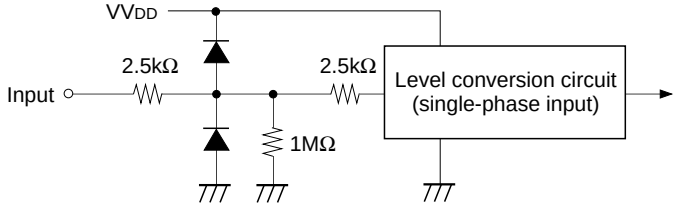
(4) HST



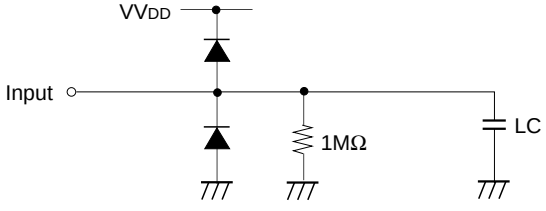
(5) PCG, VCK



(6) VST, BLK, ENB, DWN, MODE1, MODE2, MODE3



(7) COM



Input Signals

1. Input signal voltage conditions (V_{SS} = 0V)

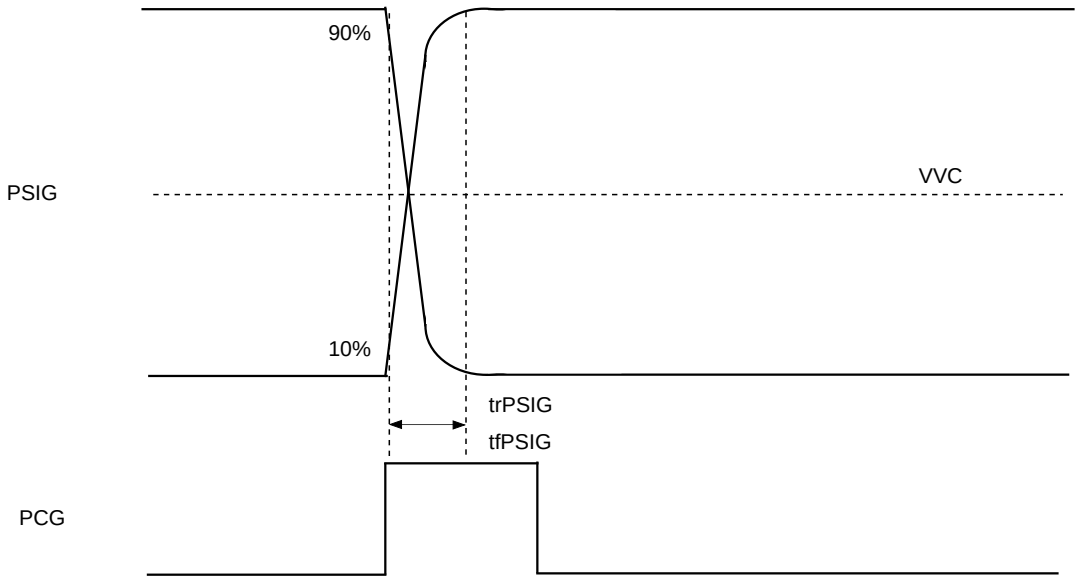
Item		Symbol	Min.	Typ.	Max.	Unit
H shift register input voltage HST, HCK1, HCK2, RGT	(Low)	VHIL	–0.5	0.0	0.4	V
	(High)	VHIH	4.5	5.0	5.5	V
V shift register input voltage MODE1, MODE2, MODE3, BLK, VST, VCK, PCG, ENB, DWN	(Low)	VVIL	–0.5	0.0	0.4	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC	6.8	7.0	7.2	V
Video signal input range*1		Vsig	VVC – 4.5	7.0	VVC + 4.5	V
Common voltage of panel*2		Vcom	VVC – 0.5	VVC – 0.4	VVC – 0.3	V
Uniformity improvement signal input voltage (PSIG)*3		Vpsig	VVC ± 4.3	VVC ± 4.5	VVC ± 4.7	V

*1 Input video signal shall be symmetrical to VVC.

*2 The typical value of the common pad voltage may lower its suitable voltage according to the set construction to use. In this case, use the voltage of which has maximum contrast as typical value.
When the typical value is lowered, the maximum and minimum values may lower.

*3 Input a uniformity improvement signal PSIG in the same polarity with video signals SIG1 to 6 and which is symmetrical to VVC. Also, the rising and falling of PSIG are synchronized with the rising of PCG pulse, and the rise time trPSIG and fall time tfPSIG are suppressed within 800ns (as shown in a diagram below).

Input waveform of uniformity improvement signal PSIG



Level Conversion Circuit

The LCX016AL has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD}. The V_{CC} of external ICs are applicable to 5 ± 0.5V.

2. Clock timing conditions (Ta = 25°C) (Macintosh17 mode: fHCKn = 4.8MHz, fVCK = 24.9kHz)

	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data set-up time	tdHst	70	80	90	
	Hst data hold time	thHst	15	25	35	
HCK	Hckn rise time*4	trHckn	—	—	30	
	Hckn fall time*4	tfHckn	—	—	30	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
VST	Vst rise time	trVst	—	—	100	
	Vst fall time	tfVst	—	—	100	
	Vst data set-up time	tdVst	5	10	15	µs
	Vst data hold time	thVst	5	10	15	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	
	Enb fall time	tfEnb	—	—	100	
	Vck rise/fall to Enb rise time	tdEnb	400	500	600	
	Enb pulse width	twEnb	2400	2500	2600	
PCG	Pcg rise time	trPcg	—	—	30	
	Pcg fall time	tfPcg	—	—	30	
	Pcg fall to Vck rise/fall time	toVck	900	1000	1100	
	Pcg pulse width	twPcg	1100	1200	1300	
BLK*5	Blk rise time	trBlk	—	—	100	
	Blk fall time	tfBlk	—	—	100	
	Blk fall to Vst rise time	toVst	32	33	34	µs
	Blk pulse width	twBlk	20	21	22	

*4 Hckn means Hck1 and Hck2.

*5 Blk is the timing during SVGA mode (fHckn = 4.0MHz, fVck = 24.0kHz).