RF / Microwave PC Board
Design and Layout
Base Materials for High Speed, High Frequency PC Boards
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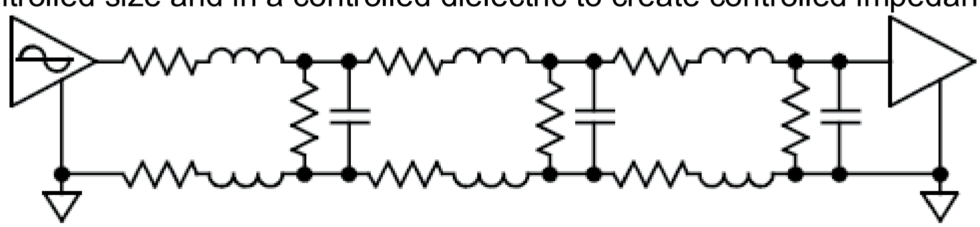
RF / Microwave Design – Basics

- Unlike digital, analog signals can be at any voltage and current level (between their min & max), at any point in time.
- Standard analog signals are assumed to be between DC and a few hundreds of MHz.
- RF/Microwave signals are one frequency or a band of frequencies imposed on a very high frequency carrier.
- RF/Microwave Circuits are designed to pass signals within band of interest and filter energy outside that range.
- Signal band can be narrow or wide.
  - Narrow band circuits usually have pass band less than 1 MHz.
  - Broad band circuits pass a range of frequencies up to tens of MHz.
- When digital and microwave exist in the same unit, pass bands of microwave circuits usually fall (by design) outside the harmonic range of the digital signals.
- RF / Microwave PC Board layout simply follows the "Laws of Physics"-
- When laws of physics can't be followed, know what compromises are available.
- Microwave signals are very sensitive to noise, ringing and reflections and must be treated with great care.
- Need complete impedance (Zo) matching (50 ohm out/ 50 ohm line/ 50 ohm in).
  - Minimizes Return Loss / VSWR.
- A Transmission Line is any pair or wires or conductors used to move energy from point A to point B, usually of controlled size and in a controlled dielectric to create controlled impedance (Zo).



Evenly Distributed R, L, G & C – $Zo=\sqrt{\frac{R}{G}+\frac{j\omega L}{j\omega C}}$

- Inductance (L) is determined by the loop function of signal and return path.
  - Small spacing (tight loop) creates high flux cancellation, hence low inductance.
- Capacitance (C) is function of signal spacing to the return path.
  - Small spacing creates high capacitance.
- Since small spacing (tight loop) creates low L & high C, and since:
  - $Zo = \sqrt{L/C}$, small spacing creates low Zo.
- Additionally, Zo is function of signal conductor width & thickness and a function of the DK dielectric constant (Er) of the material surrounding the lines.
- Sometimes dielectric surrounding transmission line isn't constant (outer layer trace on PCB).
  - DK above trace is Air (= 1.0008).
  - DK below trace is FR4 (approx = 4.1).
  - Effective Relative Er (Er_eff) is 3 to 3.25.
- Signal return currents follow the path of least impedance (in high frequency circuits that = path of least inductance).

- Whenever we neglect to provide a low impedance return path for RF / Microwave signals, they WILL find a path.
- It may NOT be what we had in mind.
- Signal Wavelength -
  - Wavelength (λ) of a signal is the distance it travels in the time of one cycle.
- For a signal traveling in free space -
  - λ = c (speed of light) / f (frequency), (λ = 11.78"/nsec at 1GHz = 11.78")
- Signal in a higher dielectric - $\lambda = c / [f \cdot (1 / \sqrt{Er})]$
- Signal critical length
  - How long a PCB trace can be before we MUST pay attention to impedance control?
  - Function of frequency (1/16th wavelength)

$$L_{critical} = \frac{c}{f} \bullet \frac{1}{\sqrt{\varepsilon_{eff}}} \bullet \frac{1}{16}$$

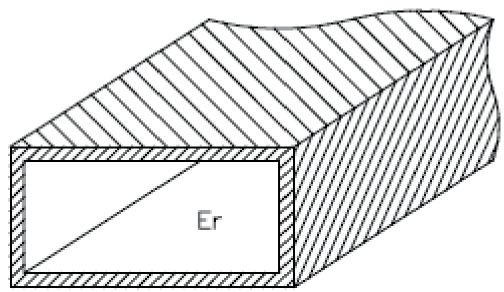
At 1 GHz = approx .425" (microstrip- FR4)
At 1 GHz = approx .375" (stripline - FR4)

Signal Loss / Noise

- Reflections -
  - Return Loss / VSWR
- Skin Effect -
  - Increased resistance of PCB trace due to decreased cross sectional area.
  - In analog circuits above 100 MHz.
  - Skin depth - 0.000822" @ 10 MHz and 0.000026" @ 10 GHz.
- Loss Tangent -
  - Dielectric Loss caused by molecular structure of board material.
  - In analog circuits above 200 MHz.
  - PTFE's far better than FR4.
- Energy Coupling-
  - Cross Talk.
  - Noise Induction.

Line Types and Impedance (Zo)

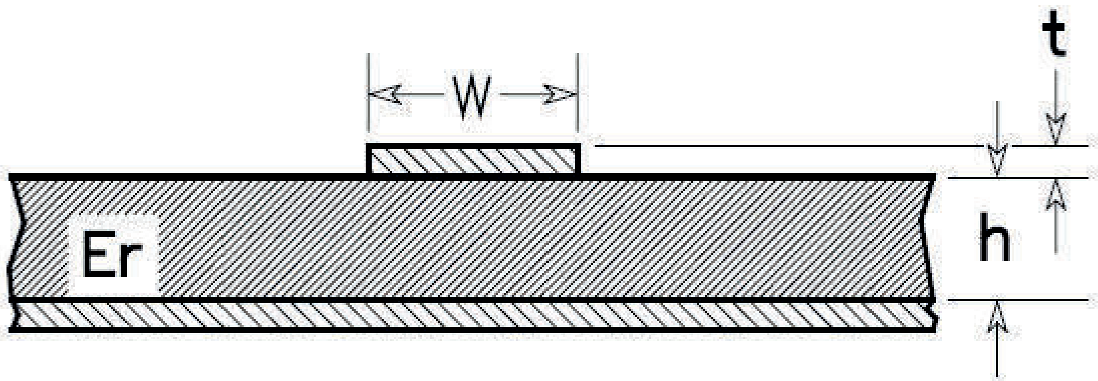
- Waveguide



  - Uses air as transmission medium and side walls of tube as return path.
  - Won't support energy propagation below cutoff frequency.
  - Works best at ultra high frequencies with millimeter wavelengths.
  - With an air dielectric, signals propagate at the speed of light.
  - Very low loss due to smooth side walls and the air dielectric.
  - Ultra low loss with high density, ultra smooth coating on walls.
  - In very high power applications, uses solid dielectric to prevent voltage arcing.
- Signal traces longer than critical length (1/16 λ in DK) need impedance control to prevent return loss due to reflections.

- Shorter circuit elements don't require impedance control, but it usually does NO harm.
- Don't bother to Zo control, short lines if it will create a problem (ie- DFM – Design for Manufacturing).
- Impedance (L/C)-
  - Lower Er materials - net higher impedance traces and faster propagation times per given trace width & trace-to-ground separation.
  - As trace width increases, trace impedance decreases (thickness has min effect).
  - As trace spacing from ground increases, impedance increases.

Microstrip



$$Z_0 = \frac{120\pi}{2.0\sqrt{2.0}\pi\sqrt{\varepsilon_r + 1.0}} \ln\left\{1.0 + \frac{4.0h}{w'}\left[\frac{14.0 + 8.0/\varepsilon_r}{11.0}\frac{4.0h}{w'} + \sqrt{\left(\frac{14.0 + 8.0/\varepsilon_r}{11.0}\right)^2\left(\frac{4.0h}{w'}\right)^2 + \frac{1.0 + 1.0/\varepsilon_r}{2.0}\pi^2}\right]\right\}(\Omega)$$

where: $w' = w + \Delta w'$

$$\Delta w' = \Delta w\left(\frac{1.0 + 1.0/\varepsilon_r}{2.0}\right)$$

$$\frac{\Delta w}{t} = \frac{1.0}{\pi}\ln\left[\frac{4e}{(t/h)^2 + \left(\frac{1/\pi}{w/t + 1.1}\right)^2}\right]$$

(Replace Er with Eeff)

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \bullet \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \quad \text{if} \quad \frac{w}{h} < 1$$

otherwise

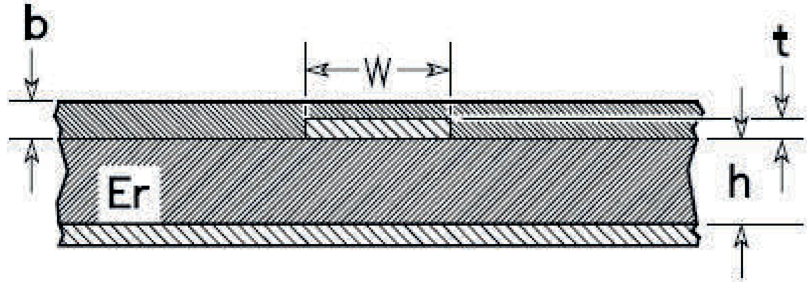
$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{eff}}} \bullet \frac{1}{\left(\frac{w}{h} + 1.393 + 0.677 \bullet \ln\left(\frac{w}{h} + 1.444\right)\right)}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1+\frac{12h}{w}}} + 0.04\left(1-\frac{w}{h}\right)^2\right] \quad \underline{\text{if}} \quad \frac{w}{h} < 1$$

<u>otherwise</u>

$$\varepsilon_{eff} = \left[\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1+\frac{12h}{w}}}\right]\right]$$

<u>Embedded Microstrip</u>

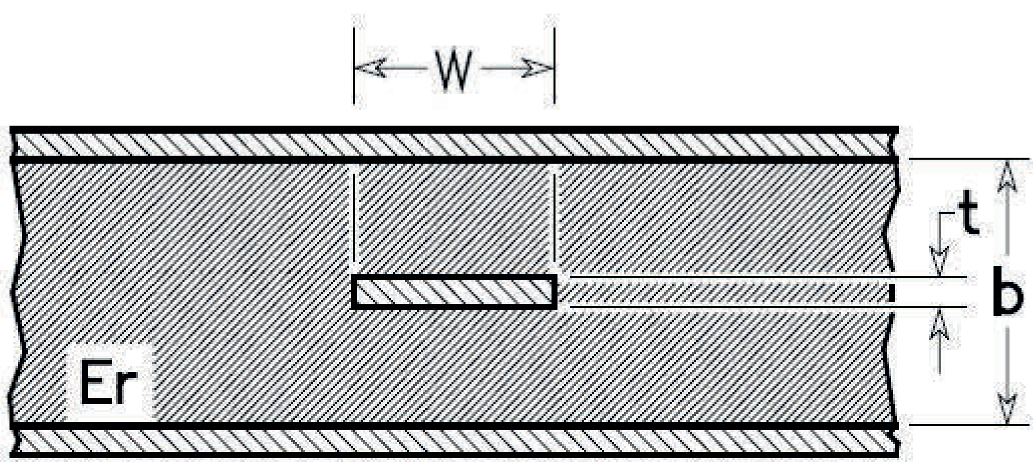


Multiply Zo (from Microstrip) by -

$$\frac{\varepsilon_{eff}}{\varepsilon_{eff} \cdot e^{(-2.0b/h)} + \varepsilon_r\left[1.0 - e^{(-2.0b/h)}\right]}$$

Can use w/Soldermask over Microstrip (Often NOT Needed)

<u>Centered Stripline</u>



$$Z_0 = \frac{120\pi}{2.0\pi\sqrt{\varepsilon_r}} \ln\left\{1.0 + \frac{4.0(b-t)}{\pi w'}\left[\frac{8.0(b-t)}{\pi w'} + \sqrt{\left(\frac{8.0(b-t)}{\pi w'}\right)^2 + 6.27}\right]\right\}$$

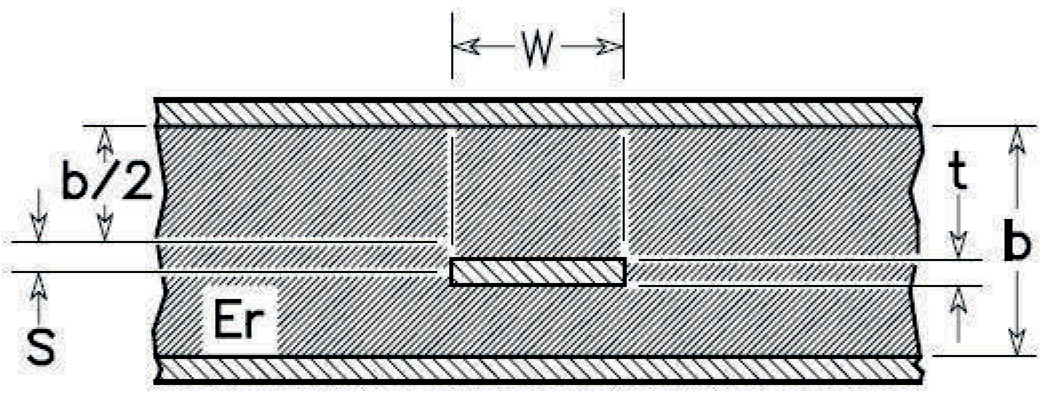
where:

$$b = 2.0h + t$$

$$w' = w + \frac{\Delta w}{t} t$$

$$\frac{\Delta w}{t} = \frac{1.0}{\pi} \ln\left[\frac{e}{\sqrt{\left(\frac{1}{2.0(b-t)/t+1}\right)^2 + \left(\frac{.25\pi}{w/t+1.1}\right)^m}}\right]$$

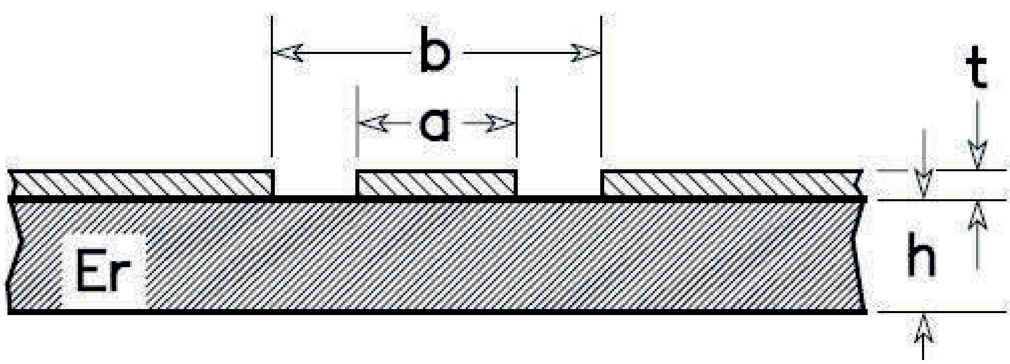
Off-Center Stripline



Microstrip verses Stripline

- Microstrip has lower loss-tangent problem.
- Microstrip has faster propagation time.
- Stripline has better immunity to crosstalk.
- Stripline has better EMI characteristics.

Coplanar Waveguide



- ‘b’ should be less than $\lambda/2$ for best performance.
- Ground must extend greater than 5x‘b’ on either side of trace ‘a’.
- Lower loss-tangent than Microstrip (signals couple mostly through air).
- Higher skin-effect losses (fields concentrate on edges of trace and grounds).

- May need to strap grounds together on either side of trace, every 1/20th wavelength.
- Only need one side of board to be accessible.
- No plated holes needed,
- Can narrow trace to match component leads.
- CPW allows variation of trace width, or spacing-to-ground or dielectric thickness to control Zo.
- Zo of CPW decreases as dielectric thickness increases.
- CPW produces smaller trace per given Zo than Microstrip.

$$Z_0 = \frac{30.0\pi}{\sqrt{\varepsilon_{eff,t}}} \bullet \frac{K(kt')}{K(kt)}$$

$$k1 = \frac{\sinh\left(\frac{\pi a_t}{4.0h}\right)}{\sinh\left(\frac{\pi b_t}{4.0h}\right)}$$

$$\varepsilon_{eff,t} = \varepsilon_{eff} - \frac{\varepsilon_{eff} - 1.0}{\frac{(b-a)/2.0}{0.7t} \bullet \frac{K(k)}{K'(k)} + 1.0}$$

$$k1' = \sqrt{1.0 - k1^2}$$

$$\varepsilon_{eff} = 1.0 + \frac{\varepsilon_r - 1.0}{2.0} \bullet \frac{K(k')K(k1)}{K(k)K(k1')}$$

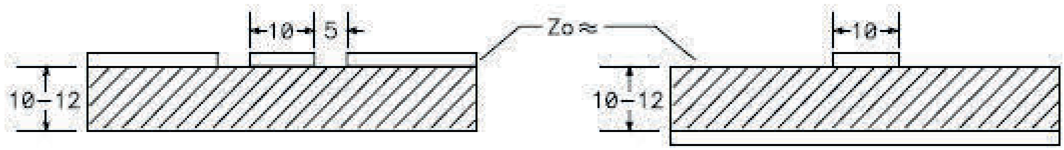
$$a_t = a + \frac{1.25t}{\pi}\left[1.0 + \ln\left(\frac{4.0\pi a}{t}\right)\right]$$

$$k_t = \frac{a_t}{b_t} \qquad k = \frac{a}{b}$$

$$b_t = b - \frac{1.25t}{\pi}\left[1.0 + \ln\left(\frac{4.0\pi a}{t}\right)\right]$$

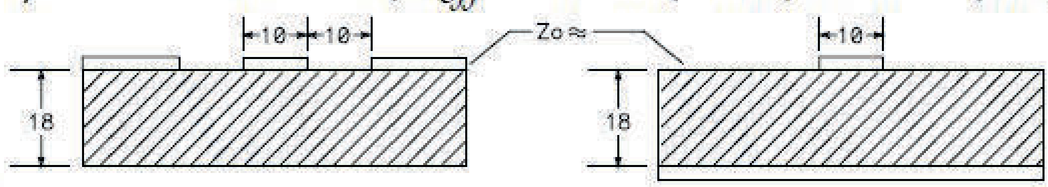
$$k_t' = \sqrt{1.0 - k_t^2} \qquad k' = \sqrt{1.0 - k^2}$$

CPW verses Microstrip



$\varepsilon_r = 4.2$ - Zo = 76 (ε_{eff} = 2.44 (CPW) & 3.02 (MS))

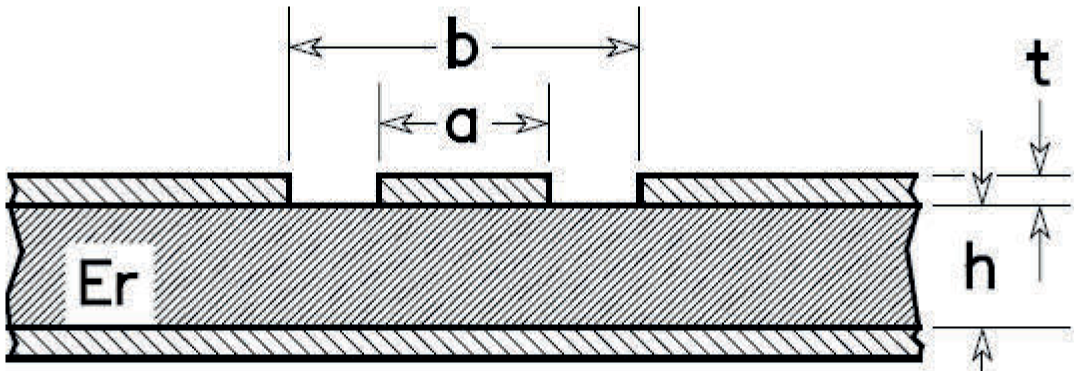
$\varepsilon_r = 2.5$ - Zo = 94 (ε_{eff} = 1.66 (CPW) & 1.96 (MS))



$\varepsilon_r = 4.2$ - Zo = 94 (ε_{eff} = 2.45 (CPW) & 2.95 (MS))

$\varepsilon_r = 2.5$ - Zo = 115 (ε_{eff} = 1.68 (CPW) & 1.92 (MS))

Coplanar Waveguide w/Ground



- In Reality, Microstrip transmission line in the RF / Microwave arena is CPWG.

$$Z_0 = \frac{120\pi}{2.0\sqrt{\varepsilon_{eff}}} \bullet \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k1)}{K(k1')}} \qquad k = a/b$$

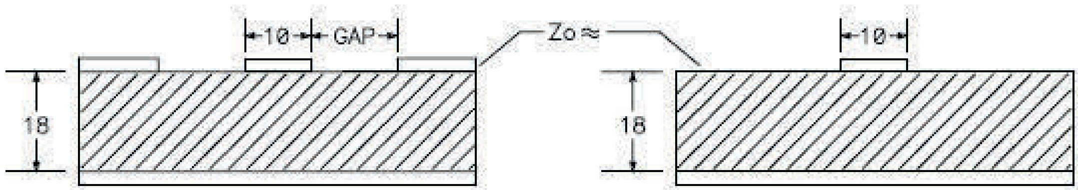
$$k' = \sqrt{1.0 - k^2}$$

$$k1' = \sqrt{1.0 - k1^2}$$

$$\varepsilon_{eff} = \frac{1.0 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k1)}{K(k1')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k1)}{K(k1')}} \qquad k1 = \frac{\tanh\left(\frac{\pi a}{4.0h}\right)}{\tanh\left(\frac{\pi b}{4.0h}\right)}$$

- To avoid Microstrip mode, h >b and left & right ground extend away from 'a' by more than 'b'.
- Zo of CPWG is increased as dielectric thickness increases. Opposite of CPW.
- If ' h' is large, CPW and CPWG behave in similar fashion.

CPWG verses Microstrip



ε_r = 4.2 - Zo = 94 Ohms (At Gap = 30)

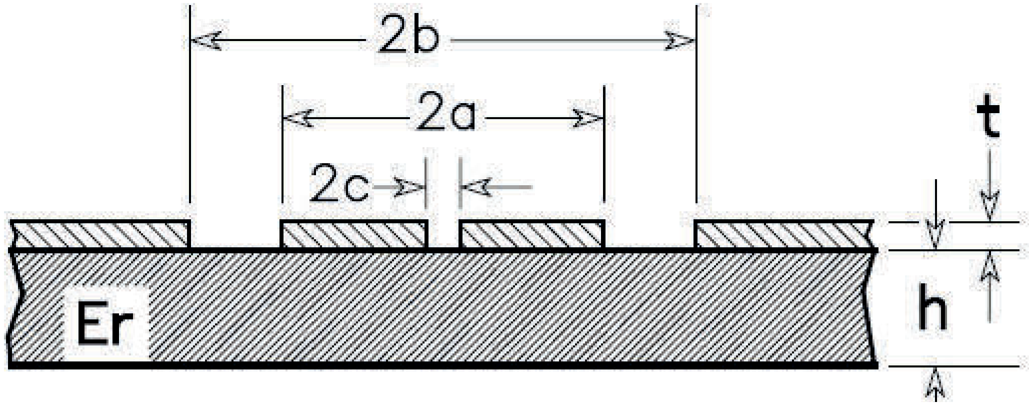
(ε_{eff} = 2.92 (CPWG) and 2.95 (MS))

ε_r = 2.5 - Zo = 115 Ohms (At Gap = 27)

(ε_{eff} = 1.89 (CPWG) & 1.92 (MS))

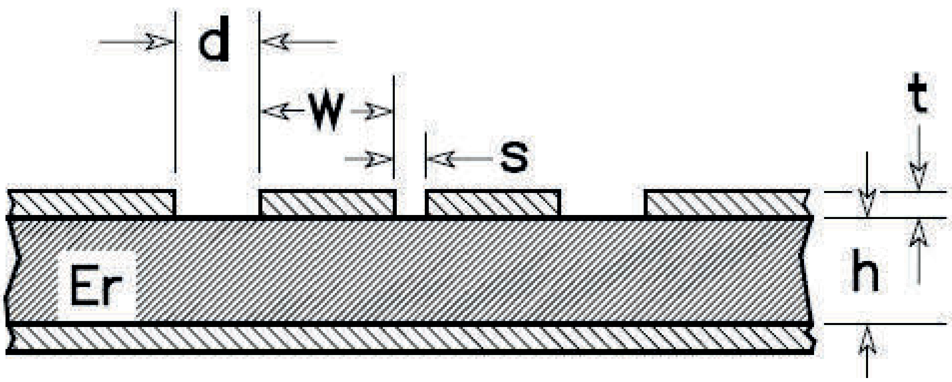
- Beyond gaps shown above, CPWG is like Microstrip.

Edge Coupled CPW (CP Differential Pair)



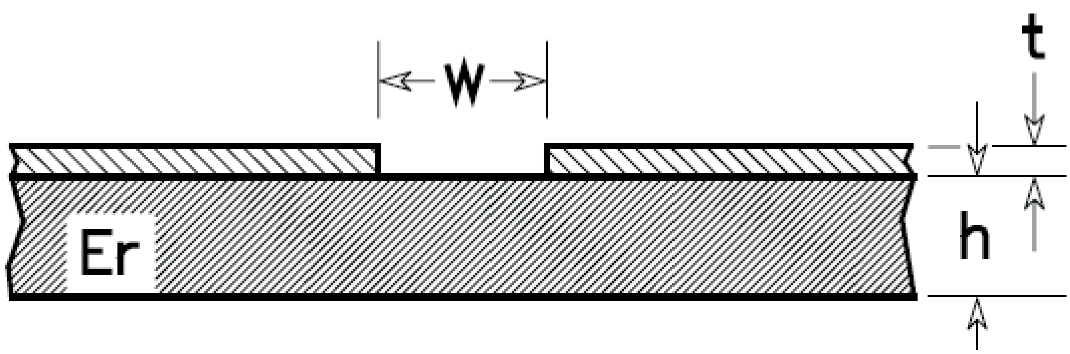
- Gives an extra degree of Signal-to-Noise isolation over standard CPW. (w/o plane, fields are large).

Edge Coupled CPWG (CP Diff Pair w/Grnd)



- Much better field containment than coupled CPW. Better yet in edge couple Stripline.

Slotline



- Acts like Waveguide with air dielectric.

Other Configurations

- 3 Line Coplanar Strip w & w/o Ground.
- Microstrip w/ limited width plane (and/or) limited width dielectric.
- Metal plate or shield covered CPW/CPWG.
- Metal plate or shield covered slotline.
- Offset CPW or CPWG.

Zo Calculations

- Use equations given or Wadell or Gupta.
- Use H.P. AppCAD (DOS and/or Windows).
- Use Rogers Corp. MWI (Dr R. Trout).
- Buy Field Solver (2D or 3D) Based Zo Calculator (i.e.- POLAR Ltd.)
- Don’t use Equations or Calcs for Dig Layout that Don’t Comp for Coplanar Effects.

Tpd, Capacitance and Inductance calculations (for all previous configurations)

$$Tpd = \sqrt{\varepsilon_{eff}} \,/\, c(\text{spd of light})$$
$$C = Tpd / Zo$$
$$L = Zo^2 \times C \ (\text{or } Tpd \times Zo)$$

Integral Components

- Components can be designed into the PC board utilizing the right configuration of lines and shapes to form-
  - Inductors
  - Capacitors
  - Couplers (similar to transformer)
  - Resistors (very small value)
  - Filters
- Capacitor formed by 2 copper plates separated by PCB dielectric (free component)

$$C = \varepsilon_r \times \varepsilon_0 \times (A/h)$$

Where: ε_r - DK of PCB Material

ε_0 - Permittivity of Space (2.25 x 10^{-13} ferrads/in.)

A - Area of Plate (L x W)

h - Dielectric Thickness

- Interdigital Capacitor