Dual-Path Architecture for Energy Harvesting Transmitters with Battery Discharge Constraints

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—We consider the design of transmission policies for sensor nodes that rely entirely on harvesting energy from the environment. Nodes store the harvested energy in a storage element which has constraints on maximum discharge rate and charging efficiency. Non-zero circuit power is considered and limitations on channel bandwidth and processor clock-rate are incorporated. We assume an additive white Gaussian noise (AWGN) channel and that time is divided into frames, with a fixed number of symbols transmitted in the frame duration. We consider an energy arrival process in which energy arrives at a constant rate within a frame but varies stochastically and independently across frames. In this context, we propose a dual-path architecture for energy flow that is shown to mitigate the performance loss due to the discharge rate constraint. For a given frame, we determine the rate-optimal time sharing ratio between harvesting energy and transmitting data. We also propose three sub-optimal policies, including statistical directional water-filling, for determining the time sharing ratio for a group of frames and compare their performance with an upper bound. We highlight that the discharge rate constraint is an important limitation of the storage element that can potentially hinder the effective use of energy.

I. Introduction

Natural energy harvesting (EH) promises near-perpetual operation of electronic devices due to its renewable nature. However, the non-deterministic and sporadic nature of energy availability pose a unique set of challenges in system design. Reliability necessitates the storing of energy in batteries or capacitors to dampen the energy fluctuations. However, storage elements (SE) have their own limitations, such as (a) capacity constraints, (b) energy leakage, (c) nonlinear charging behavior, (d) round-trip efficiency, and (e) discharge constraints [1]. Some of these limitations ((a)-(d)) have been factored into system design [2]–[13], while some (such as (e)) have not. In this paper, we want to include, amongst other factors, the impact of SE discharge constraints on the system design.

The discharge rate of a storage element is the rate at which one can draw power from the SE and it affects the discharge efficiency (γ), which is an important performance metric for storage elements [1], [14], [15]. Fig. 1 shows the experimental behavior of discharge efficiency as a function of discharge rate (for Tenergy lithium-ion 900 mAh cells); notice that γ decreases with increasing discharge rate. To study the effect of discharge rate constraints, we assume a simplified step- type behavior, with a discharge rate cutoff, after which the discharge efficiency drops from one to zero.

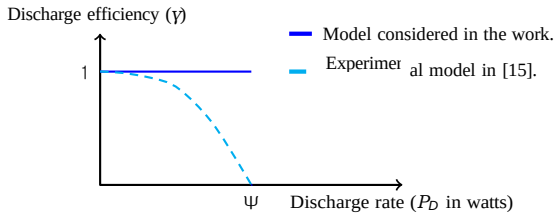

Fig. 1: The storage element (SE) discharge efficiency model used in the work. Discharge efficiency is defined as the ratio of the available energy at the load after losses to the initial energy stored in the SE. If the SE is discharged above a cut-off, i.e., discharge rate of Ψ, the discharge efficiency drops from one to zero.

In this paper, the system we study is a communication node with energy harvesting and storage element discharge constraints, as well as other constraints detailed later in the system model. Specifically, we focus on applications that require the node to communicate N symbols per frame over the channel. For instance, a sensor network deployed in an Internet of Things (IoT) application consists of sensor nodes with limited data processing and storage capabilities [16]. These may be designed to deliver a fixed number of symbols per frame, due to limited storage at the receiver. The information rate can be varied by varying the code rate. In such a scenario, it is sensible to ask how to optimally divide a frame into two parts – the first to harvest and store energy from the environment (*save phase*), and the next to harvest and use, both stored and harvested, energy for transmission (*transmit phase*).

Two state-of-the-art solutions to the EH communication problem described above are [10] and [11]. The work in [10] uses a single storage element without storing energy during the transmit phase, while [11] uses two storage elements which can instantaneously transfer energy between themselves. These solutions do not model SE discharge constraints but are impacted significantly when the discharge rate cutoff is on the order of the power needed to drive the circuit (cf. Section V-A). Our proposed solution is a dual-path architecture for energy flow, with a direct path and a path via the storage element, as shown in Fig. 2. The direct path feeds the harvested energy directly to the load, while the storage element provides the required dampening effect on energy fluctuations. The idea is that simultaneous power extraction from the direct path and the storage element provides higher power delivery. The overall effect is to eliminate the negative impact of SE discharge rate constraints. The dual-path architecture was shown to be practically feasible in [17].

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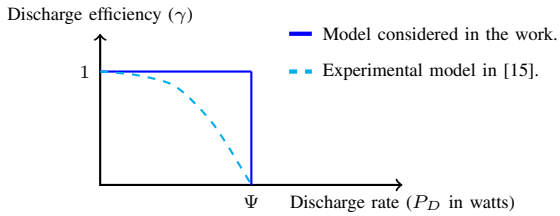

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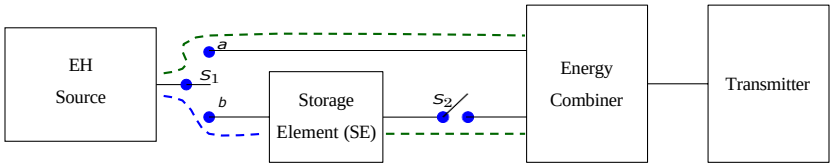


Fig. 2: The dual-path EH communication system. Harvested energy is used directly by the load when S_1 is set to a. The SE charges when S_1 is set to b and closing S_2 discharges the SE. We assume that whenever S_2 is closed, S_1 will be set to a. The blue and **green** dashed lines show the energy flow path from the EH source during the save phase and transmit phase respectively.

The problem of EH communications has been addressed from a variety of other perspectives as well. Initial studies involved finding the information theoretic capacity of storage-unconstrained [7] and constrained [2], [5], [6] systems under various assumptions on the energy arrival process. Directional water-filling (DWF) [3] and directional glue-pouring (DGP) [4] are throughput optimal with non-causal knowledge of energy arrivals in systems with zero and non-zero processing costs, respectively. Various algorithms have been proposed for throughput maximization [3] and storage element energy management [4], [12] when stochastic knowledge of energy arrival rate is available. In a queuing theoretic study in [13], the SE capacity is found to affect the communication delay. Recently, the focus has shifted towards exploring the effect of SE limitations on EH systems [18], e.g., SE leakage [8], SE non-linear charging [9] and efficiency [11].

The contributions of this paper are:

1) Introduction of an efficient dual-path architecture to reduce the impact of the discharge rate constraint of storage elements (Section II).
2) Analysis of the impact of SE discharge rate constraints, as well as circuit power, processor power, charging efficiency, bandwidth, and clock rate, on the optimal use of time resources to store energy and transmit data in a frame (Section III).
3) Derivation of three sub-optimal policies for maximizing the average rate, including two adaptive policies (instantaneous rate maximization and statistical directional water-filling) and a less complex non-adaptive policy (Section IV).
4) Performance comparison of (a) the dual-path architecture with two state-of-the-art architectures and (b) the sub-optimal policies with an upper bound (Section V).

II. System Model and Assumptions

A. System Operation

The block diagram of the system under study is shown in Fig. 2. The EH source block captures the incident natural energy and converts it to electrical energy. We assume that the output power available from the EH source is X units and is constant over a frame duration T, but varies stochastically across frames. The storage element in Fig. 2 is assumed to be a battery[1] with infinite capacity. The energy combiner combines the energy from the two paths [17] with a certain efficiency (we assume 100% efficiency in the paper). Let ρ be a real number in $[0, 1]$. In a given frame, the system depicted in Fig. 2 behaves as follows:

1) Save Phase: During the time duration $[0, \rho T)$, the SE is charged, i.e., the switch S_1 is connected to b and switch S_2 is kept open. The SE accumulates energy linearly with time. Assuming a charging efficiency of η, the accumulated energy over interval $[0, \rho T)$ is $\eta\rho XT$.
2) Transmit Phase: At time $t = \rho T$, the switch S_1 is connected to a, S_2 is closed, and transmission occurs in the time duration $[\rho T, T)$.

The parameter ρ is the *save ratio* and indicates the fraction of the frame duration for which energy is harvested and stored in the storage element.

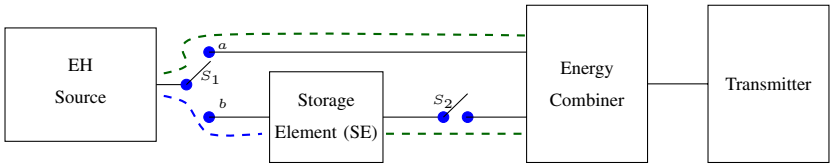
The architecture studied in [10] uses only one storage element and the save phase is exactly the same as in the dual-path architecture. But, in the transmit phase the harvested energy is neither used nor stored. We refer to the architecture in [10] as Single-Path Single-Battery (SP-SB) architecture. The architecture studied in [11] uses two storage elements – a primary and a secondary SE. During the save phase, the harvested energy is stored in the primary SE. In the transmit phase, the harvested energy is stored in the secondary SE and the energy is transferred instantaneously to the primary SE at the beginning of the following save phase. We refer to this architecture as Single-Path Dual-Battery (SP-DB) architecture.

B. Practical Constraints

1) Circuit Power: The total circuit power of any digital communication system consists of two components – data rate dependent power and data rate independent power. The power consumed in modulators, frequency synthesizers, power amplifiers and the power management unit etc. [19], is independent of the data rate. We denote this power by a constant a. On the other hand, the power consumed by the processor (including memory access) is a linear function of clock rate [19]. Any increase in ρ demands processor elements to work at a higher clock rate to meet the requirement of channeling N symbols in $(1-\rho)T$ time units. Let β be the total energy consumed in processing N symbols in T time units. The corresponding average power consumption is $\frac{\beta}{(1-\rho)T}$. Hence, the total circuit power is given by $P_C(\rho) = a + \frac{\beta}{(1-\rho)T}$.

2) Bandwidth and Clock Rate: The node is required to transmit N symbols in the duration $(1-\rho)T$, hence, the Nyquist bandwidth (W) is $N/(1-\rho)T$. The limited channel bandwidth puts an upper limit on ρ. Further, the maximum processor clock rate also puts an upper limit on ρ. Assuming

[1]The results in the paper also hold if a capacitor is charged and discharged in a battery-like manner, i.e., with constant power.



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