DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 3 CH-B	B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #x	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

				LBEXPBAK GPIO DEFINITION	
GPIO	POWER	I/O	Function	Implementation	Mother board Function
GPIO0	MAIN	I	BMBUSY#	10 K Pull-up to +3.3V	ADPT_ID_DET#
GPIO1	MAIN	I	TACH1	connect through a 0 Ω series resistor, and refer the PCA spec for Fans mapping. if not used by the system then 10K pull-up to +3.3V.	TACH1
GPIO2	MAIN	I	PCI_IRQB#	See PCA Spec	PCI Interrupt E#
GPIO3	MAIN	I	PCI_IRQF#	See PCA Spec	PCI Interrupt F#
GPIO4	MAIN	I	PCI_IRQG#	See PCA Spec	PCI Interrupt G#
GPIO5	MAIN	I	PCI_IRQH#	See PCA Spec	PCI Interrupt H#
GPIO6	MAIN	I	TACH2	**Pull-up to +3.3V and connect to P52 pin 12. The COMM Bassembly connects pin 12 directly to GND**	COMM_B_DET#/ M0M_TH_ALRT#
GPIO7	MAIN	I	TACH3	connect through a 0 Ω series resistor, and refer the PCA spec for Fans mapping. if not used by the system then 10K pull-up to +3.3V.	TACH3(PSU Fan Control)
GPIO8	RESUME	O	ICC_EN#		Reserved
GPIO9	RESUME	I	OC5	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO10	RESUME	I	OC6	**10K Pull-up to +3_3V and connect to P126-pin 16**	PRNTR_DET#
GPIO11	RESUME	I	SMBALERT#	20K Pull-up to +3_3VSB. It is always enabled as a wake event.	SMBALERT#
GPIO12	RESUME	I	LAN_DISABLE	Follow implementation in Intel Pickton Design Guide	LAN_DISABLE#
GPIO13	RESUME	I	IO_PME	10K Pull-up to +3_3V and connect to P151-pin 10; also add a no-installed pulldown to the net.	RDYBST_DET# or DASH SMI
GPIO14	RESUME	I	OC7	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation. 8.2K Pull-up to +3.3V and connect to the SMI pin on the SIO	SMI# from SIO
GPIO15	RESUME	I	PCE_GP15		Reserved
GPIO16	RESUME	O	SATA4GP	10 M pull- up to VBAT and connect to CPU SKTOCC# , SIO pin48 and PCH	CPU_MISSING
GPIO17	MAIN	I	TACH0	connect through a 0 Ω series resistor, and refer the PCA spec for Fans mapping. if not used by the system then 10K pull-up to +3.3V.	TACH0(Front Chassis Fan)
GPIO18	MAIN	I	PCICLKRQ1#	Through a 1KΩ series resistor, 8.2K pull-up to +3.3V and connect to E15-pin 1. E15 Pin 2 connect to GND	BOOT_BLK_REC#
GPIO19	MAIN	I	SATA1GP	connect to a test point	unused
GPIO20	MAIN	I	PCICLKRQ2#	Through a 0 Ω series resistor, 10Kpull-up to +3.3V and connect to HANKSVILLE -pin48	PCIECLKRQ2#
GPIO21	MAIN	I	SATA0GP	10K pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#
GPIO22	MAIN	I	SCLOCK	10K Pull-up to +3_3V and connect to P150-pin 10	INT_USB_DET#
GPIO23	MAIN	I	LDRQ1#	connect to a test point.	PEG_M0M_DET#
GPIO24	RESUME	O	MEMLED	Through a 1k Ω series resistor, 8.2K pull-up to +3_3V and connect to P125-Pin 1. 1M pull-up to VBAT and connect to P125-pin 3	HOOD_SW_DET#
GPIO25	RESUME	I	PCICLKRQ3#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ3#
GPIO26	RESUME	I	PCICLKRQ4#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ4#
GPIO27	RESUME	O	OD_PLL_VR_EN	10k pull-up to +3.3VAUX	Reserved
GPIO28	RESUME	O	PCE_GP28	connect to a test point	unused
GPIO29	RESUME	O	SLP_LAN#	refer to the PCA spec.	SLP_LAN#
GPIO30	RESUME	I	SUS_PWR_ACK	100K Pull-up to 3.3V_AUX	unused
GPIO31	MAIN	I	ACPRESENT	10K Pull-up to +3_3V and connect to P25-pin 10	FRONT_USB_DET 1#
GPIO32	MAIN	O	PCE_GP32	Through a 1k Ω series resistor, 10K pull-up to +3_3V and connect to P2-pin 6.	NON-EPA_PS_DET#
GPIO33	MAIN	O	PCE_GP33	Through a 1k Ω series resistor, 8.2K pull-up to +3_3V and connect to pin 1 of jumper E1 and E1 pin2 to GND	FDT_OVRD#
GPIO34	MAIN	O	SP_PCI#	3.3K Pull-down to GND and connect to P124-pin 2. Decouple P124-pin 2 with 0.1μF P124 pin 1 2.2K pull-pu to 5V and P124 pin 6 2.2k pull-up to 5V	HOOD_LOCK_DET
GPIO35	MAIN	O	SATACLKREQ#	10K Pull-up to +3_3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0
GPIO36	MAIN	I	SATA2GP	10K Pull-up to +3_3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1
GPIO37	MAIN	I	SATA3GP	10K Pull-up to +3_3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2
GPIO38	MAIN	I	SLOAD	Through a series 1K resistor, 10K Pull-up to +3_3V and 10K pull-down to GND and connect to P5-pin 9. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID0
GPIO39	MAIN	I	SDATAOUT0	Pull-up to +3_3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BRD_ID1
GPIO40	RESUME	I	OC1	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for XDP implementation. 8.2k Ω pull-down to GND and connect to E49-pin 2 E49 pin-1 300 pull-up to +3.3V	PASSWORD_EN
GPIO41	RESUME	I	OC2	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO42	RESUME	I	OC3	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO43	RESUME	I	OC4	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO44	RESUME	I	PCICLKRQ5#	10K pull-up to +3.3VAUX and connect to a test point.	PCIECLKRQ5#
GPIO45	RESUME	I	PCICLKRQ6#	Through a 0 Ω series resistor. 10K pull-up to +3.3V and connect to J31-pinB17	PRSNT#_J31
GPIO46	RESUME	I	PCICLKRQ7#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ7#
GPIO47	RESUME	I	PEG_A_CLKRQ#	Through a 0 Ω series resistor. 10K pull-up to +3.3V and connect to J41-pinB48 and B81	PRSNT#_J41
GPIO48	MAIN	I	SDATAOUT1	Through a series 1K resistor, 10K Pull-up to +3_3V and 10K pull-down to GND and connect to P5-pin 10. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID1
GPIO49	MAIN	O	SATA5GP	10K Pull-up to +3_3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0
GPIO50	MAIN	I	PCI_REQ#1	8.2k pull-up to VCC3	REQ1#
GPIO51	MAIN	O	PCI_GNT#1	connect to a test point	GNT1#
GPIO52	MAIN	I	PCI_REQ#2	8.2k pull-up to VCC3	REQ2#
GPIO53	MAIN	O	PCI_GNT#2	connect to a test point	GNT2#
GPIO54	MAIN	I	PCI_REQ#3	Through a 8.2KΩ series resistor, connect to E14-pin 2 and 1K pull-down to GND. E14 -pin1 connect to +3.3V	BOOT_BLK_EN#
GPIO55	MAIN	O	PCI_GNT#3	connect to a test point	GNT3#
GPIO56	RESUME	I	PEG_B_CLKRQ#	refer to the PCA spec.	AUD_AMP_DIS#
GPIO57	MAIN	I	PCE_GP57	10K Pull-up to +3_3VME installed and 10K pull-down to GND not installed.	TPM_PP
GPIO58	RESUME	O	SMLICLK	10K pull-up to 3V_AUX	SML1CLK
GPIO59	RESUME	I	OC0	connect through a 0Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO60	RESUME	O	SMLDALERT#	10K pull-up to 3V_AUX	SML0ALARM
GPIO61	RESUME	O	SUS_STAT#	connect to a test pin	LPCPD#
GPIO62	RESUME	O	SUSCLK	SUSCLK to SIO-pin16	SUSCLK
GPIO63	RESUME	O	SLP_S5#	Connect to the SIO-pin37	SLP_S5#
GPIO64	MAIN	O	CLKOUTFLEX0	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLEX0
GPIO65	MAIN	O	CLKOUTFLEX1	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLEX1
GPIO66	MAIN	O	CLKOUTFLEX2	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLEX2
GPIO67	MAIN	O	CLKOUTFLEX3	refer to the PCA spec. unused clock connect to a test point	CLK14M
GPIO72	RESUME	I	PCE_GP72	Pull-up to +3_3V and connect to P24-pin 10	FRONT_USB_DET 0#
GPIO73	RESUME	I	PCIECLKRQ0#	10K pull-up to +3.3VAUx and through a 0 Ω series resistor. connect to J42-pinB17. B31, B48, and B81	PRSNT#_J42
GPIO74	RESUME	O	SML1ALERT#	10K pull-up to 3V_AUX	SML1ALERT#
GPIO75	RESUME	O	SML1DATA	10K pull-up to 3V_AUX	SML1DATA

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Size	Document Description	Rev
Custom	PCH GPIO Table	1.0

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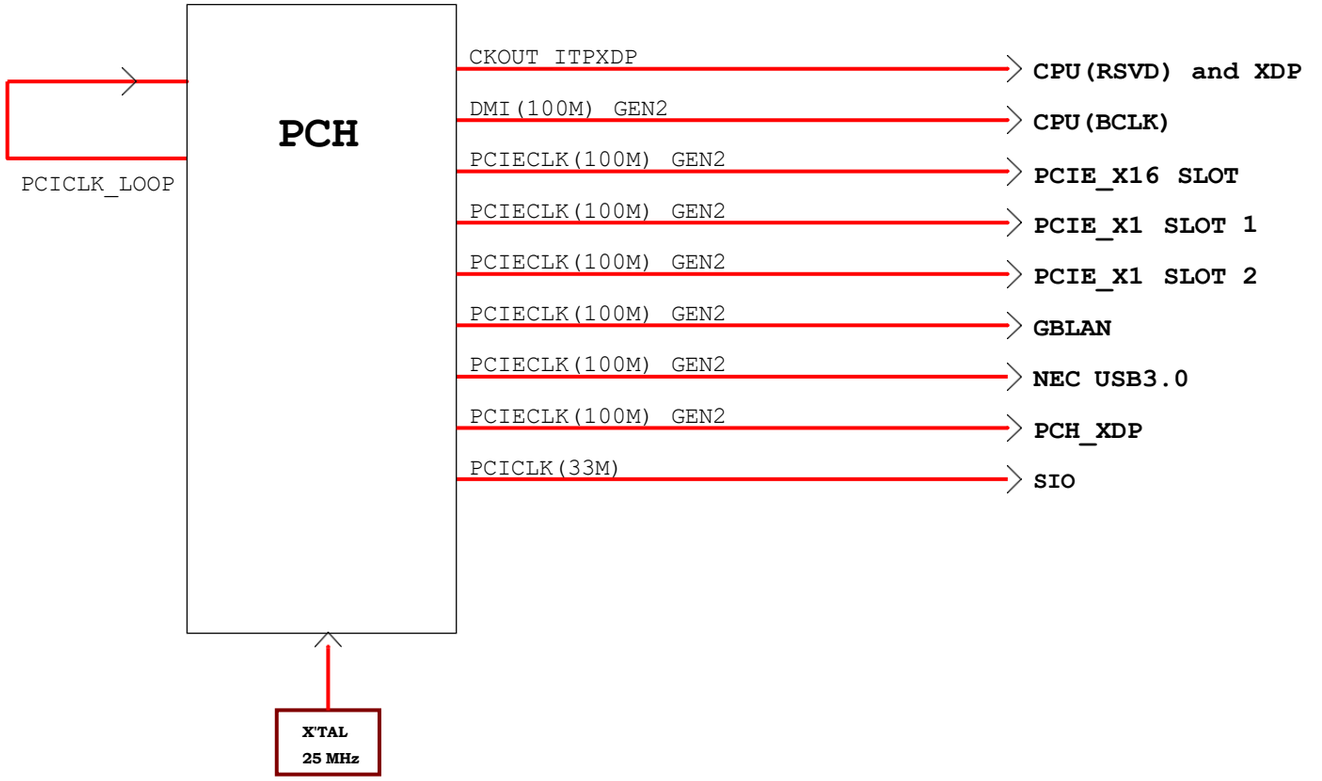

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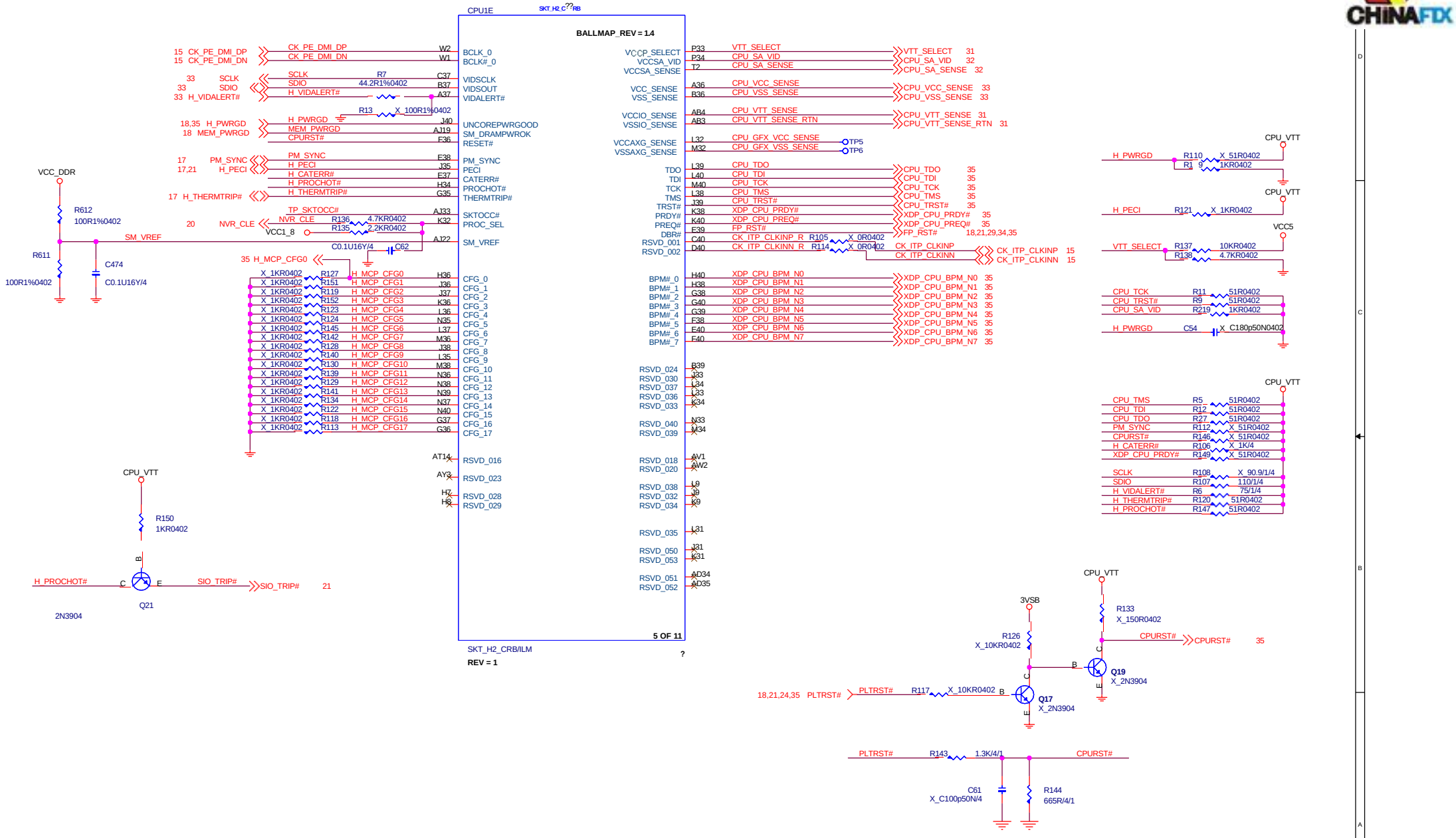

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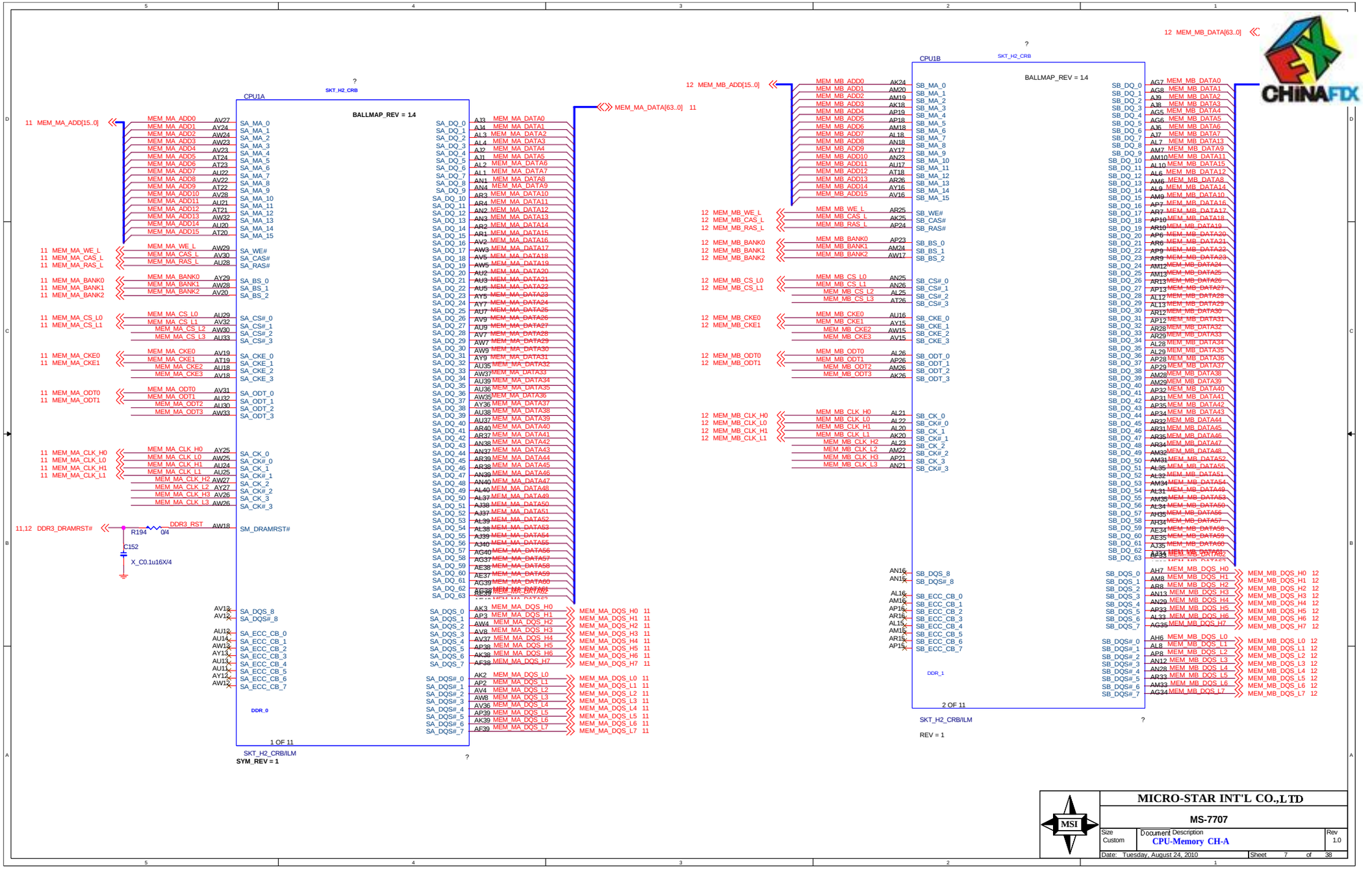

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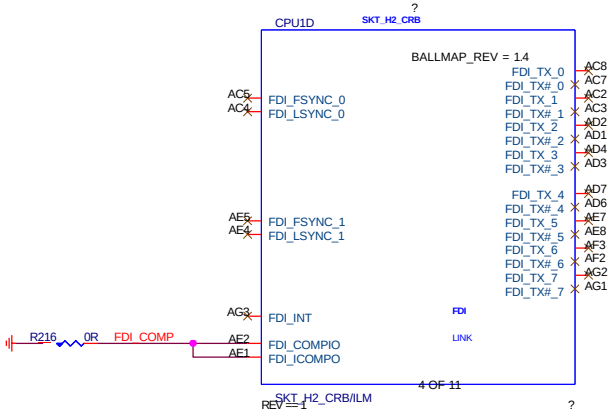
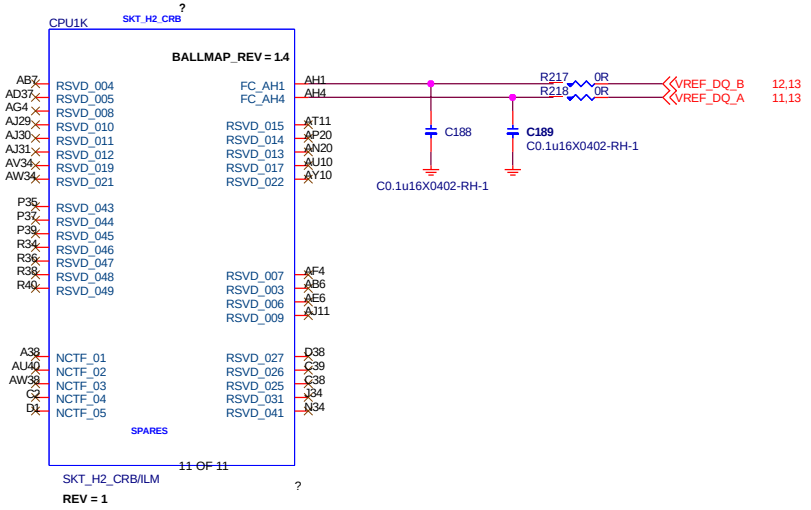
Disable Guidelines

All the FDI signals FDI_TX, FDI_FSYNC, FDI_LSYNC and FDI_INT signals on the CPU and the PCH can be left as No connect for solutions not using integrated graphics. solution.

FDI Signal	Recommendation
FDI_TX[7:0]	Float or No connect
FDI_TX#[7:0]	Float or No connect
FDI_FSYNC [1:0]	Float or No connect
FDI_LSYNC [1:0]	Float or No connect
FDI_INT	Float or No connect
FDI_COMPIO	Connect to Vss
FDI_ICOMPO	Connect to Vss





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Model	MS-7707
Size	Custom
Document Description	CPU-PEG/DMI
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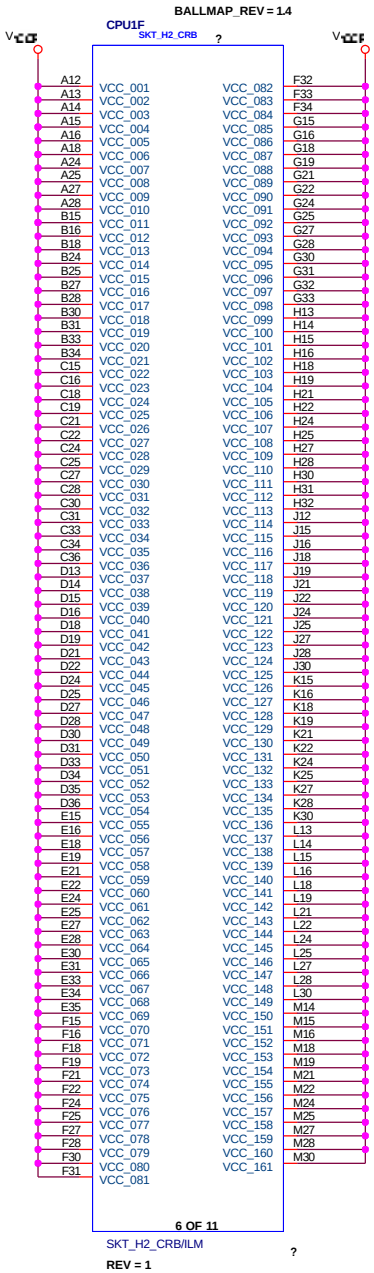
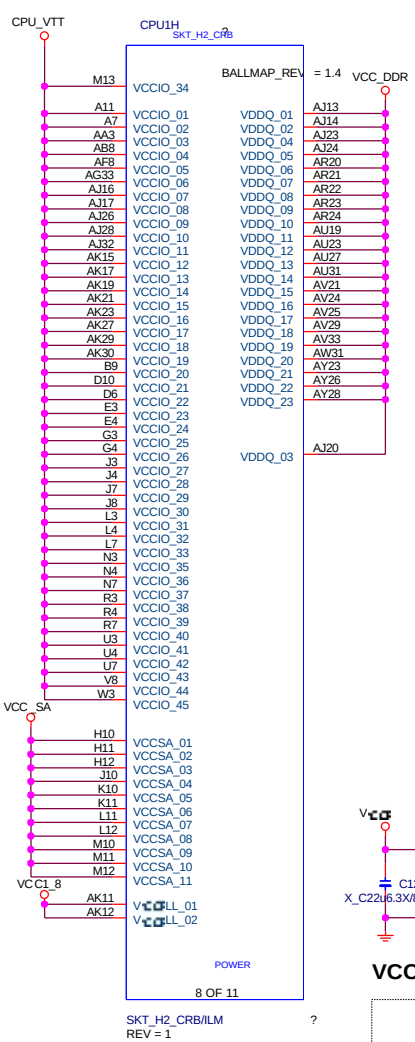
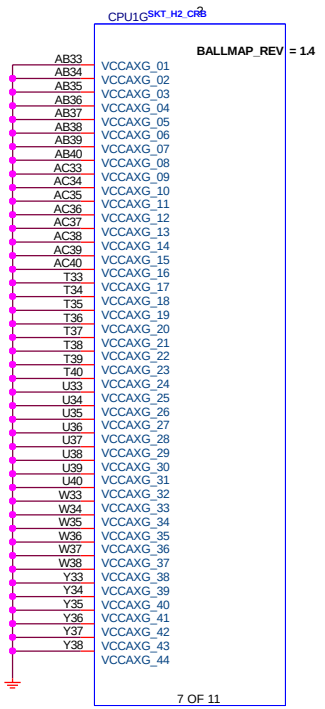
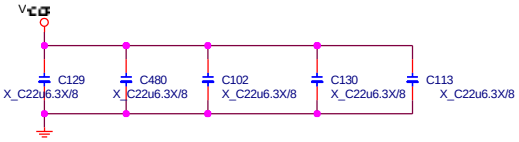
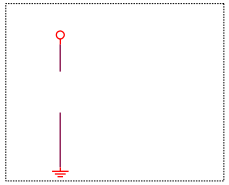




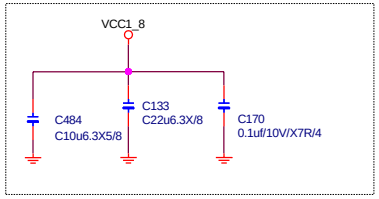




VCC_SA-Decoupling



VCC1_8-Decoupling



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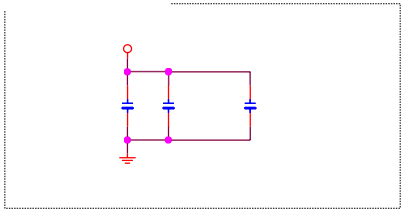
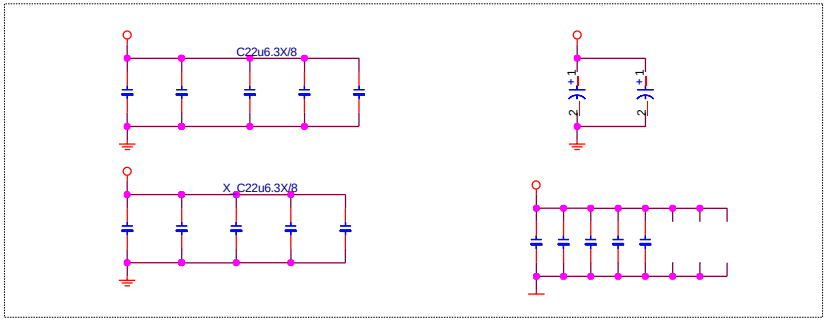
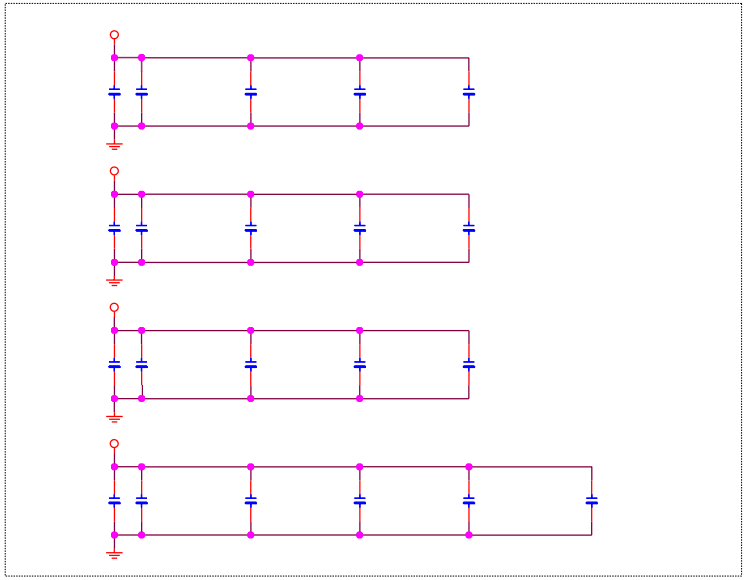


+CPU_VTT Decoupling



+CPU_VCCF-Decoupling



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