

1. Schematic Page Description :

Schematic Ver : A01

01. Title

02. Schematic Page Description

03. Block Diagram

04. ANNOTATIONS

05. Schematic Modify

06. Timing Diagram

07. AMD K8-S1 Host (1/3)

08. AMD K8-S1 DDR (2/3)

09. AMD K8-S1 MISC (3/3),Fan

10. Clock Generator

11. VIA K8N890 Host (1/3)

12. VIA K8N890 PCI-E (2/3)

13. VIA K8N890 V-Link (3/3)

14. DDRII-DIMM 0-1

15. VT1634 LVDS Transmitter

16. LCD&CRT CONN.

17. VIA VT8237A PCI/USB (1/3)

18. VIA VT8237A IDE/AC-Link (2/3)

19. VIA VT8237A V-Link/MII/LPC (3/3)

20. PCIE&IDE&MDC
21. VT6103L LAN PHY

22. KBC-ITE-8512

23. Adaptor in/Charge

24. 5VLA,5VA,3VLA,3VA

25. CPU Core Power[MAX8760]

26. CPU+1.2VHT\1.5V\2.5V

27. 1.5VS_NB/1.8V_CPU

28. Power 3VS/3V,5VS/5V,

29. Audio Codec

30. USB BOARD

For E23 Add and Del Function Component List.

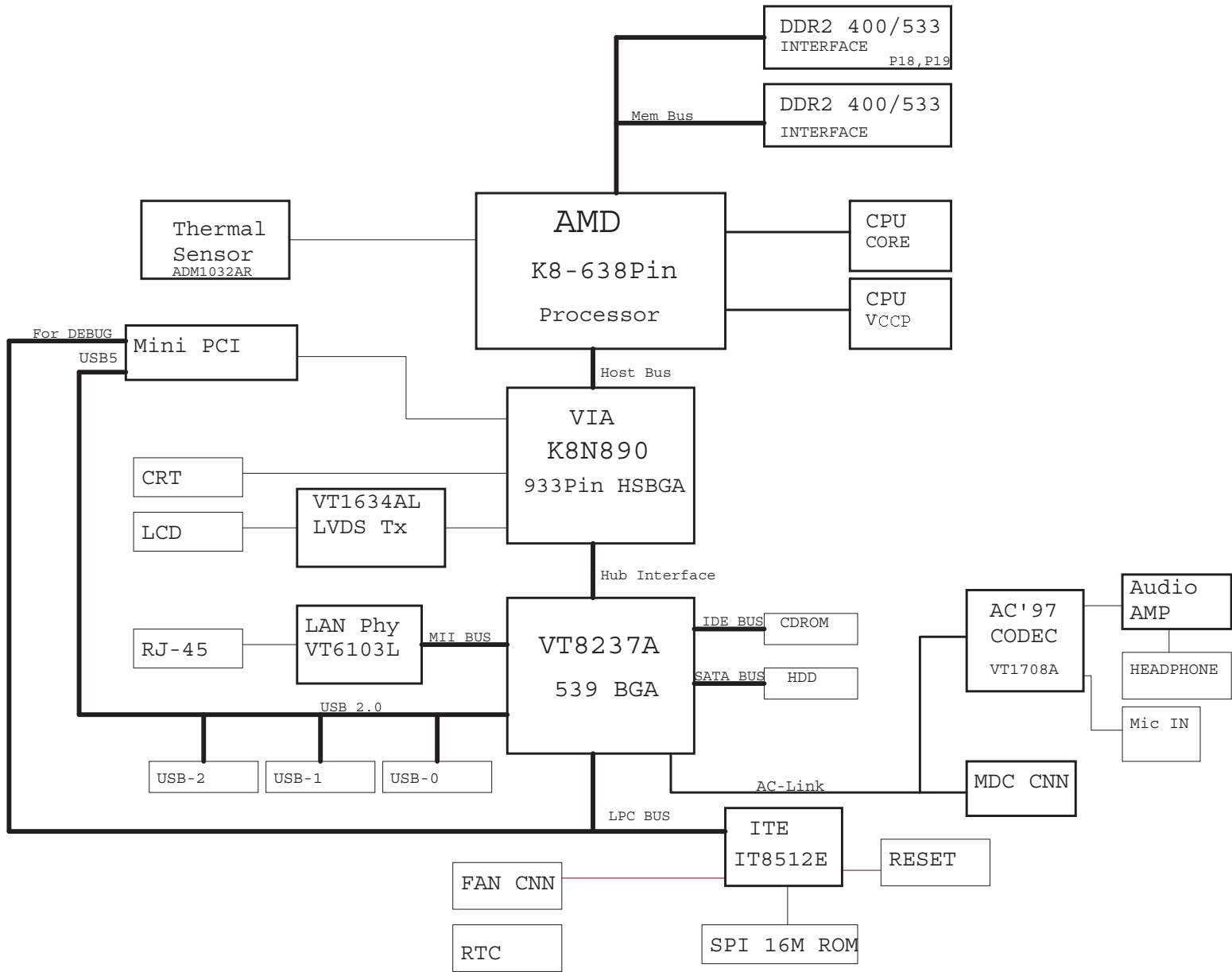
Remove MDC function (Page 20)
CN13 L38 R292 C384

Add one USB port (Page 30)
U1002 L1002 C1003 C1004 CN1003

Add audio Function (Page 29)
Del C344 R266
Add R263 C345

For K/B Function
Del R44 R52
Add R45 R50

3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
5VLA	5.0V always on power rail by LATCH or ACIN
5VA	5.0V always on power rail by ECPWON
3VA	3.3V always on power rail by ECPWON
5V	5.0V power rail by SLP_S5#_3R
3V	3.3V power rail by SLP_S5#_3R
5VS	5.0V switched power rail by SLP_S3#_3R
3VS	3.3V switched power rail by SLP_S3#_3R
Vcore_CPU	Core Voltage for CPU
VCCP	1.05V for AGTL+ Termination Voltage
+V1.8_CPU	1.8V for CPU PLL Voltage
+V0.9_DDR	0.9V DDR Termination Voltage
+V1.5S	1.5V switched power rail
+V1.5	1.5V power rail
+V1.5A	1.5V always on power rail
+V2.5S	2.5V power rail for SATA

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RS	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal
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Signal Conditioning

D	=	Damped (by a resistor)
Q	=	Isolated (by a Q-switch)
L	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers	PCB Thickness :1.2mm+/-0.1 mm .
Layer 1	Component Side, Microstrip signal Layer
Layer 2	Power Plane
Layer 3	Stripline Layer (AGTL, CLOCK, DDR)
Layer 4	Stripline Layer (Analog, LVDS, other)
Layer 5	Ground Plane
Layer 6	Solder Side, Microstrip signal Layer

Table 1-3. Six-Bit Voltage Identification (VID) Codes

VID[5:0]	Voltage (V)	VID[5:0]	Voltage (V)	VID[5:0]	Voltage (V)	VID[5:0]	Voltage (V)
000000	1.5500	010000	1.1500	100000	0.7625	110000	0.5625
000001	1.5250	010001	1.1250	100001	0.7500	110001	0.5500
000010	1.5000	010010	1.1000	100010	0.7375	110010	0.5375
000011	1.4750	010011	1.075	100011	0.7250	110011	0.5250
000100	1.4500	010100	1.050	100100	0.7125	110100	0.5125
000101	1.4250	010101	1.025	100101	0.7000	110101	0.5000
000110	1.4000	010110	1.000	100110	0.6875	110110	0.4875
000111	1.3750	010111	0.975	100111	0.6750	110111	0.4750
001000	1.3500	011000	0.950	101000	0.6625	111000	0.4625
001001	1.3250	011001	0.925	101001	0.6500	111001	0.4500
001010	1.3000	011010	0.900	101010	0.6375	111010	0.4375
001011	1.2750	011011	0.875	101011	0.6250	111011	0.4250
001100	1.2500	011100	0.850	101100	0.6125	111100	0.4125
001101	1.2250	011101	0.825	101101	0.6000	111101	0.4000
001110	1.2000	011110	0.800	101110	0.5875	111110	0.3875
001111	1.1750	011111	0.775	101111	0.5750	111111	0.3750

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6.Schematic modify Item and History :

Version 0.1 change to 0.2 change list.

- 1.D6 from BAT54C-7 change to PNP DTA144EUA 50V 30mA SC70
- 2.C493 Change BOM to NU
- 3.BOM Change EEPROM FROM SST25VF080B TO W25X80VSSIG
- 4.CN5 K/B Connect FROM 25PIN CHANGE TO 24PIN
- 5.C312 BOM Change TO 1000pF
- 6.HDD FROM PATA CHANGE TO SATA
- 7.R471 BOM Cange To NU
- 8.R268 R269 R 270 R271 R272 From 220Ohm CHANGE To 1000Ohm BOM Change
- 9.Schematic Change R268 R269 Connect To 3VLA
- 10.Q28 DEL By BOM Change
- 11.C481 From 1uF Change To 10uF BOM Change
- 12.R135 From Pulldown Change To pullhigh
- 13.Add LED for Wireless-LAN
- 14.2.5VS UP to 2.6VS
- 15.1.5VS UP to 1.6VS
- 16.Jmp wire from C513 to Q45 567Pin.
- 17.X1 and X3 Pin 1,4 and 2,3 change.
- 18.Jmp wire from C513 to Q45 567Pin.
- 19.R542 and R543 BOM Change to 2.2K
- 20.R540 and R541 BOM Change to 00hm
- 21.A20GET U31,W3 Pin connect to U18,126 Pin
- 22.KBRC U31,V1 Pin connect to U18,16Pin
- 23.R183, R221 BOM Change to 47K
- 24.C266, C311 Change to 4.7uF 25V 1206
- 25.R149 Change to 51K BOM Change.
- 26.R547 Change to 2.1K BOM Change.
- 27.C479 DEL
- 28.C436 BOM change NU
- 29.C425,C429,C433 BOM change to 22p For VESA
- 30.R264 R266 BOM change to 15K.
- 31.R547 BOM change to 2.1K.
- 32.L47,L48,L49 BOM change to 17 ohm + - 25% 100MHZ 0.1 ohm 600mA (0805).
- 33.SPEC.change PATA to SATA
- 34.Battery schematic change.

Version 0.2 change to 0.3 change list.

- 35.Function change EC-ON-power issue.3VLA plan Delete.
- 36.Function change CPU THERMTRIP# ON/OFF POWER for 5VLA.
- 37.SATA-Pull -Power 2.5V modify.
- 38.POWER ON sequence For Battery only time Change.
- 39.SATA-Connect change to DIP.
- 40.PCB From 1.4mm change to 1.2mm
- 41.Add HDD Led Pull High.
- 42.Power Del mOhm resistance.(All Power Plan)
- 43.BOM change. Del C91 & C92 For some Memory issue.
- 44.W-lan change to green LED.
- 45.Modify SATA-IDE clock 25Mhz.

Version 0.3 change to AX1 change list.(SI buid)

- 46.ADD EMI Solution on SPEAKER Side 150pF.
- 47.ADD USB Solution on SB8237A PLLPower.
- 48.Modify EC Power ON solution. Add R624
- 49.Modify SATA LED add pull HIGH.
- 50.Modify USB test R531 from 6.4K change to 5.11K.

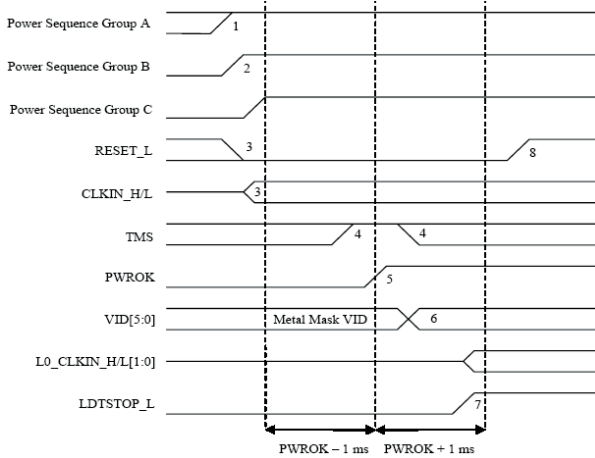
(SI buid) Change List

- 51.Modify BOM for Mini-PCIE connect too High over botton cover.

Version AX1 change to A01 change list.(PV buid)

- 52.Add Function For Modem RING#.(L38 Power plan change to 3VA)
- 53.Modify BOM for DC-IN connect .(ME)
- 54.Modify BOM for C596,C597,C598,C599 from 5pF to 0.1uF (EMI)
- 55.Add BOM for L68 (EMI)
- 56.change BOM for AUDIO function R264 and 266 From 10k change to 20K
- 57.change BOM for EMI function Add R672 22ohm.
- 58.change BOM for EMI function Add C623-631 0.1uF
- 59.change BOM for USB function Issue R531 from 5.1K change to 6.04K
- 60.change USB power plan function Support S3 wake up.
- 61.change WLAN LED function Only Support ON-OFF.
- 62.change BOM for LCD on-off.

VDDIO=DRAM POWER 1.8V
VTT=DRAM Vref POWER 0.9V
VDDA=CPU POWER 2.5V
VDD=CPU core POWER by VID
(first 0.9V)
VLDT=CPU POWER 1.2V



A01 change A02 BOM change list.(PV buid to MP BOM cheng List)

- 63. 將Vcore Voltage 調高每增加1A Vcore voltage 下降 0.75mV原本是每增加1A Vcore voltage 下降 1.5mV.
Modify R611,R612,R613,R614-----60130B1020ZT(1K---0402)
change to 6013A0018401---2k 1% ---0402

- 64. USB eye-pattern 調大 From R531 6.04K 1% 0603 (6013A0068501) change to 5.62K 1% 0603 (60130B56219T)
- 65. Change BOM L66,L62,L23 to R630,R631,R632 from (60140EA0063T) to 0 OHM 5% (60130B00000Z) and (60130BA0003T)
- 66. SATA eye-pattern 調大 From R559 6.19K 1% 0603 (6013A0068501) change to 5.62K 1% 0603 (60130B56219T)
- 67. RTC C515,C511 change to (6010078R220Y) CAPACITOR-CHIP,8.2PF,50V,D,NP0,0603,TR
- 68. R446 NU
- 69. EMI issue Change C323,C535,C320,C327,C321 From 12pF change to 22pF 50V 5% 0603 NPO (60100722020Z)
- 70. For North bridge Thermal issue ADD R486 4.7K 5% 1/16W 0402(60130B4720ZT)
- 71. North bridge Vref. V-LINK Change R592 From 1K 5%(60130B1020ZT) to 1K 1%(60130B10019Z)
- 72. Change South bridge Voltage to 2.5V R547 from 2.1K 1% 1/10W 0603 change to 2.2K 1%(60130B22019T)

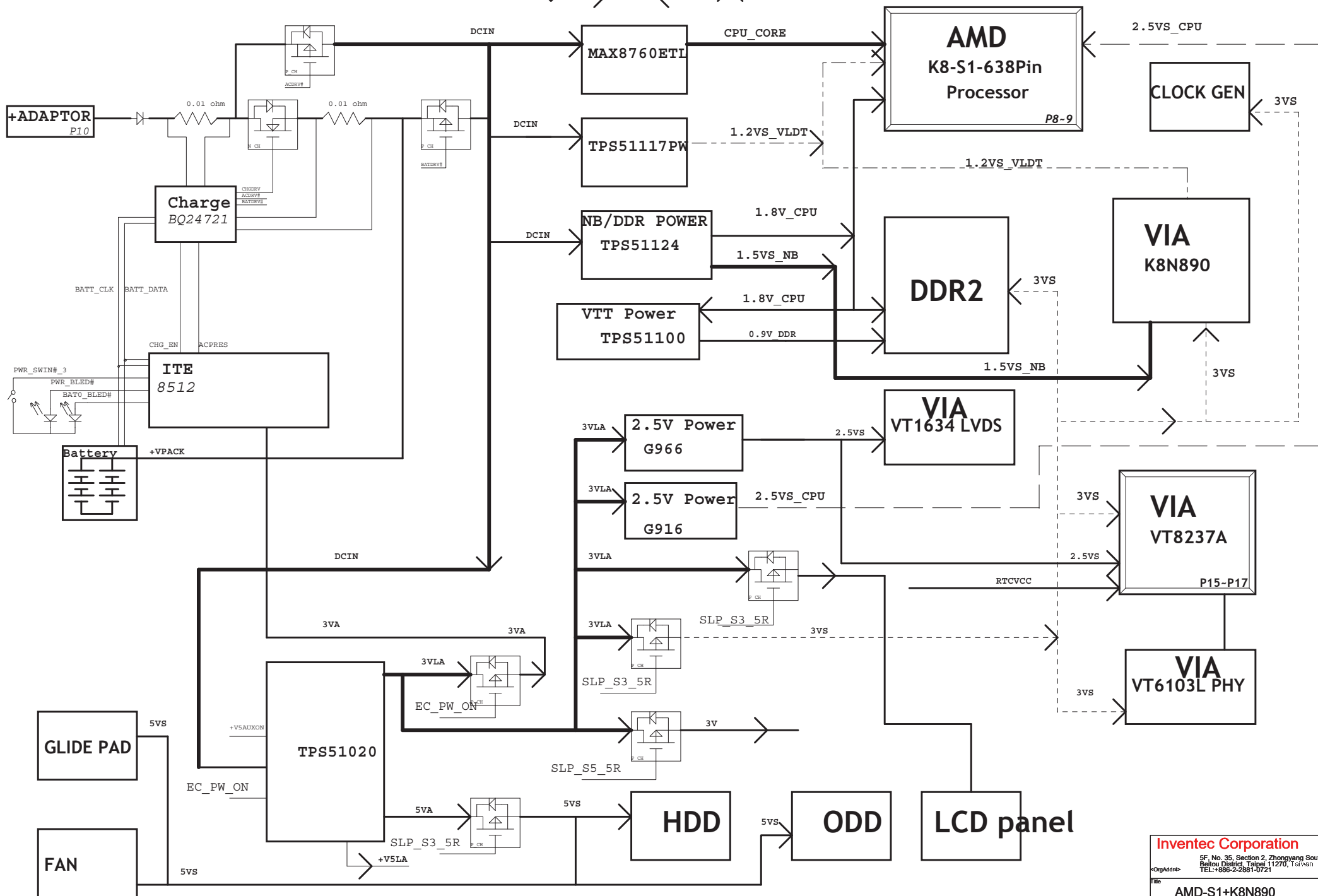
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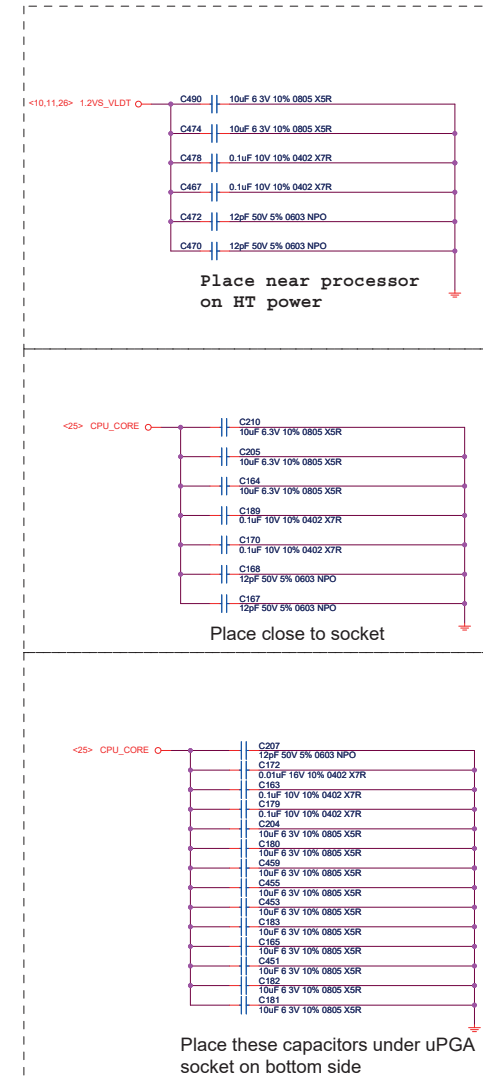
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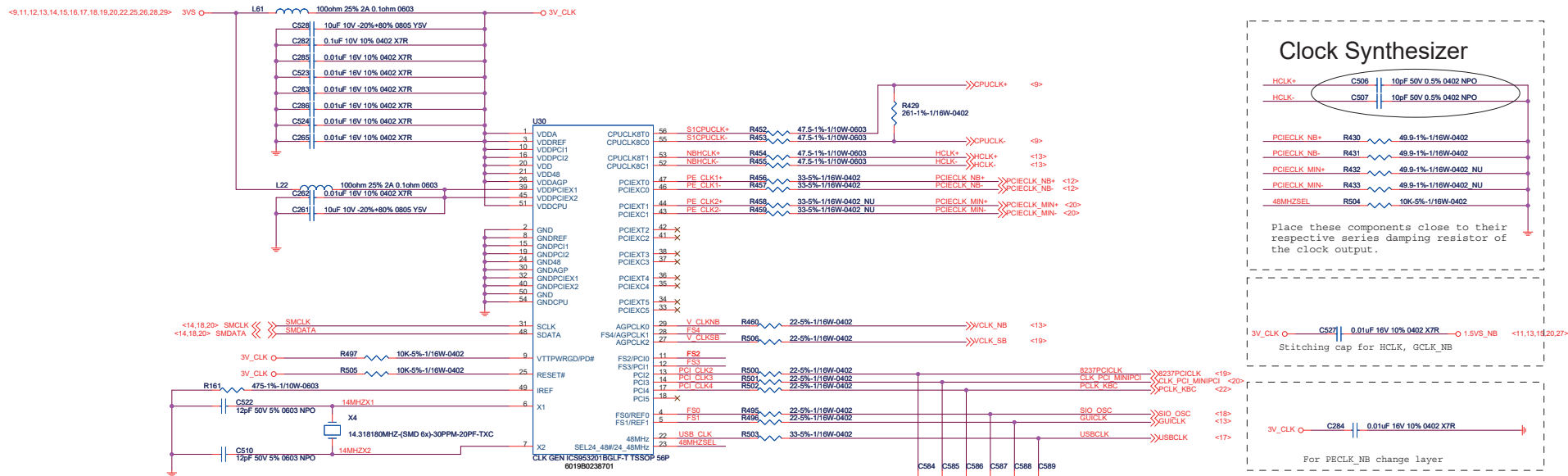
Rev

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LAYOUT: Place HT bypass caps on topside near unconnected Clawhammer HT Link

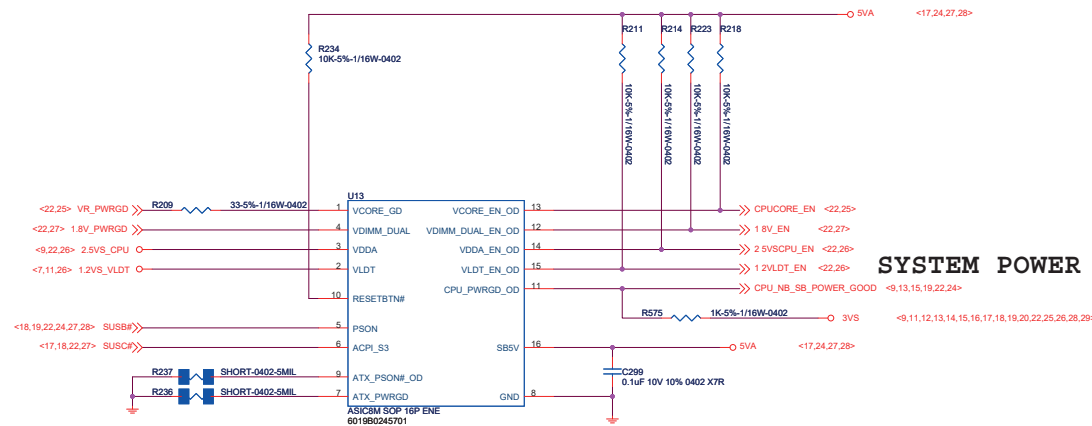




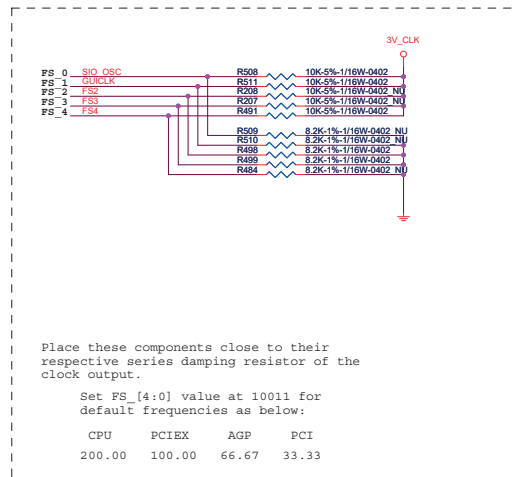


FS_[4:0]	CPU	PCIEX	AGP	PCI	FS_[4:0]	CPU	PCIEX	AGP	PCI
00000	100.90	100.90	67.27	33.63	10000	100.00	100.00	66.67	33.33
00001	133.90	100.43	66.95	33.48	10001	133.00	100.00	66.67	33.33
00010	168.00	100.80	67.20	33.60	10010	166.66	104.16	69.44	34.72
00011	202.00	101.00	67.33	33.67	10011	200.00	100.00	66.67	33.33
00100	100.20	100.20	66.80	33.40	10100	103.00	103.00	68.67	34.33
00101	133.50	100.13	66.75	33.38	10101	137.33	103.00	68.66	34.33
00110	166.70	100.02	66.68	33.34	10110	171.66	103.00	68.66	34.33
00111	200.40	100.20	66.80	33.40	10111	206.00	103.00	68.67	34.33
01000	160.00	100.00	66.67	33.33	11000	208.00	104.00	69.33	34.67
01001	202.00	101.00	67.33	33.67	11001	210.00	105.00	70.00	35.00
01010	210.00	105.00	70.00	35.00	11010	215.00	107.50	71.67	35.83
01011	212.00	106.00	70.67	35.33	11011	220.00	110.00	73.33	36.67
01100	270.00	101.25	67.50	33.75	11100	226.00	113.00	75.33	37.67
01101	225.00	112.50	75.00	37.50	11101	230.00	115.00	76.67	38.33
01110	266.67	100.00	66.67	33.33	11110	240.00	120.00	80.00	40.00
01111	300.00	112.50	75.00	37.50	11111	250.00	125.00	83.33	41.67

CPU POWER ON CONTROL



SYSTEM POWER GOOD

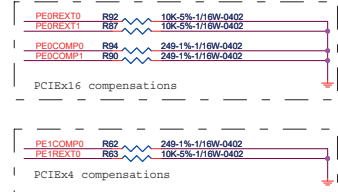


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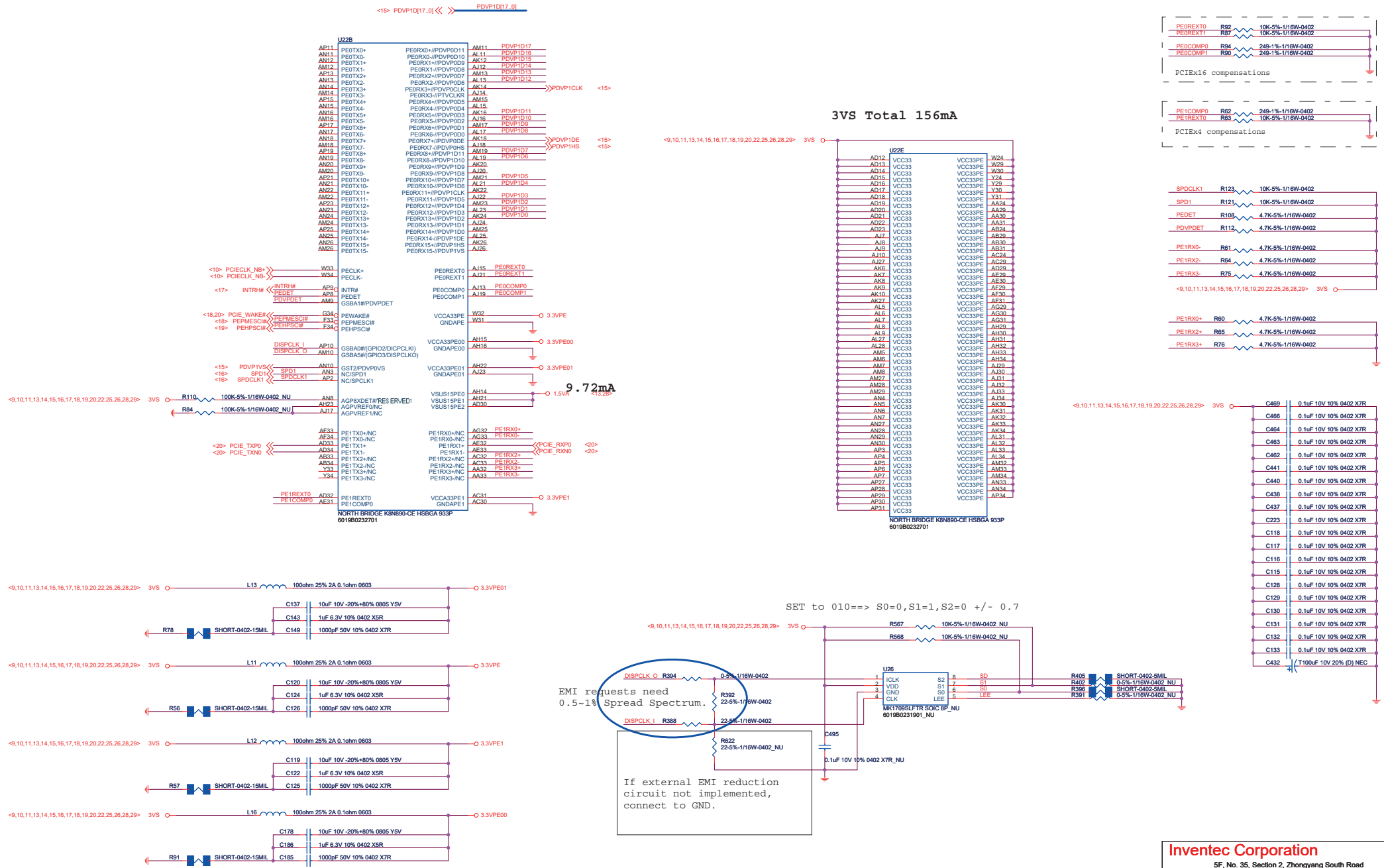
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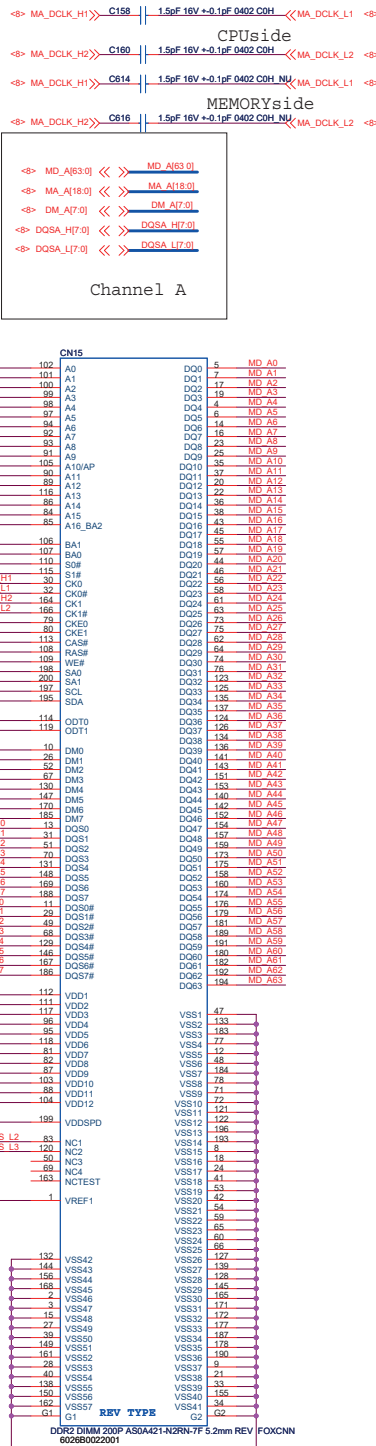
Note:
K8M890CE support 1 Xi Lane PCI Express
K8T900 support 4 Xi Lane or 1 X4 Lane PCI Express.



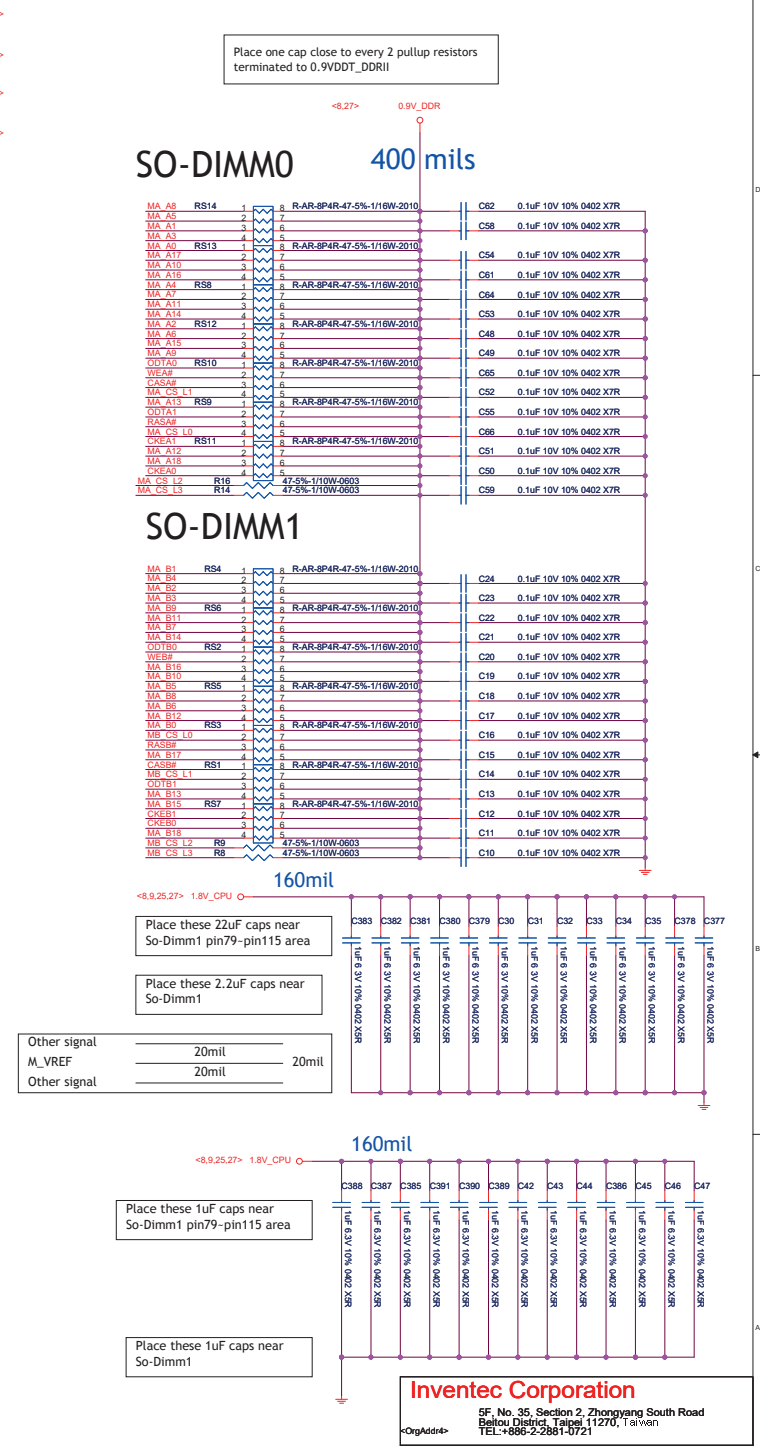
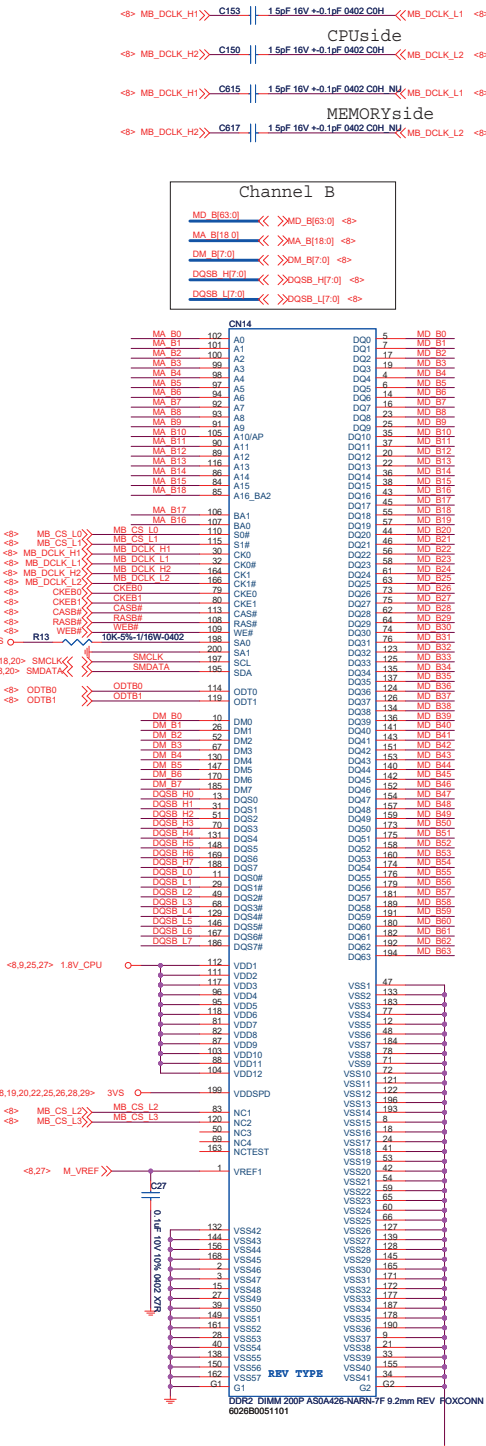
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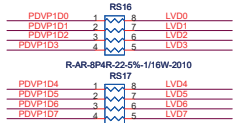
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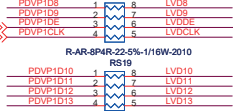
SO-DIMM1



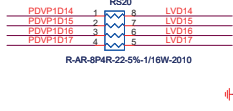
<12> PDVP1D[17..0] << PDVP1D[17..0]



R-AR-8PAR-22-5%-1/16W-2010



R-AR-8PAR-22-5%-1/16W-2010



R-AR-8PAR-22-5%-1/16W-2010

C75 5pF 50V 0.25% 0402 COG_NU

<12> PDVP1VS << PDVP1VS

<12> PDVP1HS << PDVP1HS

R372 22-5%-1/16W-0402

R344 22-5%-1/16W-0402

R FB

TYPE

MODEL

PDB

PANELREF

VREF

TYPE

MODEL

PDB

LVDS TRANS V11634AL LQFP 48P VIA

6019B0154201

LVDS0

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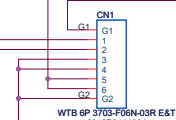
LVDS280

LVDS281

LVDS Interface

CABLE 28AWG

80mil



INVERT CONTROL

Please as close as possible to the LVDS CONN

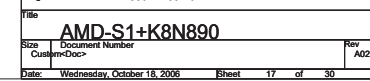
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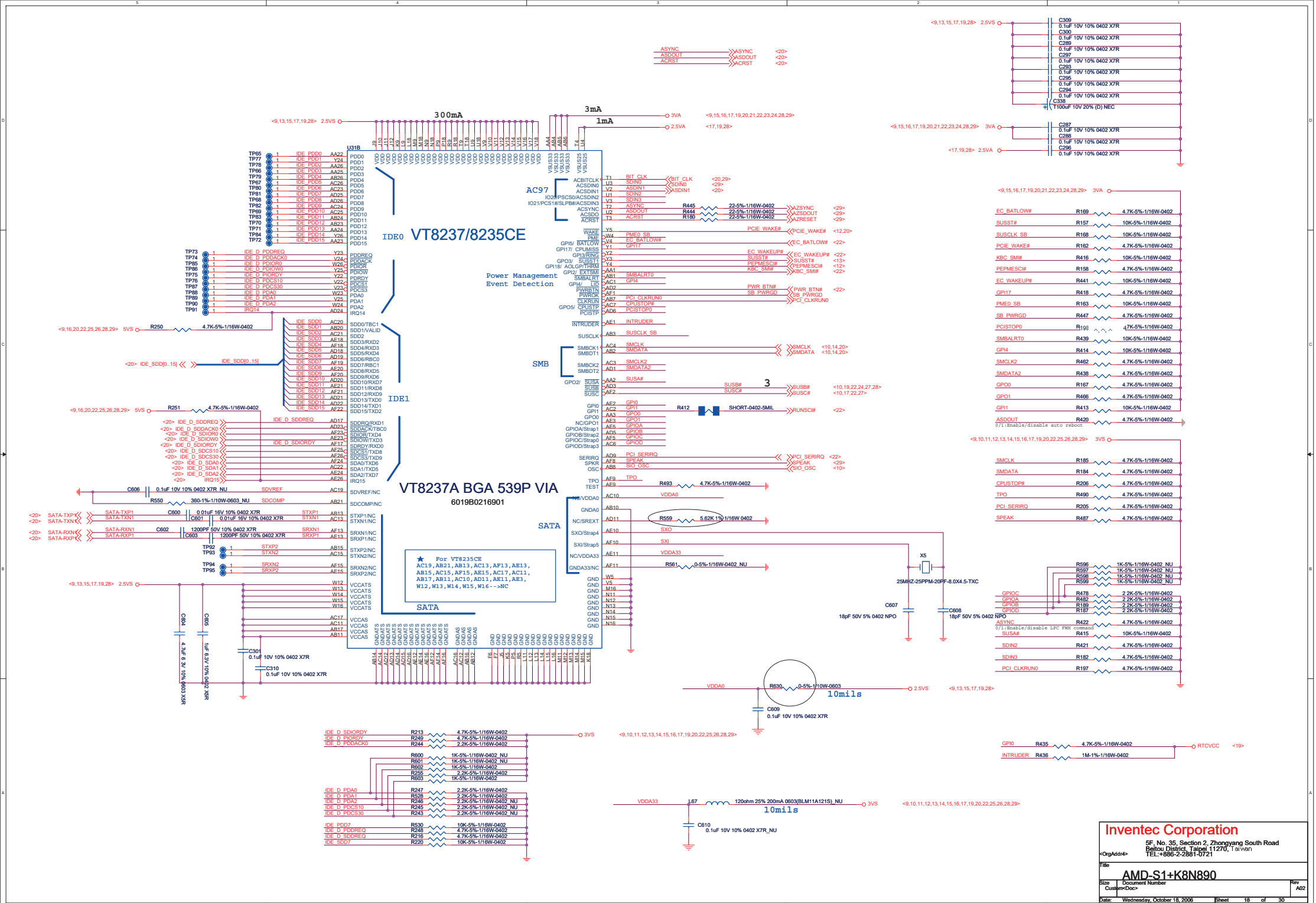
TOP SIDE

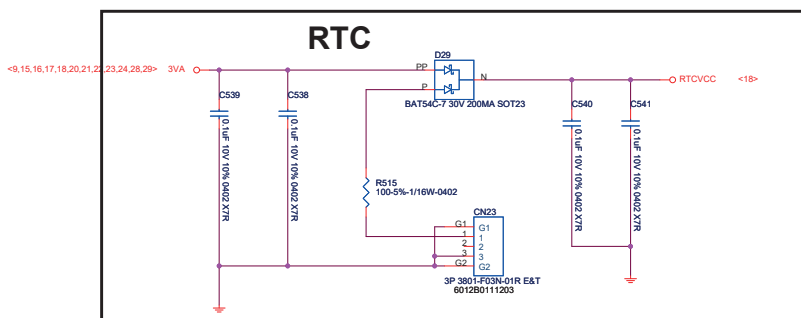
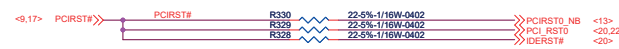
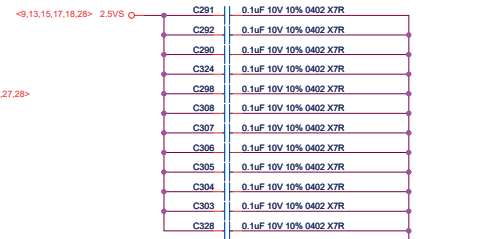
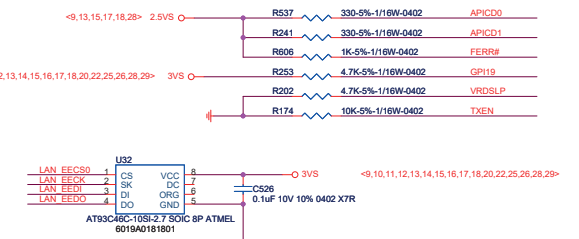
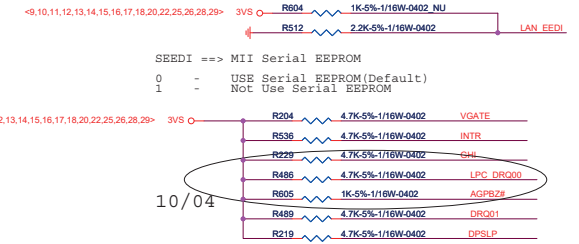
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Beitou District, Taipei 11270, Taiwan
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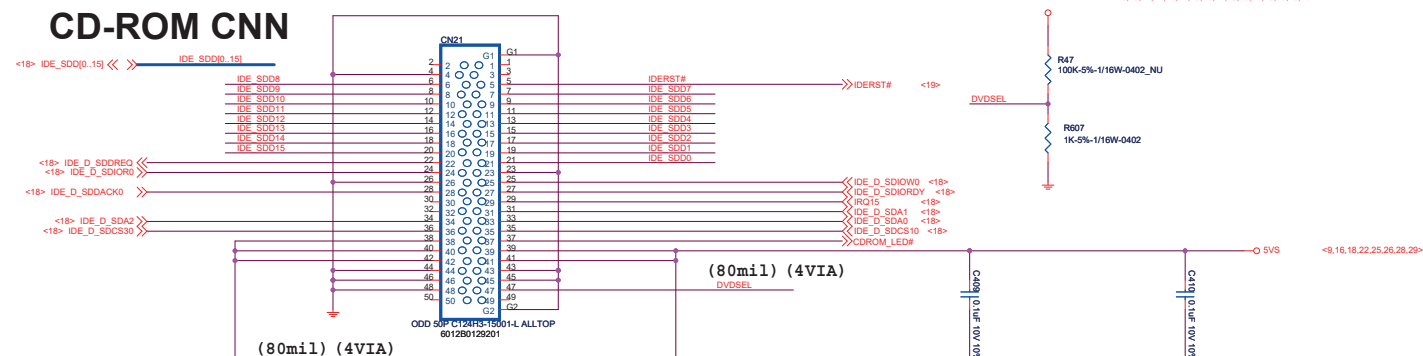
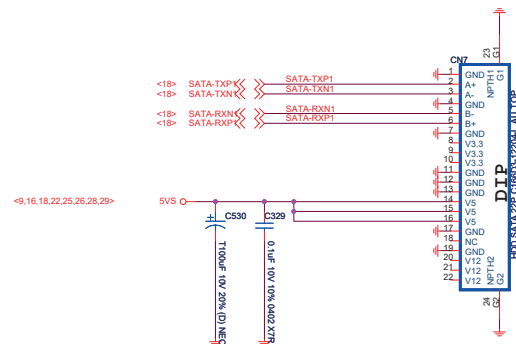
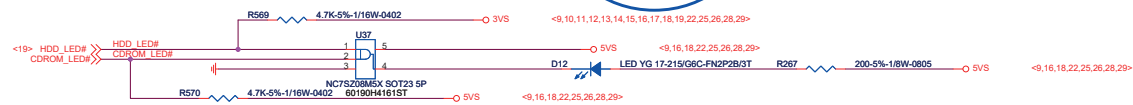
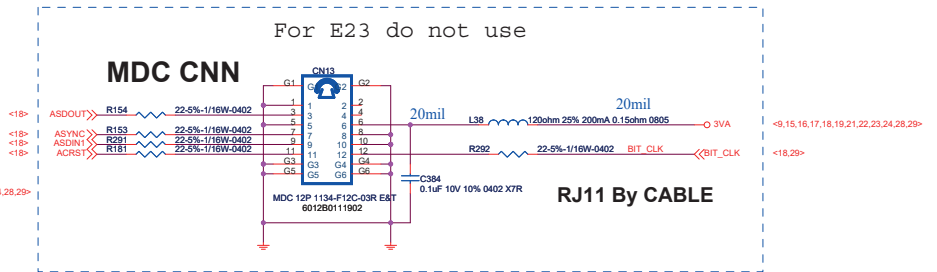
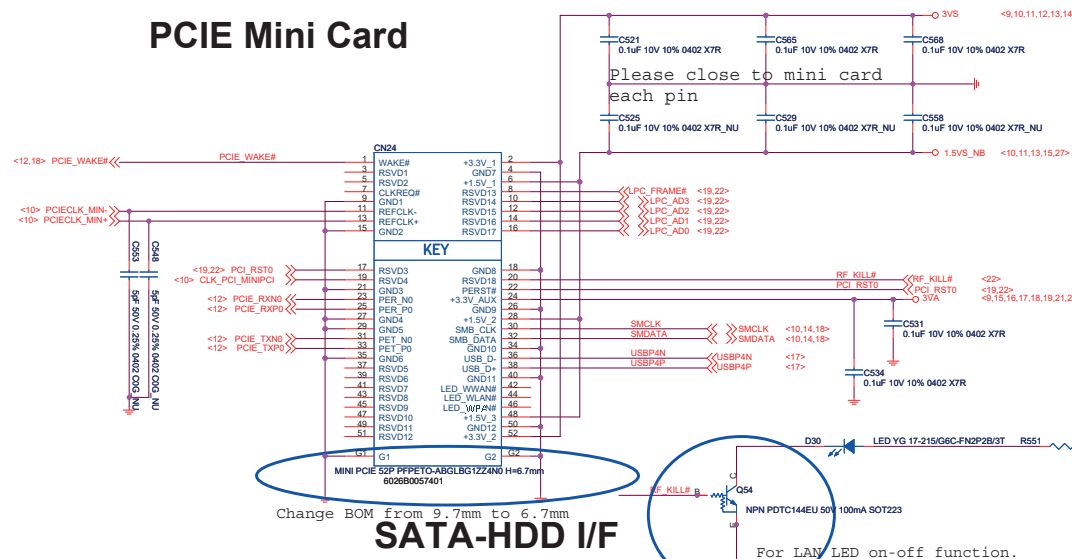
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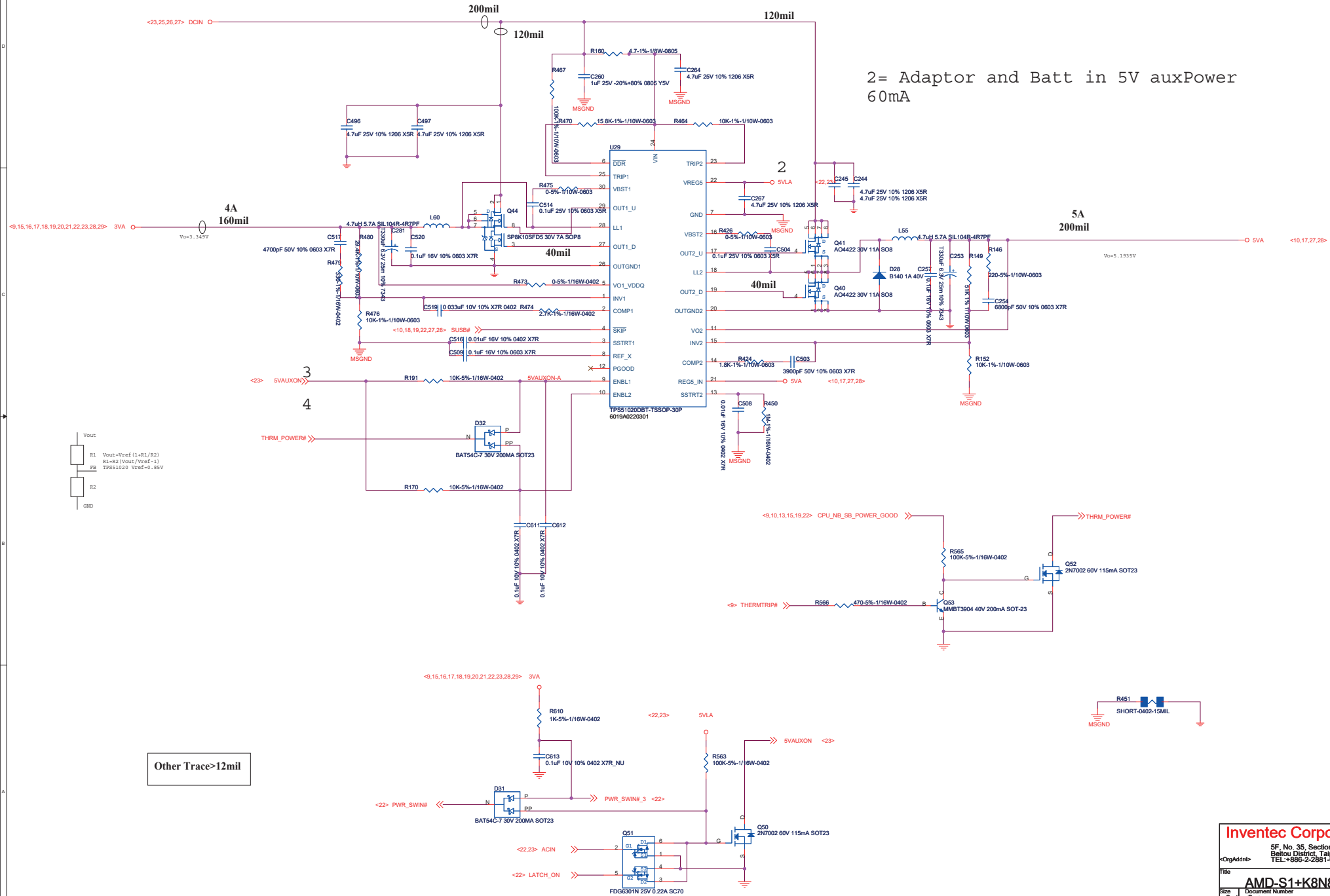




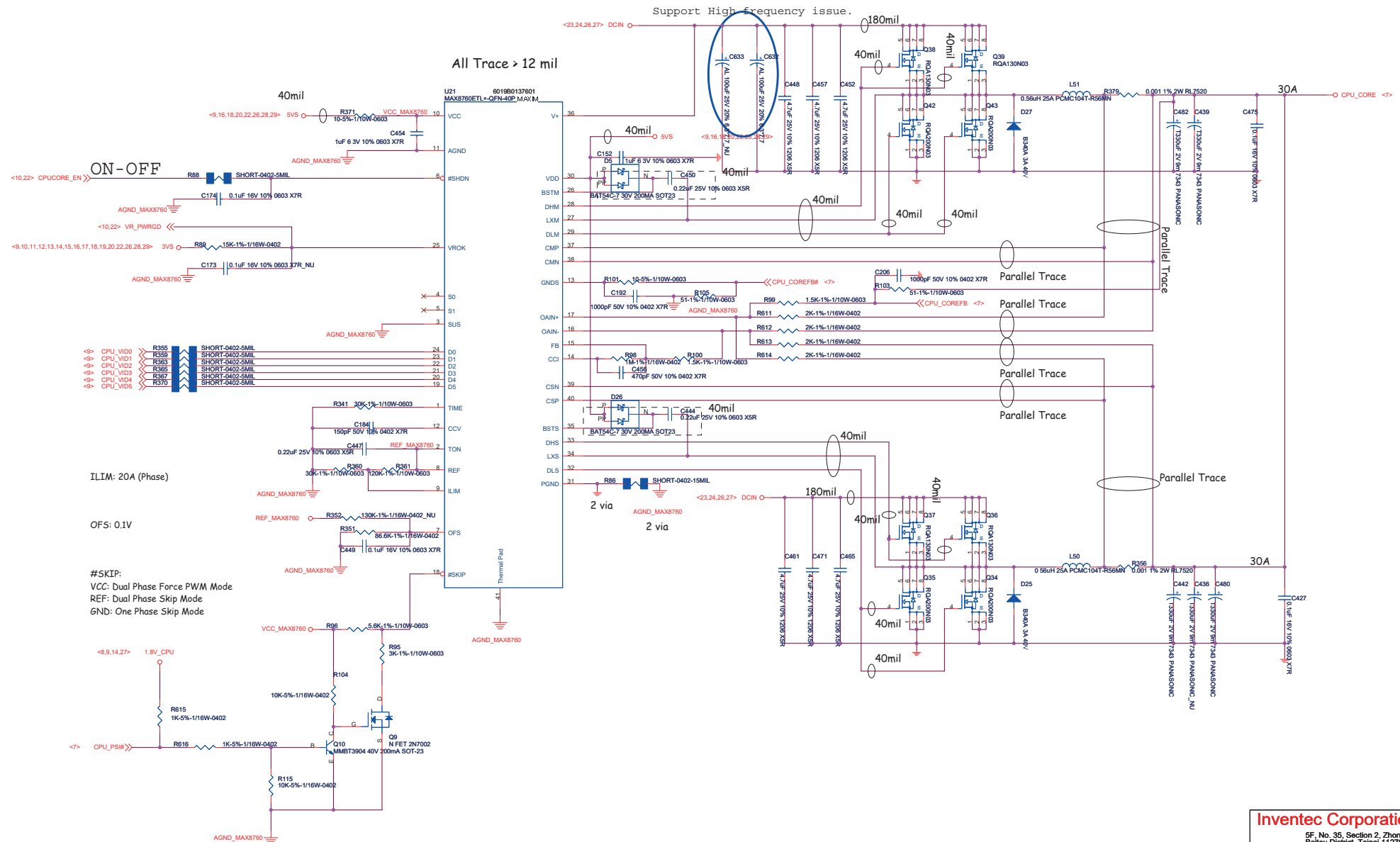
PCIE Mini Card



+V5A/+V5LA/+V3A/+V3LA

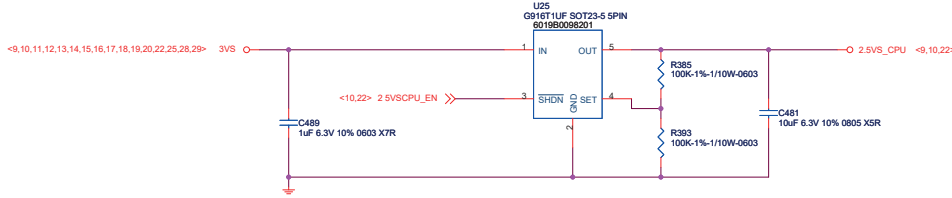


AMD K8 CPU Core Power (MAX8760)



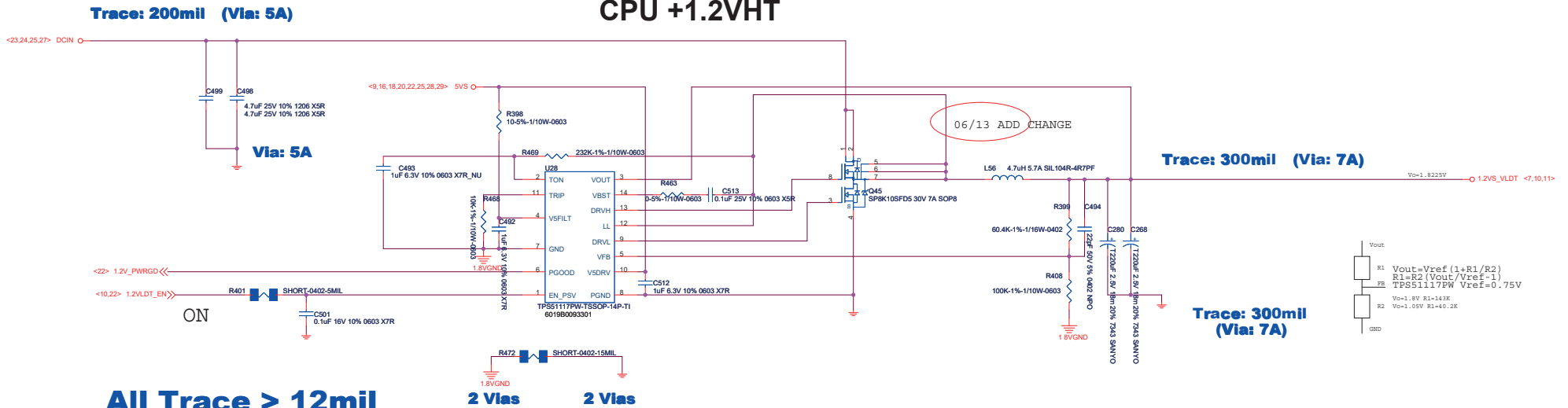
CPU 2.5V

1.8V_PWRGD to 2.5VS_CPU = 2ms



2.5VS_CPU to CPUCORE_EN = 2ms

CPU +1.2VHT



All Trace > 12mil

2 Vias

2 Vias

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