F-Tile JESD204C Intel® FPGA IP User Guide

Updated for Quartus® Prime Design Suite: **24.1**

IP Version: **2.2.0**

Online Version
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Contents

1. About the F-Tile JESD204C Intel® FPGA IP User Guide

This user guide provides the features, architecture description, steps to instantiate, and guidelines to design the F-Tile JESD204C Intel® FPGA IP using Agilex™ 7 and Agilex 9 devices.

Intended Audience

This document is intended for:

- Design architect to make IP selection during system level design planning phase
- Hardware designers when integrating the IP into their system level design
- Validation engineers during system level simulation and hardware validation phase

Related Documents

For other documents related to the JESD204C protocol, refer to the related information.

Acronyms and Glossary

Table 1. Acronym List

Acronym	Expansion
LEMC	Local Extended Multiblock Clock
FC	Frame clock rate
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
TX	Transmitter
RX	Receiver
DLL	Data link layer
CSR	Control and status register
CRU	Clock and Reset Unit
ISR	Interrupt Service Routine
FIFO	First-In-First-Out
SERDES	Serializer Deserializer
ECC	Error Correcting Code
FEC	Forward Error Correction
SERR	Single Error Detection (in ECC, correctable)

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Acronym	Expansion
DERR	Double Error Detection (in ECC, fatal)
PRBS	Pseudorandom binary sequence
MAC	Media Access Controller. MAC includes protocol sublayer, transport layer, and data link layer.
NPDME	Native PHY Debug Master Endpoint
PHY	Physical Layer. PHY typically includes the physical layer, SERDES, drivers, receivers and CDR.
PCS	Physical Coding Sub-layer
PMA	Physical Medium Attachment
RBD	RX Buffer Delay
UI	Unit Interval = duration of serial bit
RBD count	RX Buffer Delay latest lane arrival
RBD offset	RX Buffer Delay release opportunity
SH	Sync header
SRC	Soft reset controller
TL	Transport layer

Table 2. Glossary List

Term	Description
Converter Device	ADC or DAC converter
Logic Device	FPGA or ASIC
Octet	A group of 8 bits, serving as input to 64/66 encoder and output from the decoder
Nibble	A set of 4 bits which is the base working unit of JESD204C specifications
Block	A 66-bit symbol generated by the 64/66 encoding scheme
Link Clock	Link Clock = Lane Line Rate/66.
Frame	A set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal.
Frame Clock	A system clock which runs at the frame's rate, that must be 1x or 2x link clock.
Samples per frame clock	Samples per clock, the total samples in frame clock for the converter device.
LEMC	Internal clock used to align the boundary of the extended multiblocks between lanes and into the external references (SYSREF or Subclass 1).
Subclass 0	No support for deterministic latency. Data should be immediately released upon lane to lane deskew on receiver.
Subclass 1	Deterministic latency using SYSREF.
Multipoint Link	Inter-device links with 2 or more converter devices.
64B/66B Encoding	Line code that maps 64-bit data to 66 bits to form a block. The base level data structure is a block that starts with 2-bit sync header.
FEC	Forward error correction

Table 3. Symbols

Term	Description
L	Number of lanes per converter device
M	Number of converters per device
F	Number of octets per frame on a single lane
S	Number of samples transmitted per single converter per frame cycle
N	Converter resolution
N’	Total number of bits per sample in the user data format
CS	Number of control bits per conversion sample
CF	Number of control words per frame clock period per link
HD	High Density user data format
E	Number of multiblocks in an extended multiblock

Related Information

Related documents for JESD204C

2. Overview of the F-Tile JESD204C Intel FPGA IP

The F-Tile JESD204C Intel FPGA IP is a high-speed point-to-point serial interface for digital-to-analog (DAC) or analog-to-digital (ADC) converters to transfer data to FPGA devices. This unidirectional serial interface runs at a maximum data rate of 32.44032 Gbps. This protocol offers higher bandwidth, low I/O count and supports scalability in both number of lanes and data rates.

The F-Tile JESD204C Intel FPGA IP addresses multidevice synchronization using Subclass 1 to achieve deterministic latency.

The F-Tile JESD204C Intel FPGA IP supports true simplex, TX-only, RX-only, and Duplex (TX and RX) mode. The Intel FPGA IP is a unidirectional protocol where interfacing to ADC utilizes the transceiver RX path and interfacing to DAC utilizes the transceiver TX path.

The F-Tile JESD204C TX and RX cores run on a link clock with 64-bit data width, which reduces the area utilization.

The Intel FPGA IP incorporates:

- Media access control (MAC)—data link layer (DLL) and transport layer (TL) blocks that control the link states.
- Physical layer (PHY)—physical coding sublayer (PCS) and physical media attachment (PMA) block.

The transport layer (TL) in the MAC controls the assembling and disassembling of the frames.

Figure 1. F-Tile JESD204C Duplex Functional Block Diagram

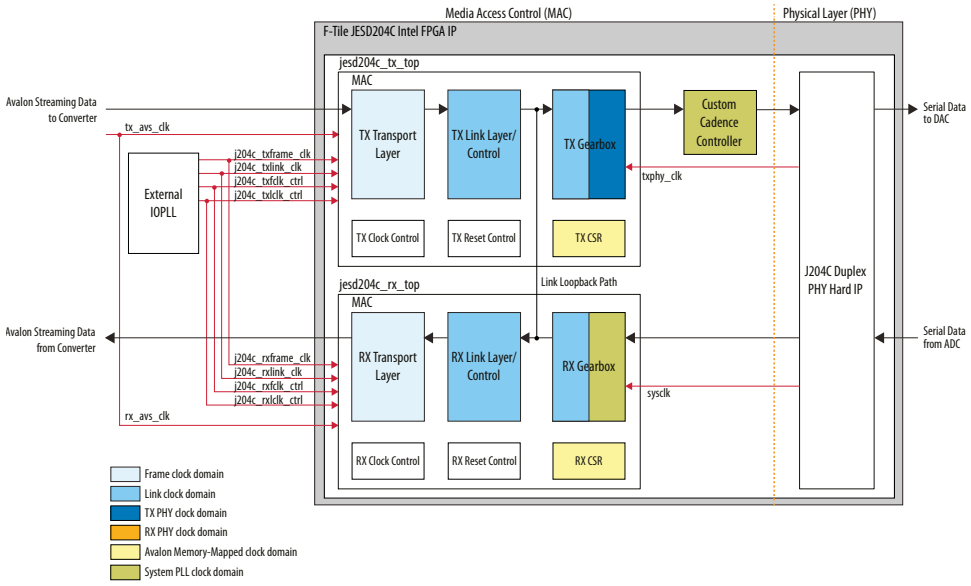


Figure 2. F-Tile JESD204C TX-only Functional Block Diagram

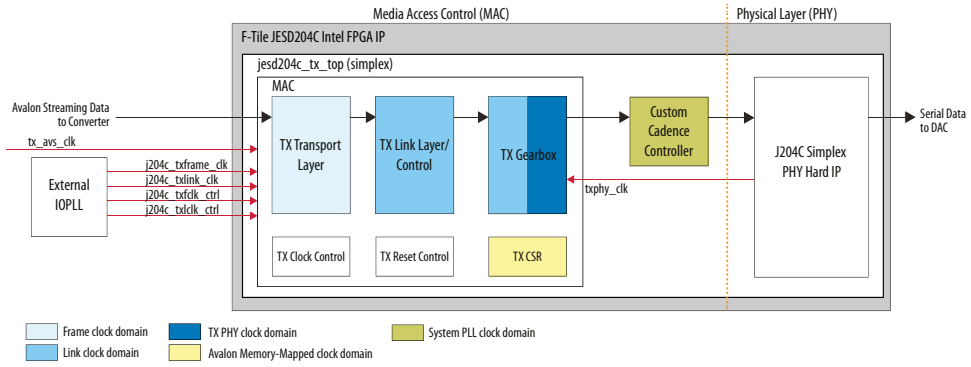
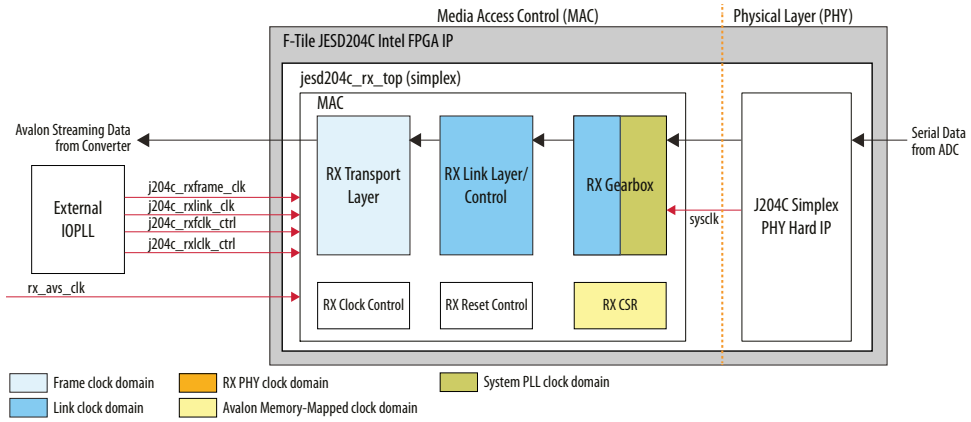


Figure 3. F-Tile JESD204C RX-only Functional Block Diagram



2.1. Release Information

Intel FPGA IP versions match the Quartus® Prime Design Suite software versions until v19.1. Starting in Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 4. F-Tile JESD204C Intel FPGA IP Release Information

Item	Description
IP Version	2.2.0
Quartus Prime Pro Edition Version	24.1
Release Date	2024.04.01
Ordering Code	IPS-JESD204

Related Information

F-Tile JESD204C Intel FPGA IP Release Notes
Provides information about the new features and updates for each IP release.

2.2. Device Family Support

Table 5. Intel Device Family Support

Device Family	Support Level
Agilex 7 (F-Tile) Agilex 9 (F-Tile)	Preliminary

The following terms define device support levels for Intel FPGA IP cores:

- Advance support—the IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- Preliminary support—the IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
- Final support—the IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

2.3. F-Tile JESD204C Intel FPGA IP Features

The F-Tile JESD204C Intel FPGA IP is a high-speed point-to-point serial interface intellectual property (IP). The F-Tile JESD204C Intel FPGA IP is the latest IP from Intel that supports the F-Tile JESD204C protocol. This IP is not backwards compatible and does not support JESD204B protocol. You can use the existing the JESD204B Intel FPGA IP to support JESD204B protocol.

Table 6. Brief Information about the F-Tile JESD204C Intel FPGA IP

Features	Description
Protocol Features	• Joint Electron Device Engineering Council (JEDEC) F-Tile JESD204C standard 2017 • Device subclass: — Subclass 0—No deterministic latency — Subclass 1—Uses SYSREF signal to support deterministic latency
Core Features	• Data rate of up to 32.44032 Gbps for Agilex 7 (F-tile) devices • Single or multiple lanes (up to 16 lanes per link) • Local extended multiblock clock (LEMC) counter based on E = 1 to 32 • Supports F = 1 to 256 octets per frame • Serial lane alignment and monitoring • Lane synchronization • Modular design that supports multidevice synchronization • MAC and PHY partitioning • Deterministic latency support • Interrupts and error handling support • System PLL clocking • 64/66 encoding • Scrambling/descrambling • Avalon® streaming interface for transmit and receive datapaths • Avalon memory-mapped interface for control and status registers (CSR) • Dynamic generation of simulation testbench • Bonded and non-bonded TX PMA mode

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