DVB-T channel receiver TDA10045H

FEATURES

- 2 and 8 kbytes Coded Orthogonal Frequency Division Multiplexer (COFDM) demodulator (fully DVB-T compliant: ETSI 300-744)
- All modes supported, including hierarchical modes
- Fully automatic transmission parameters detection (including Fast Fourier Transformer (FFT) size and guard interval)
- Digital Signal Processor (DSP) based synchronization (software can be upgraded on the fly)
- No extra-host software required
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 2nd or 1st IF variable analog input
- Only fundamental crystal oscillator required (4 MHz typical ±100 ppm)
- 6, 7 and 8 MHz channels with the same crystal
- Pulse killer algorithm to protect against impulse noise
- Digital frequency correction (±90 kHz)
- Frequency offset ($\pm^1/_6$ MHz) automatic estimator to speed-up the scan
- RF tuner input power measurement
- Parallel or serial transport stream interface
- BER measurement (before and after Viterbi decoder)
- Signal-to noise ratio estimation
- Constellation, CSI and channel frequency response outputs
- TPS bits I²C-bus readable (including spare ones)
- Controllable dedicated I²C-bus for the tuner (5 V tolerant)
- 3 low frequency spare DACs and 2 spare inputs
- CMOS 0.2 μm technology.

APPLICATIONS

- DVB-T fully compatible
- Digital data transmission using COFDM modulation.

GENERAL DESCRIPTION

The TDA10045H is a single-chip channel receiver for 2 and 8 kbytes COFDM modulated signals based on the ETSI specification (ETSI 300-744). The device interfaces directly to an IF signal, which could be either 1st or 2nd IF and integrates a 10-bit Analog-to-Digital Converter (ADC), a Numerically Controlled Oscillator (NCO) and a Phase-Locked Loop (PLL), simplifying external logic requirements and limiting system costs.

The TDA10045H performs all the COFDM demodulation tasks from IF signal to the MPEG-2 transport stream. An internal DSP core manages the synchronization and the control of the demodulation process, and implements specially developed software for robustness against co-channel and adjacent channel interference, to deal with Single Frequency Network (SFN) echo situations, and to assist in a very fast scan of the bandwidth. After baseband conversion and FFT demodulation, the channel frequency response is estimated, which is based on the scattered pilots, and filtered in both time and frequency domains. This estimation is used as a correction on the signal, carrier by carrier. A common phase error and estimator is used to deal with the tuner phase noise. The Forward Error Correction (FEC) decoder is automatically synchronized by the frame synchronization algorithm that uses the TPS information included in the modulation. An embedded 'pulse killer' algorithm enables the bad effects of short and strong impulsive noise interference that could be caused by electrical domestic devices and/or car traffic to be greatly reduced.

This device is controlled via an I²C-bus (master). The chip provides 2 switchable I²C-buses derived from the master: a tuner I²C-bus to be disconnected from the I²C-bus master when not necessary and an EEPROM I²C-bus. The DSP software code can be fed to the chip via the master I²C-bus or via the dedicated EEPROM I²C-bus.

Designed in 0.2 μm CMOS technology and housed in a 100 pin QFP package, the TDA10045H operates over the commercial temperature range.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		VERSION
	NAME	DESCRIPTION	
TDA10045H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

BLOCK DIAGRAM

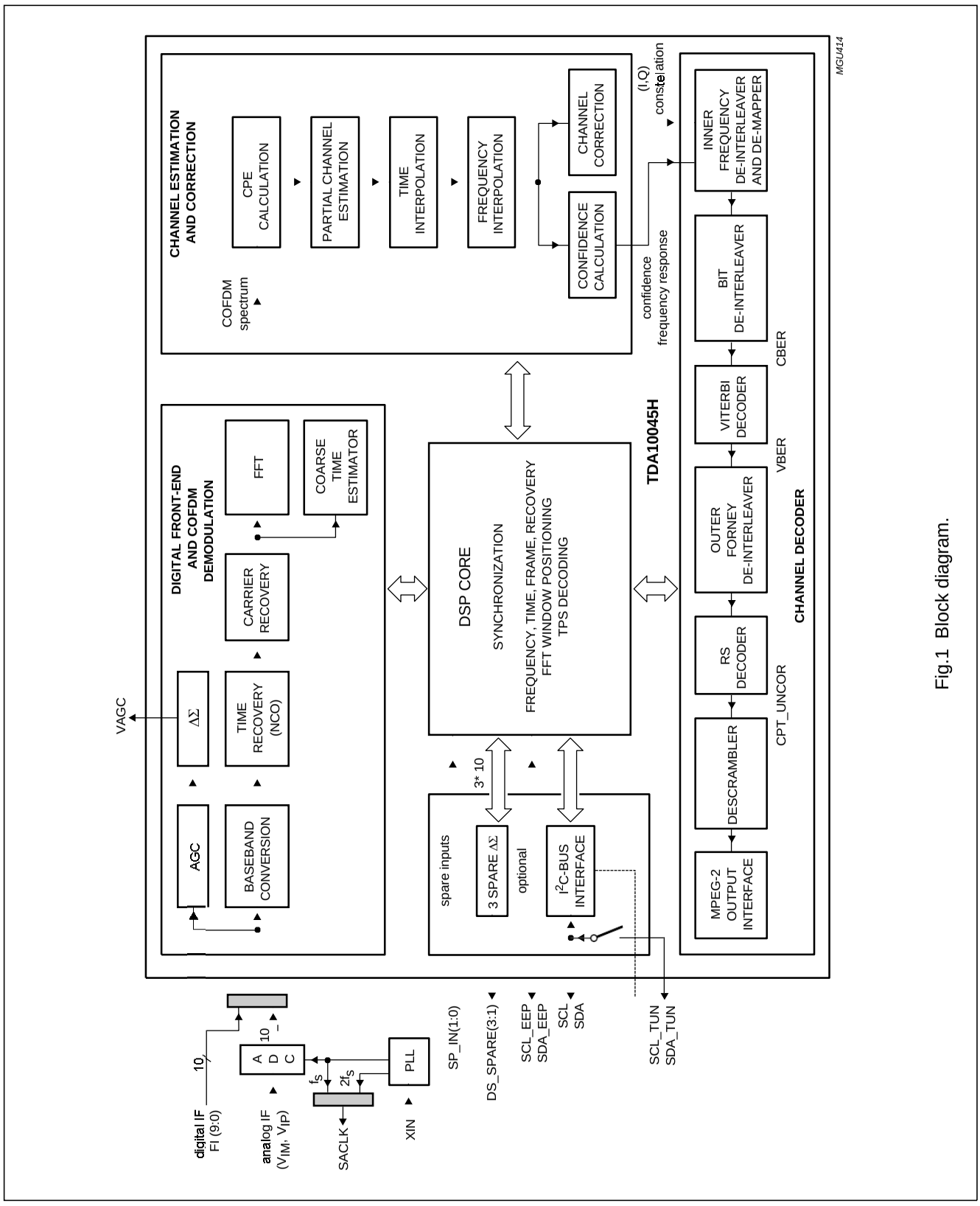

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{DDD33}	1	–	digital supply voltage for the pads (3.3 V typ.)
V_{SSD}	2	–	digital ground supply (0 V
DS_SPARE3	3	O	spare delta-sigma output; managed by the DSP to generate an analog level (after a RC low-pass filter)
VAGC	4	O	output value from the Delta-Sigma modulator, used to control a log-scaled amplifier (after analog filtering)
SCL_EEP	5	O	extra I^2C-bus clock to download DSP code from an external EEPROM (optional mode); can be connected to the master I^2C-bus
V_{DDD33}	6	–	digital supply voltage for the pads (3.3 V typ.)
V_{SSD}	7	–	digital ground supply (0 V)
SDA_EEP	8	I/OD	extra I^2C-bus data bus to download DSP code from an external EEPROM (optional mode). It can be connected to the master I^2C-bus; this pin is open-drain which requires an external pull-up resistor (to V_{DDD33} or V_{DDD50}), even if not used.
SCL_TUN	9	OD(1)	tuner I^2C-bus serial clock signal; this signal is derived from the master SCL and is open-drain which requires an external pull-up resistor (to V_{DDD33} or V_{DDD50}), even if not used
SDA_TUN	10	I/OD	tuner I^2C-bus serial data signal; this signal is derived from the master SDA and is open-drain which requires an external pull-up resistor (to V_{DDD33} or V_{DDD50}), even if not used
SCL	11	I(2)	I^2C-bus master serial clock; up to 700 kbit/s
SDA	12	I/OD	I^2C-bus master serial data input/output, open-drain I/O pad, which requires an external pull-up resistor (to V_{DDD33} or V_{DDD50})
n.c.	13	–	not connected
CLR#	14	I(2)	asynchronous reset signal; active LOW
EEPADDR	15	I(2)	EEPADDR is the LSB of the I^2C-bus address of the EEPROM. The MSBs are internally set to 101000. Therefore the complete I^2C-bus address of the EEPROM is (MSB to LSB): 1, 0, 1, 0, 0, 0, EEPADDR.
SADDR[1:0]	16 and 17	I(2)	SADDR[1:0] are the 2 LSBs of the I^2C-bus address of the TDA10045; the MSBs are internally set to 00010; therefore the complete I^2C-bus address of the TDA10045 is (MSB to LSB): 0, 0, 0, 1, 0, SADDR[1] and SADDR[0]
V_{DDD18}	18	–	digital supply voltage for the core (1.8 V typ.)
V_{SSD}	19	–	digital ground supply (0 V)
TM[3:0]	20 to 23	I(2)	test mode bus; for test purpose; must be set to ‘0000’
SCAN_EN	24	I(2)	scan enable for production test; connected to GND
V_{DDD50}	25	–	digital supply voltage (5 V typ.); can be set to 3.3 V (with caution) if the 5 V tolerant I/O is not required
V_{SSD}	26	–	digital ground supply (0 V)
DWNLOAD	27	I(2)	processor control, boot mode; if set to logic 0, the DSP downloads the software from an external EEPROM on the dedicated I^2C-bus (pins SDA_EEP and SCL_EEP). If set to logic 1 the software is downloaded in the I^2C-bus register CODE_IN from the host; in this case the external EEPROM is not needed.
SP_IN[1:0]	28 and 29	I(2)	spare inputs