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CHAPTER 1

Introduction to EL-12864A LCM

EL-12864A is a dot matrix graphic LCD module which is fabricated by low power COMS technology. It can display 128*64 dots size LCD panel using a 128*64 bit-mapped Display Data RAM (DDRAM). It interfaces with an 8-bit microprocessor.

Features

- Display format: 128*64 dots matrix graphic
- STN yellow-green mode
- Easy interface with 8-bit MPU
- Low power consumption
- LED back-light
- Viewing angle: 6 O'clock
- Driving method : 1/64 duty , 1/6.7 bias
- LCD driver IC: KS0108B(2) KS0107B
- Connector: Zebra

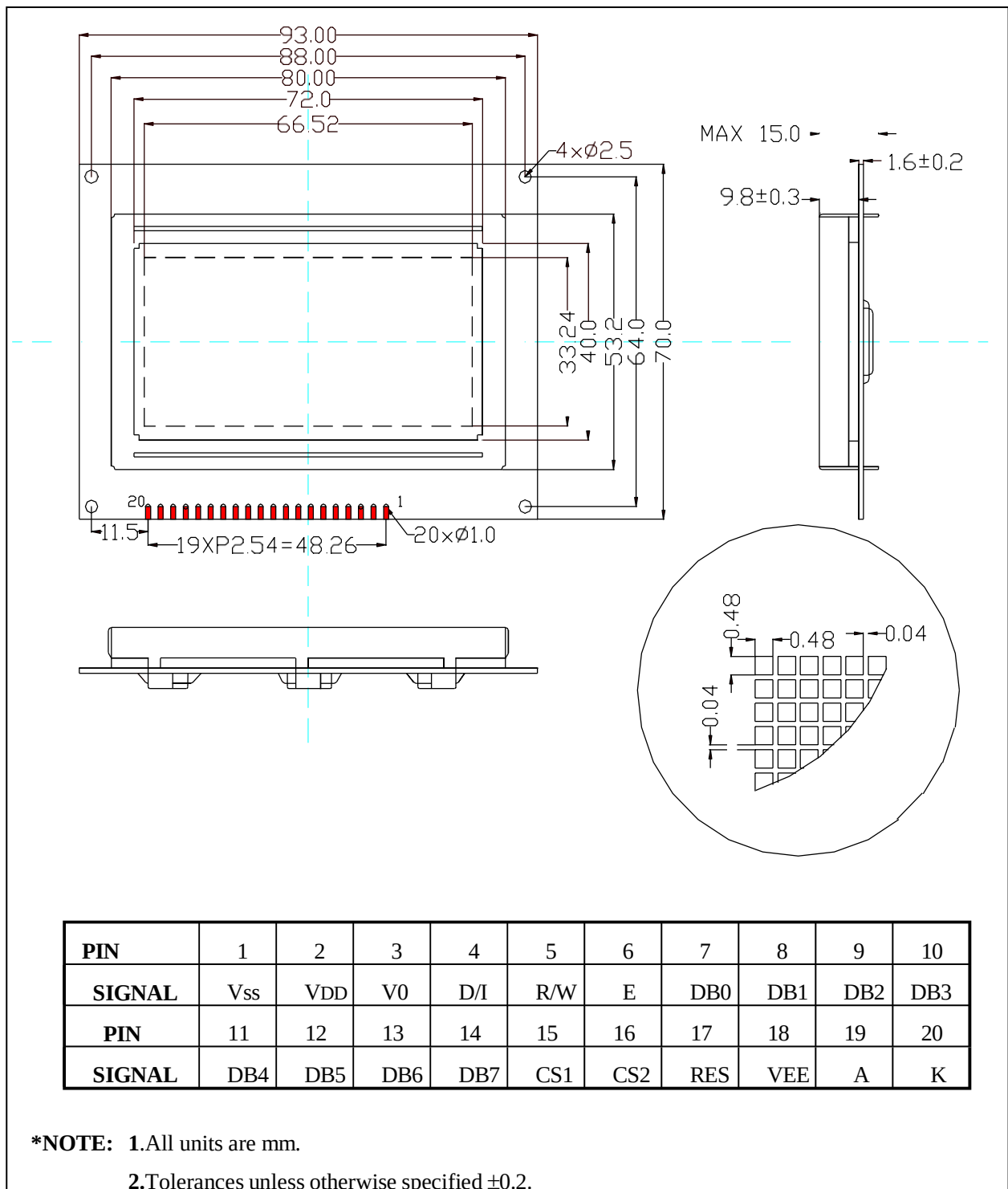
Mechanical Specifications

Item	Dimension	Unit
Module Size(W*H*T)	93.0*70.0*10.0	mm
Viewing Area(W*H)	72.0*40.0	mm
Number of Dots	128.0*64.0	PCS
Dot Size(W*H)	0.48*0.48	mm
Dot Pitch(W*H)	0.52*0.52	mm
Module Size With B/L	93.0*70.0*15.0	mm

Temperature Characteristics

Parameter	Symbol	Rating	Unit
Operating temperature	Topr	0 ~ +50	
Storage temperature	Tstg	-20 ~ +70	

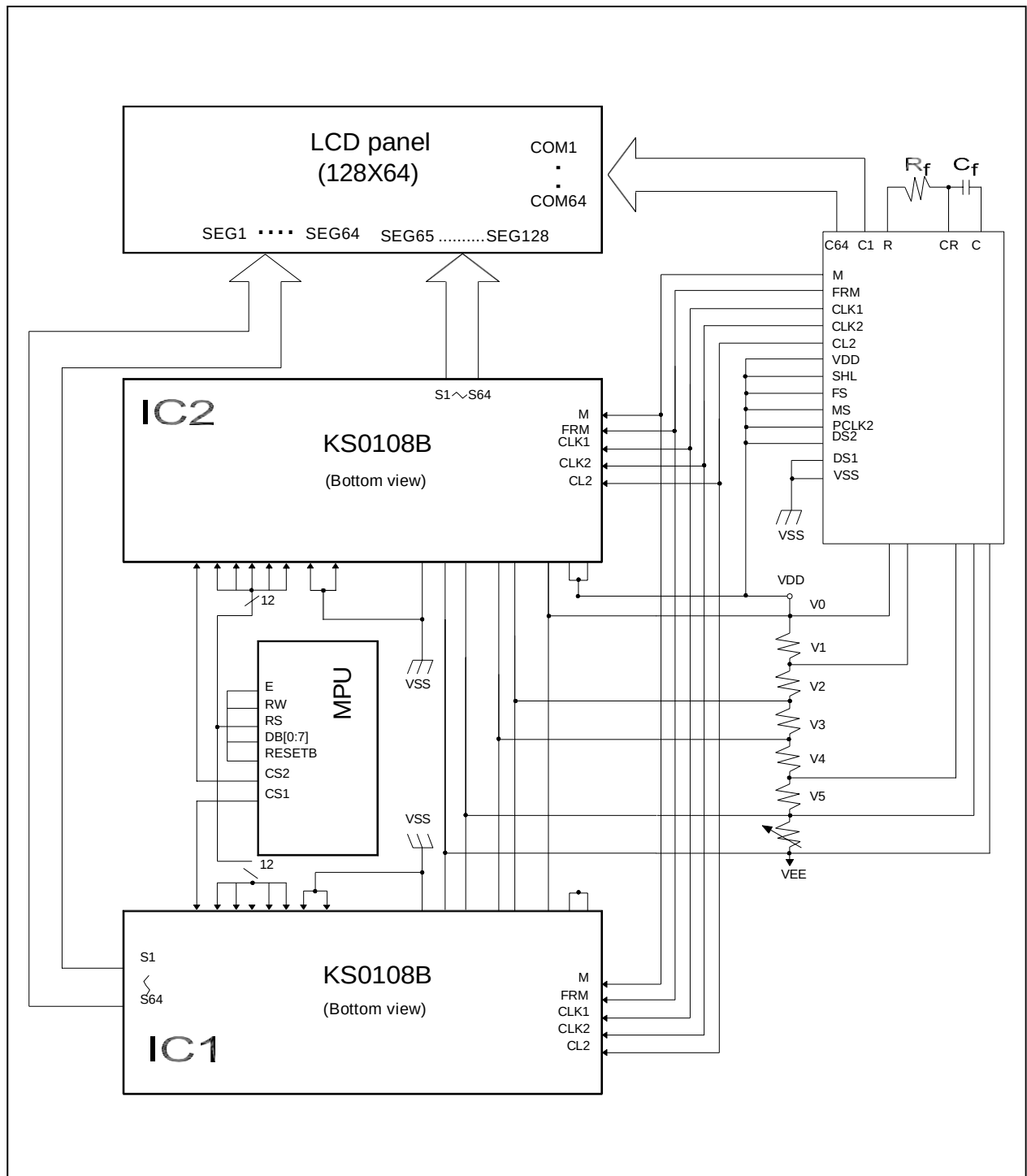
Figure 1. External Dimensions



PIN	1	2	3	4	5	6	7	8	9	10
SIGNAL	V _{SS}	V _{DD}	V ₀	D/I	R/W	E	DB0	DB1	DB2	DB3
PIN	11	12	13	14	15	16	17	18	19	20
SIGNAL	DB4	DB5	DB6	DB7	CS1	CS2	RES	VEE	A	K

ELATEC LCD MODULE EL-12864A

Figure 2. Application Diagram

***Note**

1/64 duty, 1/6.7 bias

 $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{EE}$

Electro-Optical characteristics

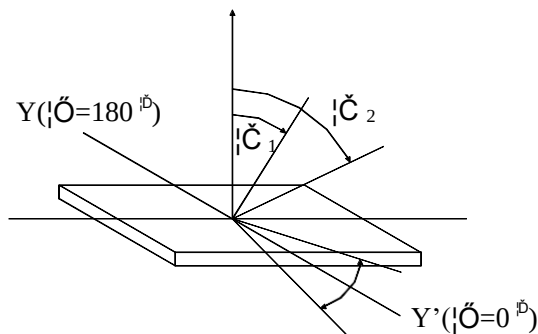
TN Type (Twisted Nematic)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle	$\frac{\theta_2 - \theta_1}{\varphi}$	40	-	-	deg.	Cr = 2.0	1,2
Contrast Ratio	Cr	-	4	-	-	$\theta = 20^\circ$ $\varphi = 0^\circ$	3
Response Time (rise)	t_R	-	110	-	ms	$\theta = 20^\circ$ $\varphi = 0^\circ$	4
Response Time (fall)	t_F	-	110	-	ms	$\theta = 20^\circ$ $\varphi = 0^\circ$	4

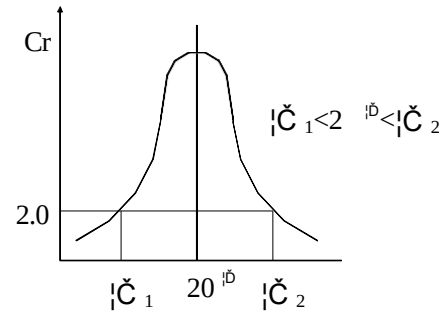
STN Type (Super Twisted Nematic)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle	$\frac{\theta_2 - \theta_1}{\varphi}$	70 -90	-	+90	deg.	Cr = 2.0	1,2
Contrast Ratio	Cr	-	4	-	-	$\theta = 20^\circ$ $\varphi = 0^\circ$	3
Response Time (rise)	t_R	-	110	-	ms	$\theta = 20^\circ$ $\varphi = 0^\circ$	4
Response Time (fall)	t_F	-	110	-	ms	$\theta = 20^\circ$ $\varphi = 0^\circ$	4

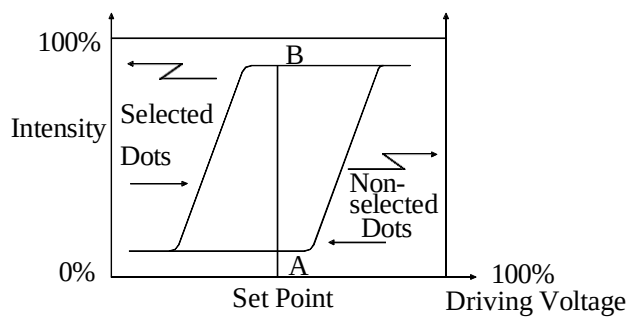
1. Definition of angle θ_1 & θ_2



2. Definition of viewing angle θ_1 & θ_2



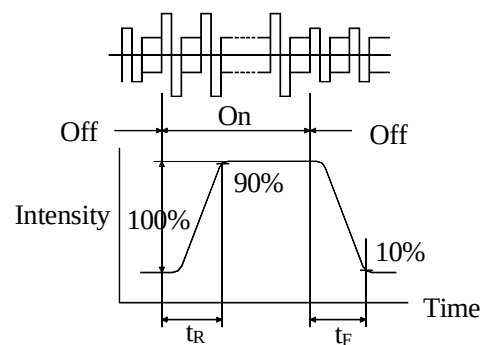
3. Definition of contrast Cr



$$Cr = (A / B)^P$$

Negative : P = -1
Positive : P = +1

4. Definition of optical response



Interface Pin Connections

Pin No.	Symbol	I/O Type	Description																				
1	VSS	Supply	Ground																				
2	VDD	Supply	Power supply																				
3	V0	Supply	LCD driver supply voltage																				
4	D/I		Data input/output pin of internal shift register																				
			<table><tr><th>MS</th><th>SHL</th><th>DIO1</th><th>DIO2</th></tr><tr><td>H</td><td>H</td><td>Output</td><td>Output</td></tr><tr><td>H</td><td>L</td><td>Output</td><td>Output</td></tr><tr><td>L</td><td>H</td><td>Input</td><td>Output</td></tr><tr><td>L</td><td>L</td><td>Output</td><td>Input</td></tr></table>	MS	SHL	DIO1	DIO2	H	H	Output	Output	H	L	Output	Output	L	H	Input	Output	L	L	Output	Input
MS	SHL	DIO1	DIO2																				
H	H	Output	Output																				
H	L	Output	Output																				
L	H	Input	Output																				
L	L	Output	Input																				
5	R/W		Read or Write																				
			<table><tr><th>RW</th><th>Description</th></tr><tr><td>H</td><td>Data appears at DB[7:0] and can be read by the CPU while E= H CS1B=L,CS2B=L and CS3=H.</td></tr><tr><td>L</td><td>Display data DB[7:0] can be written at falling edge of E when CS1B=L, CS2B=L and CS3=H.</td></tr></table>	RW	Description	H	Data appears at DB[7:0] and can be read by the CPU while E= H CS1B=L,CS2B=L and CS3=H.	L	Display data DB[7:0] can be written at falling edge of E when CS1B=L, CS2B=L and CS3=H.														
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6	E		Enable signal																				
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H	Read data in DB[7:0] appears while E= “High”.																						
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7	DB0	I/O	Data bus [0~7]																				
8	DB1		Bi-directional data bus																				
9	DB2																						
10	DB3																						
11	DB4																						
12	DB5																						
13	DB6																						
14	DB7																						
15	CS1	I	Chip selection																				
16	CS2		When CS1=H,CS2=L, select IC1																				
			When CS1=L,CS2=H, select IC2																				
17	RESETB	I	Reset signal.																				
			When RSTB=L																				
			1 ON/OFF register becomes set by 0.(display off)																				
			2 display start line register becomes set by 0 (Z-address 0 set, display from line 0)																				
			3 After releasing reset , this condition can be changed only by instruction.																				
18	VEE	Power	VEE is connected by the same voltage.																				
19	A		Back-light anode																				
20	K		Back-light cathode																				

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