Chunghwa Picture Tubes, Ltd.
Technical Specification

To :
Date :

CPT TFT-LCD

CLAA181EA01

ACCEPTED BY :

TENTATIVE 1

APPROVED BY	CHECKED BY	PREPARED BY
		TFT-LCD Plant Application Div.

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1.OVERVIEW

CLAA181EA01 is 18.1" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver Ics, control circuit and backlight.

By applying 8 bit digital data, 1280×1024, 16.7M-color images are displayed on the 18.1" diagonal screen. Input power voltage is 12.0V for LCD driving.

Inverter for backlight is not included in this module. General specification are summarized in the following table:

ITEM	SPECIFICATION
Display Area(mm)	359.0(H)x287.2(V) (18.1-inch diagonal)
Number of Pixels	1280(H)x1024(V)
Pixel Pitch(mm)	0.2805(H)x0.2805(V)
Color Pixel Arrangement	RGB vertical strip
Display Mode	normally white TN
Number of Colors	16.7M(8bits/color)
Brightness(cd/m^2)	(250)cd/m^2(Typ.)
Viewing Angle	-75~75(H),-60~50(V)(Typ.)
Surface Treatment	Anti-glare
Electrical Interface	LVDS , 2Ch
Total Module Power(W)	(Typ.)
Optimum Viewing Angle	6 o'clock
Module Size(mm)	389.0(H)x317.2"(H)x16.4"(D)
Module Weight(g)	2000
Backlight Unit	CCFL, 4 tables, edge-light(top/bottom)

The LCD Products listed on this document are not suitable for use of aerospace equipment, submarine cables, nuclear reactor control system and life support systems. If customers intend to use these LCD products for above application or not listed in "Standard" as follows, please contact our sales people in advance.

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tool, Industrial robot, Audio and Visual equipment, Other consumer products.

2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT
Power Supply Voltage for LCD	VCC	-0.3	13.2	V
Logic Input Voltage	VI	-0.3	3.6	V
Lamp Voltage	VL	0	2500	Vrms
Lamp Current	IL	0	10.0	mArms
Lamp Frequency	FL	-	100	kHz
Operation Temperature *1)	Top	0	50	℃
Storage Temperature *1)	Tstg	-20	60	℃

Note:

*1)Humidity

Relative Humidity ≦90% (Ta≦ 40℃)

Wet Bulb Temperature ≦40℃(Ta≧40℃)

3. ELECTRICAL CHARACTERISTICS

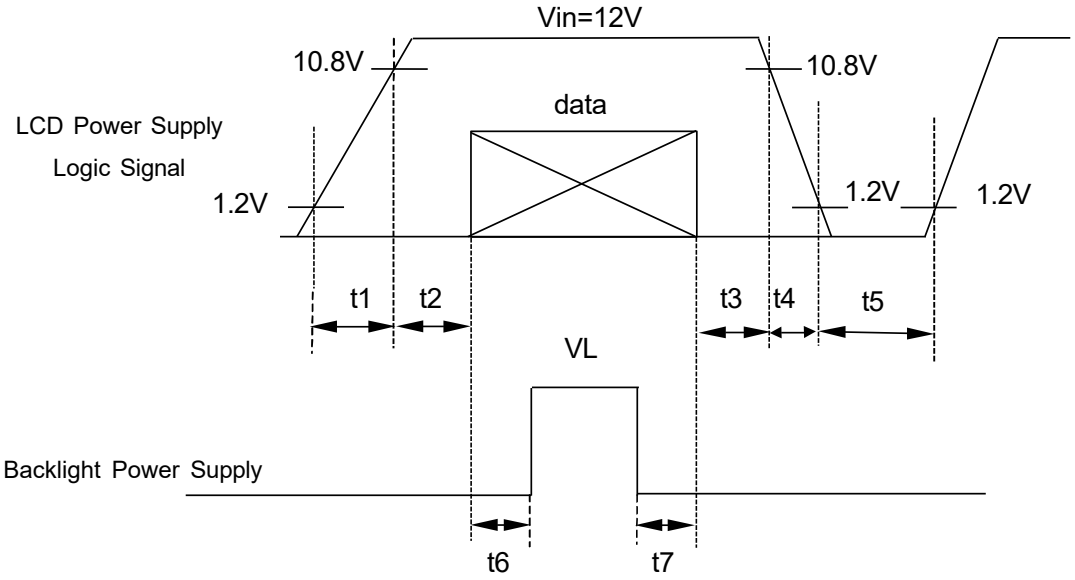
(a) TFT-LCD

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	Remark
Power Supply Voltage for LCD		Vin	10.8	12.0	13.2	V	Note1
Power Supply Current for LCD		Iin	-	(400)	(800)	mA	Note2
Permissive Input Ripple Voltage		VRP	-	-	100	mVp-p	Vcc=12.0V
Differential impedance		Zm	90	100	110	Ω	
Input Threshold Voltage	High	VIH	2.5	3.3	3.6	V	
	Low	VIL	0	-	0.8	V	

[Note 1]

VCC-turn-on conditions:

t1≦10ms
0.01< t2≦50ms
0.01< t3≦20ms
0.01< t4≦10 ms
3sec≦t5
200ms≦t6
200ms≦t7

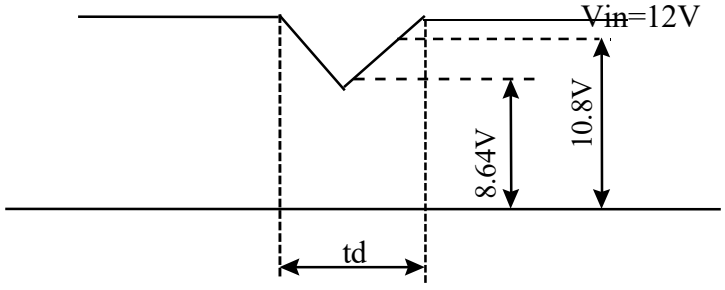


Data: RGB DATA, DCLK, HD, VD, DENA

VCC-dip conditions

1) When 8.64V≦Vin(min)<10.8V
td≦10 ms

2) When Vin > 10.8V
VCC-dip conditions should also follow the VCC-turn-on conditions.



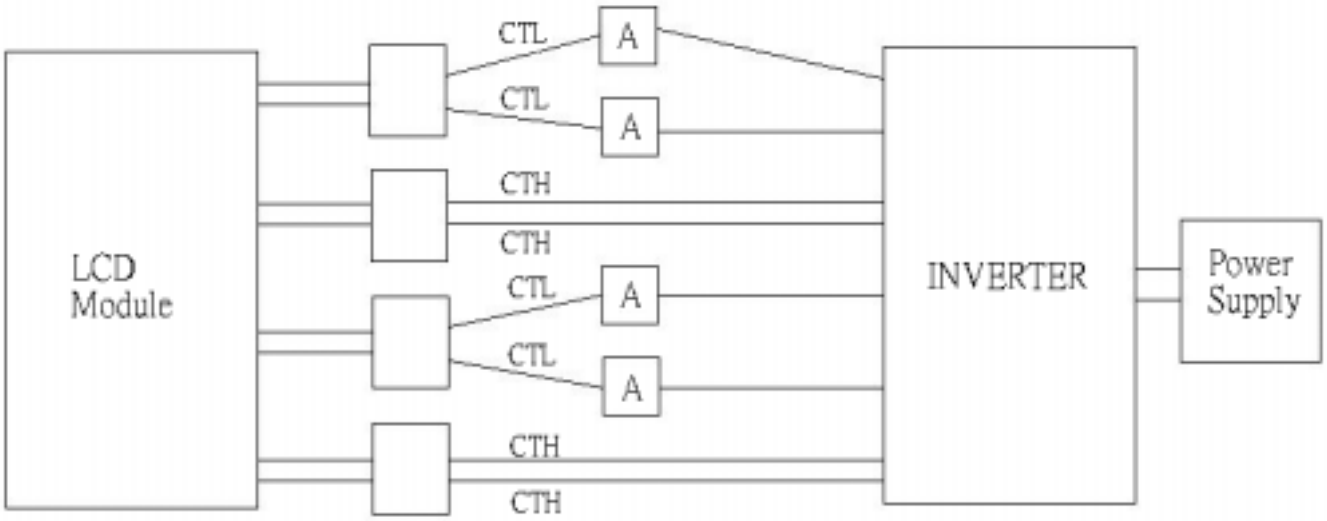
[Note 2] Typical current situation : 1280 line mode, Vin=12.0V,Fh=64Khz,Fv=60Hz,Fclk=54 MHz .

(b)Backlight

Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
Lamp Voltage	VL	-	(740)	-	V	IL=6.0mA
Lamp Current	IL	5.0	(6.0)	8.0	mA	Note1
Interter Frequency	FL	45	-	70	kHz	Note2
Starting Lamp Voltage	VS	1810	-	-	V	Ta=0℃
		1450	-	-	V	Ta=25℃
Lamp life Time	LT	--	50000	-	hr	Note3 IL=6.0mA Continuous Operation

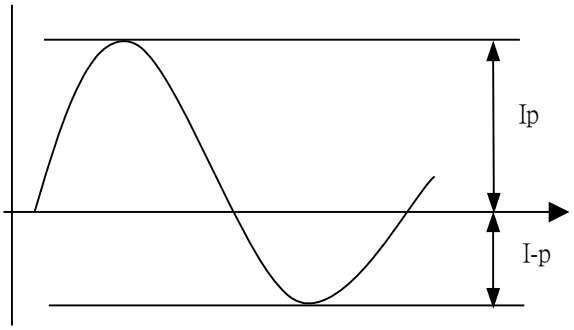
[Note 1]
Lamp Current measurement method (The current meter is inserted in cold line)



[Note 2]
Lamp frequency of inverter may produce interference with horizontal synchronous frequency,and this may cause horizontal beat on the display.Therefore,please adjust lamp frequency,and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

[Note 3] Lamp life time is defined as the time either when the brightness becomes 50% of the initial value,or when the starting lamp voltage does not meet the value specified in this table .

[Note 4] The degrees of unbalance： ＜10%
The ratio of wave height： ＜$\sqrt{2}$ ±10%



Ip：high side peak

I-p：low side peak

A：The degrees of unbalance = | Ip－I-p | / Irms ×100 (%)
B：The ratio of wave height = Ip (or I-p) / Irms

4. INTERFACE PIN CONNECTION

(a) CN1(Data Signal and Power Supply)

Used connector:FI-XB30S-HF10(JAE)

Pin No. of used connector	Pin No. of mating connector	symbol	Function
1	-	GND	Ground
2	2	VCC	(+12V)
3	3	VCC	(+12V)
4	4	VCC	(+12V)
5	5	VCC	(+12V)
6	6	GND	Ground
7	7	GND	Ground
8	8	TEST	NC
9	9	GND	Ground
10	10	RO0-	Negative LVDS differential data input. Channel O0(Odd)
11	11	RO0+	Positive LVDS differential data input. Channel O0(Odd)
12	12	RO1-	Negative LVDS differential data input. Channel O1(Odd)
13	13	RO1+	Positive LVDS differential data input. Channel O1(Odd)
14	14	RO2-	Negative LVDS differential data input. Channel O2(Odd)
15	15	RO2+	Positive LVDS differential data input. Channel O2(Odd)
16	16	ROCLK-	Negative LVDS differential clock input. (Odd)
17	17	ROCLK+	Positive LVDS differential clock input. (Odd)
18	18	RO3-	Negative LVDS differential data input. Channel O3(Odd)
19	19	RO3+	Positive LVDS differential data input. Channel O3(Odd)
20	20	GND	Ground
21	21	RE0-	Negative LVDS differential data input. Channel E0(Even)
22	22	RE0+	Positive LVDS differential data input. Channel E0(Even)
23	23	RE1-	Negative LVDS differential data input. Channel E1(Even)
24	24	RE1+	Positive LVDS differential data input. Channel E1(Even)
25	25	RE2-	Negative LVDS differential data input. Channel E2(Even)
26	26	RE2+	Positive LVDS differential data input. Channel E2(Even)
27	27	RECLK-	Negative LVDS differential clock input. (Even)
28	28	RECLK+	Positive LVDS differential clock input. (Even)
29	29	RE3-	Negative LVDS differential data input. Channel E3(Even)
30	30	RE3+	Positive LVDS differential data input. Channel E3(Even)
31	31	GND	Ground
32	-	GND	Ground

(b)CN2,3(BACKLIGHT)

Backlight-side connector: BHSR-02VS-1

Inverter-side connector: SM02B-BHSS-1(JST)

Pin No.	Symbol	Function
1	CTH1	VBLH1(High voltage)
2	CTH2	VBLH2(High voltage)

(c)CN4,5(BACKLIGHT)

Backlight-side connector: BHR-02VS-1

Inverter-side connector: SM02(4.0)B-BHS-1(JST)

Pin No.	Symbol	Function
1	CTL1	VBLL(Low voltage)
2	CTL2	VBLL(Low voltage)

[Note]

VBLH-VBLL = VL

5. INTERFACE TIMING

(a)Timing Specifications

ITEM		SYMBOL	MIN	TYP	MAX	UNIT
DCLK	Frequency	f_{CLK}	50	54	60	MHz
	Period	t_{CLK}	16.7	18.5	20	ns
DATA Enable DENA *3)	Horizontal Active Time	tHA	640	640	640	tCLK
	Horizontal Front Porch	tHFP	0	24	-	tCLK
	Horizontal Back Porch	tHBP	9	180	-	tCLK
	Vertical Active Time	tVA	1024	1024	1024	tH
	Vertical Front Porch	tVFP	0	1	-	tH
	Vertical Back Porch	tVBP	2	41	-	tH
HD *2) *4)	Frequency	f_H	–	64	77.7	KHz
	Period	t_H	649	844	–	t_{CLK}
	Pulse Width(low)	t_{WHL}	1	56	–	t_{CLK}
VD *2)	Frequency	f_V	55	60	75	Hz
	Period	t_V	1026	1066		t_H
	Pulse Width(low)	t_{WVL}	1	3	–	t_H

[Note]

1) Polaritites of HD and VD are negative in this specification.
2) DENA(Data Enable)should always be positive polarity as shown in the timing specification.
3) DCLK should appear during all blanking period, and HD should appear during blanking period of frame cycle.
4) LVDS transmitter IC ：DS90C383MTD(NS) or SN75LVDS83(TI) .

[Note]

Required signal assignment for flat link transmitter

Pin	Pin	Require Signal	Pin	Pin Name	Require Signal
1	VCC	Power Supply for TTL Input	29	GND	Ground pin for TTL
2	D5	TTL Input (R7)	30	D26	TTL Input(DE)
3	D6	TTL Input (R5)	31	TxCLKIN	TTL Level clock Input
4	D7	TTL Input (G0)	32	PWR DWN	Power Down Input
5	GND	Ground pin for TTL	33	PLL GND	Ground pin for PLL
6	D8	TTL Input (G1)	34	PLL VCC	Power Supply for PLL
7	D9	TTL Input (G2)	35	PLL GND	Ground pin for PLL
8	D10	TTL Input (G6)	36	LVDS GND	Ground pin for LVDS
9	VCC	Power Supply for TTL Input	37	TxOUT3+	Positive LVDS differential data
10	D11	TTL Input (G7)	38	TxOUT3-	Negative LVDS differential data
11	D12	TTL Input (G3)	39	TxCLKOUT+	Positive LVDS differential clock
12	D13	TTL Input (G4)	40	TxCLKOUT-	Negative LVDS differential clock
13	GND	Ground pin for TTL	41	TxOUT2+	Positive LDVS differential data
14	D14	TTL Input (G5)	42	TxOUT2-	Negative LVDS differential data
15	D15	TTL Input (B0)	43	LVDS GND	Ground pin for LVDS
16	D16	TTL Input (B6)	44	LVDS VCC	Power Supply for LVDS
17	VCC	Power Supply for TTL Input	45	TxOUT1+	Positive LVDS differential data
18	D17	TTL Input (B7)	46	TxOUT1-	Negative LVDS differential data
19	D18	TTL Input (B1)	47	TxOUT0+	Positive LVDS differential data
20	D19	TTL Input (B2)	48	TxOUT0-	Negative LVDS differential data
21	GND	Ground pin for TTL	49	LVDS GND	Ground pin for TTL
22	D20	TTL Input (B3)	50	D27	TTL Input (R6)
23	D21	TTL Input (B4)	51	D0	TTL Input (R0)
24	D22	TTL Input (B5)	52	D1	TTL Input (R1)
25	D23	TTL Input (LVDS)	53	GND	Ground pin for TTL
26	VCC	Power Supply for TTL Input	54	D2	TTL Input (R2)
27	D24	TTL Input (HSYNC)	55	D3	TTL Input (R3)
28	D25	TTL Input (VSYNC)	56	D4	TTL Input (R4)