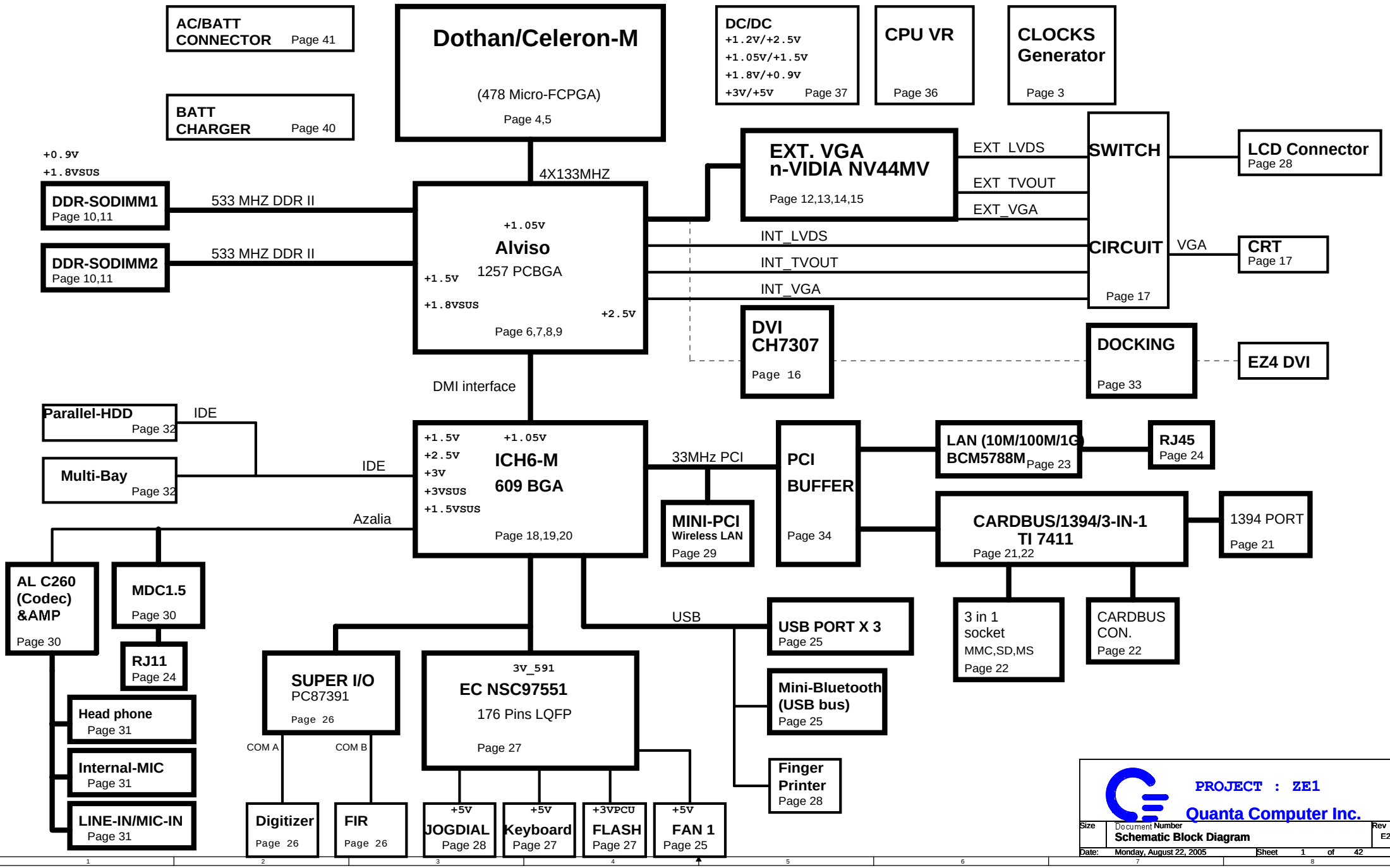
ZE1

REV : E2C



PROJECT : ZE1

Quanta Computer Inc.

Size	Document Number	Rev
	Schematic Block Diagram	E2C
Date: Monday, August 22, 2005	Sheet 1 of 42	

B TEST CHANGE ITMES:

06/22 MODIFY LIST

1. Remove all no-use text meno, ie: Rev A2.
2. Page 12. Chage R157, R158, R162~R167 power source from +3V to IFPC_IOVDD.
3. Page 15. Add R615, R616, R614 Q44 and Q43. Follow nVIDIA's suggestion. TMDS Backdrive Prevention circuit.
4. Page 16. Change single R to RN. R62, R63 => RN16; R56, R57 => RN17; R58, R59 => RN18; R60, R61=> RN19. And all use 0 ohm.
5. Page 24. Swap net of CN10-12 and CN10-13. Wrong connection.
6. Page 25. Change USB power source from 5VPCU to +5VSUS. Wrong design.
7. Page 30. Reserve R617 (stuff), R618 (stuff), C859 (NA), C869 (NA), C861 (NA) and C862 (NA). For noise in EZ4's LINE-IN.

06/23 MODIFY LIST

8. Page 23. Delete R36 and R76. VESDchange PWR source from LAN_3V to 3V_LAN directly.
9. Page 23. Delete R40 from TCK.
10. Page 23. Delete R42 from Q9-B and Q9-C.
11. Page 23. Add option resisters in 3VLAN. Add R56 and R57 for BCM4401.
12. Page 23. Add PI-filiter for AVDD and separate from VDDP. Add L72.
13. Page 23. Add PI-filiter for AVDDL. Add L73 and C863.
14. Page 23. BOM modification. Correct RDAC's resister from 1.18K to 1.24K (BCM5788).
15. Page 23. BOM modification. R70: stuff; R68: NA. FAE: Support CLKRUN#.

	R51, R 8	R56, R57	R38	R97, R87	Q5, Q9	U7	U8
BCM5788M	S UFF	NA	1.2 K	S UFF	S UFF	S UFF	NA
BCM 01	NA	S UFF	1.27K	NA	NA	NA	S UFF
NOTE	3VRUN	3V_LAN	RDAC			AT93C 6	2 LC128

06/28 MODIFY LIST

16. Page 28. Delete R112 (pull hign/ 10K) and Add R624 (0 ohm) to GND. BOM.
17. Page 28. Add R625 and R626 to GND. ALPS setting. BOM.
18. Page 28. Add R619, R620, R621 and R623 for bypass 3D function. BOM.
19. Page 28. Reserve R624, R622, C864 and U62. Those are for 3D function.

06/28 MODIFY LIST

20. Page 13. Update and correct U27 and U28 footprint. Correct DQS and DQM.
21. Page 13. Re-route MDA[0..63] QSA[0..7] and -DQMA[0..7]
22. Page 9. C272 change from CH73301M8B9 to CH747LM8801(LOW profile). BOM

B2 TEST CHANGE ITMES:

07/19 MODIFY LIST

23. Page 25. Change U32, U58 and U33 to AL000547001 (GMT).
    Change C489, C800 and C490 to CH71001M393 (100uF).
    Del R289, R296, R562, R555, R292 and R294
24. Page 25. Add USB PWR control (SUSON) circuit. Add R554 (10K) and Q39(DTC144EUA)
25. Page 42. Add Semtcech solution in Track-point.
    Add U63, U66, U65, U64, C866, C868, C867, C870, C872, C871, R637, R638, R643, R642, R645, R644, R647, R641, R646, R640, R639, R638.
26. Page 22. Chane CN13 from 4 in1 to 3 in 1. Re-routing it.
27. Page 28. BOM delete D4. Acer: no action in LID.

07/26 MODIFY LIST

28. Page 32. Add HOLE45 for MDC.
29. Page 32. Add HOLE46 for VRAM. (NO SPACE!!!)
30. Page 32. Add clip's PAD. P5, P6 and P7.

07/29 MODIFY LIST

31. Page 27. Add PULL HIGH 10K/ R649 to 3V. (EC)
32. Page 40. BOM: Remove PR149 and Stuff PR147. (EC)
33. Page 40. Delete PQ41. PU10, PC97, PC98 and PC99. REFP => VIN; REF3V => 3V_591. (EC and PWR)
    REFP in PD19-1 and PC130-1; REF3V in PU13-12, PR40-1, PR64-1 and PU14-5.
34. Page 40. Delete PR134 and PR139. Then SHORT them. (PWR)
35. Page 40. Change PQ52-3 from PU13-13(CC-SET) to PU13-8. And change PR87 from 0 ohm to 10K.(PWR)
36. Page 28. Upate CN7's footprint to 88264-06XX-6P-R
37. Page 28. Upate CN8's footprint to 88264-10XX-10P-R
38. Page 28. Upate CN3's footprint to 88264-04XX-4P-L
39. Page 39. Delete JP1. Change +1V5_S5 to +1.5V_S5.
40. Page 39. Delete JP2 and JP5. Change VCCP-OUT to +VCCP.
41. Page 31. Reserve and Stuff R650 and R651. For Fine-tune the value of headphone.

07/30 MODIFY LIST

41. Page 35. Disable NVVDD & +1.2V for INT VGA cost-down
42. Page 35. change R128 from 100K to 97.6Kohm, R127 from 34K to 100Kohm for power fine-tune VGA voltage
43. Page 42. Change trackpointer function from ALPS to SEMTECH
44. Page 12. Change EXT_BLON reistor R446 form 10K to 1K for boot white screen
45. Page 04. Disable R596 for Battery only can't boot

C TEST CHANGE ITMES:

08/9 MODIFY LIST

46. Page 26. Modify serial port function for EZ4 (MRXD1 & MTXD1)
47. Page 25. Change USB_Power_on voltage from +5VSUS to 5VPCU
48. Page 25. Modify all USB power switch OC# pull-up 10k to +3VSUS

08/10 MODIFY LIST

49. Page 26. Add GND in C577 & C578 for FIR
50. Page 33. Remove LAN's reserve capacitors(C817/C513/C542/C546/C554/C555/C525/C523/C533/C530) by EMI engineer confirm

08/11 MODIFY LIST

51. Page 36. CPU CORE Power(PU11's pin25) add another CAP 0.022UF(C170) by power engineer request
52. Page 23. Add two new CAP 0.1UF(C873 & C874) for AVDD_LAN & +1.8V_1.2V_LAN by EMI request

08/12 MODIFY LIST

53. Page 23. Change R38 from 1.24k to 1.18k for LAN droop & template
54. Page 17. Change L59/L60/L61 from FBM-10-160808-470(47ohm) to BLM18BA220(22ohm) for EA measure fail
55. Page 28. Modify Bluetooth led can't light for FOXCONN Bluetooth module (Add R652 & R653)
56. Page 31. Modify Line-in noise change R650 &R651 from 0ohm to 1kohm
    Page 30. Modify Line-in noise add C859 &C861 (0.1UF)
57. Page 31. Add AND gate(U67) & R654(0 ohm) for popo sound (delete D29 & D30 & R550)
58. Page 31. Add MOSFET (Q48&Q49) for headphone popo sound, and reserve Q46/Q47 for speaker popo sound issue
59. Page 33. Change L33/L34/L36 from 22ohm BEAD to short

08/13 MODIFY LIST

60. Page 26. Change R449 from 1k ohm to 4.7k ohm for SIO

08/18 MODIFY LIST

61. Page 17. Change R399/R400/R401/R387/R388/R390 size from 0402 to 0603 for EMI request
62. Page 31. Add Q50 & R656(10K) for Normal close type audio jack issue (Reserve)
63. Page 32. Change Q13 from Transistor to MOS and R110 (47k to 10k) & C139(0.22U to 0.1U) and add R657 (0R) from EC (154pin) for Lite_On ODD issue
64. Page 33. Add C875/C876/C877/C878 (12pf) for Docking DVI EMI issue(Reserve)

08/19 MODIFY LIST

65. Page 21. Change 1394 connecotor(CN28) type form SMD to DIP for SMT request
66. Page 28. Update CN7's footprint to 88264-06XX-6P-R-ZE1 & CN8's footprint to 88264-10XX-10P-R-ZE1 for SMT request (Increase PAD length 0.2mm)
67. Page 25. Update CN5's footprint to SM08B-SURS-8P-R-ZE1 for SMT request (Increase PAD length 0.2mm)
68. Page 41. Add new CAP(PC171/PC172) in BAT-V plane for EMI request
69. Page 23. Add new CAP(C879/C880) in AVDD_LAN plane for EMI request
70. Page 23. Add new CAP(C881/C882) in +3V plane for EMI request
71. Page 33. Change C1/C2 from TOP to BOT side for Mechanical request

06/27 LAYOUT SWAP

Pin 'JD M1.152' moved one 'R_B_MD 2'.
Pin 'JD M2.153' moved one 'R_A_MD 6'.
Pin 'JD M2.191' moved one 'R_A_MD5 '.
Pin 'JD M2.181' moved one 'R_A_MD 8'.
Pin 'JD M1.58' moved to me 'R_B_MD19'.
Pin 'JD M2.6' moved to me 'R_A_MD0'.
Pin 'JD M2.175' moved one 'R_A_MD61'.
Pin 'JD M2.16' moved to me 'R_A_MD6'.
Pin 'JD M2. ' moved to me 'R_A_MD16'.
Pin 'JD M2. 3' moved to me 'R_A_MD21'.
Pin 'JD M1.56' moved to me 'R_B_MD18'.
Pin 'JD M2.15 ' moved one 'R_A_MD 2'.
Pin 'JD M1.57' moved to me 'R_B_MD22'.
Pin 'JD M2.192' moved one 'R_A_MD51'.
Pin 'JD M1.176' moved one 'R_B_MD51'.
Pin 'JD M2.179' moved one 'R_A_MD 9'.
Pin 'JD M1.19 ' moved one 'R_B_MD59'.
Pin 'JD M1.192' moved one 'R_B_MD58'.
Pin 'JD M2.186' moved one 'R_A_DQS#6'.
Pin 'JD M1.5' moved to me 'R_B_MD 3'.
Pin 'JD M2.7' moved to me 'R_A_MD5'.
Pin 'JD M2.167' moved one 'R_A_DQS#7'.
Pin 'JD M2.152' moved one 'R_A_MD 3'.
Pin 'JD M1.7' moved to me 'R_B_MD5'.
Pin 'JD M2.157' moved one 'R_A_MD57'.
Pin 'JD M2.20' moved to me 'R_A_MD13'.
Pin 'JD M1.158' moved one 'R_B_MD 8'.
Pin 'JD M2.159' moved one 'R_A_MD60'.
Pin 'JD M2.173' moved one 'R_A_MD56'.
Pin 'JD M1.191' moved one 'R_B_MD62'.
Pin 'JD M2.5' moved to me 'R_A_MD1'.
Pin 'JD M1.61' moved to me 'R_B_MD29'.
Pin 'JD M2.170' moved one 'R_A_DM7'.
Pin 'JD M2.57' moved to me 'R_A_MD22'.
Pin 'JD M1.15 ' moved one 'R_B_MD 3'.
Pin 'JD M2.188' moved one 'R_A_DQS6'.
Pin 'JD M1.62' moved to me 'R_B_MD2 '.
Pin 'JD M2.61' moved to me 'R_A_MD29'.
Pin 'JD M1.182' moved one 'R_B_MD57'.
Pin 'JD M1.153' moved one 'R_B_MD 6'.
Pin 'JD M1.151' moved one 'R_B_MD 7'.
Pin 'JD M1.126' moved one 'R_B_MD32'.
Pin 'JD M1.157' moved one 'R_B_MD52'.
Pin 'JD M1.180' moved one 'R_B_MD56'.
Pin 'JD M1.175' moved one 'R_B_MD55'.
Pin 'JD M2.17' moved to me 'R_A_MD3'.
Pin 'JD M1. ' moved to me 'R_B_MD0'.
Pin 'JD M2.169' moved one 'R_A_DQS7'.
Pin 'JD M1.63' moved to me 'R_B_MD28'.
Pin 'JD M1.36' moved to me 'R_B_MD15'.
Pin 'JD M2.6 ' moved to me 'R_A_MD25'.
Pin 'JD M1.38' moved to me 'R_B_MD10'.
Pin 'JD M1.6 ' moved to me 'R_B_MD25'.
Pin 'RP ' moved to me 'R_B_MA '.
Pin 'RP6. ' moved to me 'SM_CS2#'.
Pin 'RP7 2' moved to me 'M_ODT2'.
Pin 'RP20.2' moved to me 'R_A_MA13'.
Pin 'RP6 2' moved to me 'R_B_SASA#'.
Pin 'RP28. ' moved to me 'R_A_BM#EA#'.
Pin 'RP2 .2' moved to me 'R_A_MA12'.
Pin 'RP20. ' moved to me 'M_ODT0'.
Pin 'RP .2' moved to me 'R_B_MA2'.
Pin 'RP7. ' moved to me 'R_B_MA13'.
Pin 'RP2. ' moved to me 'R_B_MA6'.
Pin 'RP2 2' moved to me 'CKE3'.
Pin 'RP2 . ' moved to me 'R_A_MA9'.
Pin 'RP3 2' moved to me 'R_B_MA7'.
Pin 'RP1 .2' moved to me 'R_B_MA12'.
Pin 'RP28.2' moved to me 'R_A_SCASA#'.
Pin 'RP1 . ' moved to me 'R_B_MA9'.
Pin 'JD M1.55' moved to me 'R_B_MD23'.
Pin 'JD M1. 5' moved to me 'R_B_MD20'.
Pin 'JD M2.180' moved one 'R_A_MD53'.
Pin 'JD M2.58' moved to me 'R_A_MD19'.
Pin 'JD M2.23' moved to me 'R_A_MD12'.
Pin 'JD M2.185' moved one 'R_A_DM6'.
Pin 'JD M1.35' moved to me 'R_B_MD1 '.
Pin 'JD M1.17 ' moved one 'R_B_MD50'.
Pin 'JD M2.63' moved to me 'R_A_MD28'.
Pin 'JD M2. 5' moved to me 'R_A_MD20'.
Pin 'JD M2.160' moved one 'R_A_MD63'.
Pin 'JD M1.179' moved one 'R_B_MD61'.
Pin 'JD M1. 3' moved to me 'R_B_MD21'.
Pin 'JD M2.182' moved one 'R_A_MD52'.
Pin 'JD M1.159' moved one 'R_B_MD53'.
Pin 'JD M2.151' moved one 'R_A_MD 7'.
Pin 'JD M2.158' moved one 'R_A_MD58'.
Pin 'JD M1.189' moved one 'R_B_MD63'.
Pin 'JD M1.6' moved to me 'R_B_MD1'.
Pin 'JD M2.1 ' moved to me 'R_A_MD2'.
Pin 'JD M1.173' moved one 'R_B_MD5 '.
Pin 'JD M2.62' moved to me 'R_A_MD2 '.
Pin 'JD M2.19 ' moved one 'R_A_MD50'.
Pin 'JD M1.160' moved one 'R_B_MD 9'.
Pin 'JD M1.181' moved one 'R_B_MD60'.
Pin 'JD M2. 6' moved to me 'R_A_MD17'.
Pin 'JD M1. ' moved to me 'R_B_MD16'.
Pin 'JD M2.189' moved one 'R_A_MD55'.
Pin 'JD M2.17 ' moved one 'R_A_MD62'.
Pin 'JD M1. 6' moved to me 'R_B_MD17'.
Pin 'JD M2.22' moved to me 'R_A_MD8'.
Pin 'JD M2.19' moved to me 'R_A_MD7'.
Pin 'JD M2.56' moved to me 'R_A_MD23'.
Pin 'JD M2.176' moved one 'R_A_MD59'.
Pin 'JD M1.123' moved one 'R_B_MD37'.

PROJECT ZE1
Quanta Computer Inc.

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		EDC
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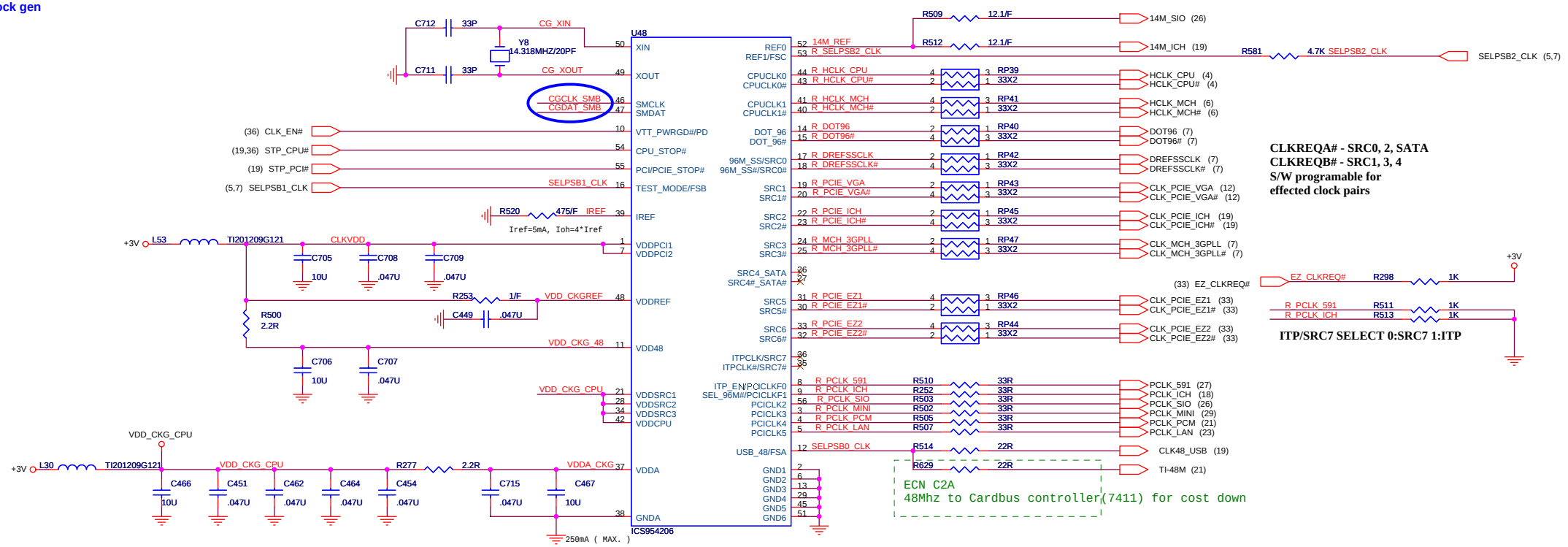
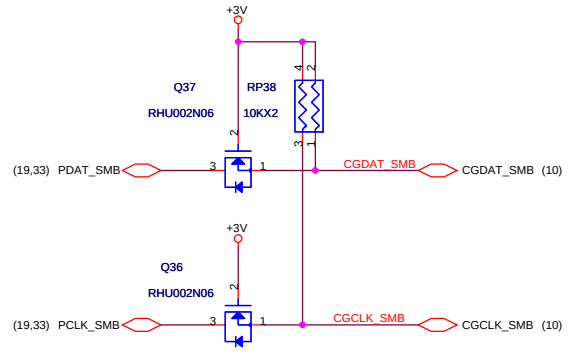
Clock gen



SM Bus

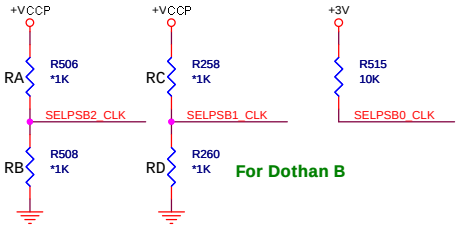


Speed setting

Resistor Stuff Table

	RA	RB	RC	RD
Dothan A 400	V	X	X	V
Dothan A 533	X	V	X	V
Dothan B	X	X	X	X

Default



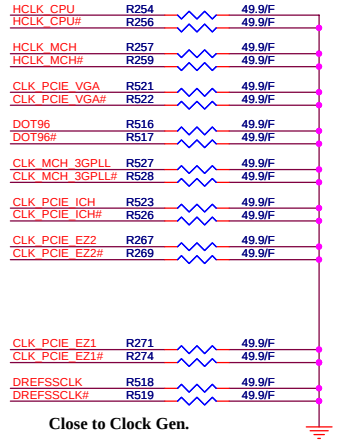
Clock Gen. Frequency Selection Table

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

DOTHAN BSEL Output Value

FSB Frequency	DOTHAN A-Step		DOTHAN B-Step	
	BSEL1	BSEL0	BSEL1	BSEL0
400 MHz	0	0	0	1
533 MHz	0	1	0	0

Clock terminator



Close to Clock Gen.

PROJECT : ZE1

Quanta Computer Inc.

Size	Document Number	Rev
	Clock Gen.	B2A
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CPU

U51A

Dothan

1 0F 3

(6) HA#[3..31] — HA#[3..31] — HA#3 P4 … HA#31 AF1 — A3# … A31# — REQUEST PHASE SIGNALS

(6) HADSTB0# U3 — (6) HADSTB1# AE5 — ADSTB0# ADSTB1#

(6) HREQ#0 R2 — (6) HREQ#1 P3 — (6) HREQ#2 T2 — (6) HREQ#3 P1 — (6) HREQ#4 T1 — REQ0# REQ1# REQ2# REQ3# REQ4#

(6) ADS# N2 — ADS# — ERROR SIGNALS

IERR# A4 — IERR#

(6) HBREQ0# N4 — (6) BPRI# J3 — (6) BNR# L1 — (6) HLOCK# J2 — BREQ0# BPRI# BNR# LOCK# — ARBITRATION PHASE SIGNALS

(6) HIT# K3 — (6) HITM# K4 — (6) DEFER# L4 — HIT# HITM# DEFER# — SNOOP PHASE SIGNALS

T200 T197 T111 T113 — BPM#0 C8 … BPM#3 C9 — BPM#0 … BPM#3 — RESPONSE PHASE SIGNALS

(6) HTRDY# M3 — (6) RS#0 H1 — (6) RS#1 K1 — (6) RS#2 L2 — TRDY# RS0# RS1# RS2#

(18) A20M# C2 — (18) FERR# D3 — (18) IGNNE# A3 — (18) CPUPWRGD E4 — (18) SMI# B4 — A20M# FERR# IGNNE# PWRGOOD SMI# — PC COMPATIBILITY SIGNALS

TCK A13 — TDO A12 — TDI C12 — TMS C11 — TRST# B13 — TCK TDO TDI TMS TRST# — DIAGNOSTIC & TEST SIGNALS

T196 T198 T112 T199 — ITP_CLK0 A16 — ITP_CLK1 A15 — PREQ# B10 — PRDY# A10 — DBR# A7 — (19) DBR# — ITP_CLK0 ITP_CLK1 PREQ# PRDY# DBR#

(18) INTR D1 — (18) NMI D4 — (18) STPCLK# C6 — (6,18) CPUSLP# A6 — (18) DPSLP# B7 — LINT0 LINT1 STPCLK# SLP# DPSLP# — EXECUTION CONTROL SIGNALS

(18) DPRSTP# G1 — DPRSTP#

THERMDA B18 — THERMDC A18 — THERMDA THERMDC

(7,18) THERMTRIP# — R596 *0R — THERMTRIP#_RR C17 — THERMTRIP#

PROCHOT# B17

VCCP — R499 56R — CPU_PROCHOT#

THERMAL DIODE

Dothan Processor

HD#[0..63] — HD#[0..63] (6) — D0# A19 HD#0 … D63# AF26 HD#63 — DATA PHASE SIGNALS

DSTBN0# C23 HDSTBN0# (6) … DSTBN3# AE25 HDSTBN3# (6)

DSTBP0# C22 HDSTBP0# (6) … DSTBP3# AE24 HDSTBP3# (6)

DINV0# D25 HDBI0# (6) … DINV3# AD20 HDBI3# (6)

DBSY# M2 DBSY# (6) — DRDY# H2 DRDY# (6)

BCLK1 B14 HCLK_CPU# (3) — BCLK0 B15 HCLK_CPU (3)

INIT# B5 CPUINIT# CPUINIT# (18)

RESET# B11 CPURST# CPURST# (6)

DPWR# C19 DPWR# (6)

G1 Pin:NC for Dothan and DPRSTP# for Yonah

ECN D2B For Battery only can't boot

EMI request

Thermal monitor

Q38 RHU002N06 — (12,27,41) MBCLK — THCLK_SMB

Q40 RHU002N06 — (12,27) MBDATA — THDAT_SMB

Q41 *RHU002N06 — (9) THERM_ALERT# — THERM_ALERT#_RR

3V — R549 10K — R553 10K — R575 10K — R566 100R — 280VCC — C799 .1U

U57 MAX6642ATT98-T — SCLK SDA ALERT# VCC DXF GND — THERMDA — C775 2200P — THERMDC

Address 1001 101

Power reset circuit

VCCP — R263 332/F — C453 .1U — Q25 MMBT3904 — 1999_SHT# — 1999_SHT# (37)

R610 330R THERMTRIP#

ITP debug

Default ITP Function Disabled

VCCP — R489 54.9/F — R494 *54.9/F — R491 39.2/F

TDI TMS TDO TRST# CPURST# TCK — JT7 JT2 JT4 JT3 JT1 JT6 — R493 *22.6/F — R490 *22.6/F

TCK NO STUB

R496 680R — R495 27.4/F

JT8 JT5 — VCCP 3V_S5 — C733 *.1U — R488 150/F — DBR#

JITP Connector Place these Components as close as possible.

Close to CPU

VCCP — TDI R492 150/F — IERR# R486 56R — CPUPWRGD R276 200/F

PROJECT : ZE1

Quanta Computer Inc.

Size	Document Number	Rev
	DOTHAN (HOST)	B2A
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CPU

Place pulldown resistors within 0.5" of COMP pins

Place voltage divider within 0.5" of GTLREF pin

U51B

Dothan 2 0F 3

POWER, GROUND, RESERVED SIGNALS

Dothan Processor

U51C

Dothan 3 0F 3

POWER, GROUND AND NC

VID

Dothan Processor

DOTHAN-A NC

DOTHAN-B POP

ECN C2A

Reserve for Power saving

CAP

PROJECT : ZE1

Quanta Computer Inc.

Size	Document Number	Rev
	DOTHAN (POWER & NC)	B2A
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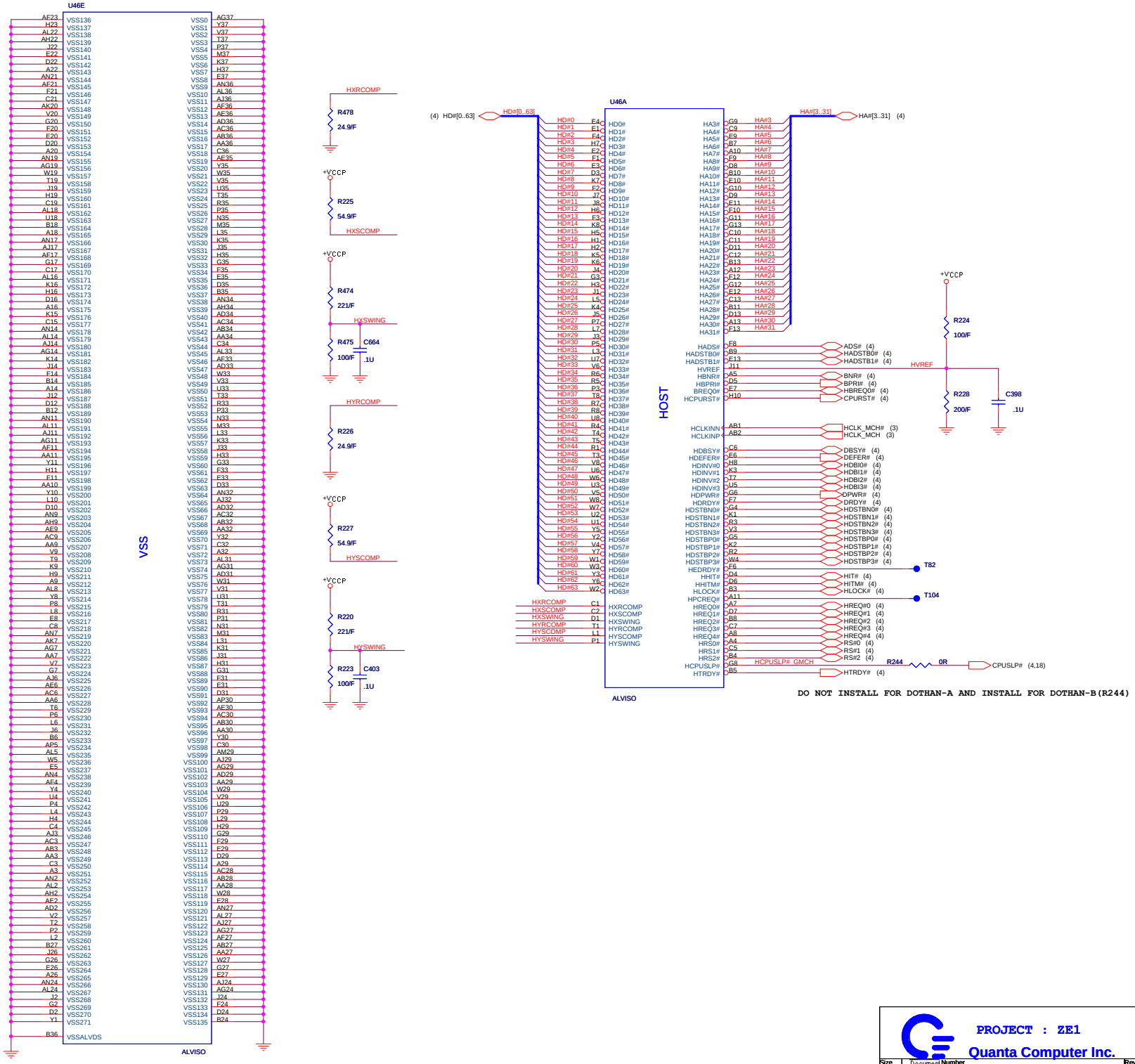

U46E
VSS
ALVISO
HXRCOMP
R478
24.9/F
+VCCP
R225
54.9/F
HXSCOMP
R474
221/F
HXSWING
R475
100/F
C664
.1U
HYRCOMP
R226
24.9/F
R227
54.9/F
HYSCOMP
R220
221/F
HYSWING
R223
100/F
C403
.1U
U46A
HOST
ALVISO
(4) HD#[0..63]
HD#[0..63]
HA#[3..31]
HA#[3..31] (4)
R224
100/F
R228
200/F
C398
.1U
HVREF
HADS# (4)
HADSTB0# (4)
HADSTB1# (4)
BNR# (4)
BPR# (4)
HBREQ0# (4)
CPURST# (4)
HCLK_MCH# (3)
HCLK_MCH (3)
DBSY# (4)
DEFER# (4)
HDBI0# (4)
HDBI1# (4)
HDBI2# (4)
HDBI3# (4)
DPWR# (4)
DRDY# (4)
HDSTBN0# (4)
HDSTBN1# (4)
HDSTBN2# (4)
HDSTBN3# (4)
HDSTBP0# (4)
HDSTBP1# (4)
HDSTBP2# (4)
HDSTBP3# (4)
T82
HIT# (4)
HITM# (4)
HLOCK# (4)
T104
HREQ#0 (4)
HREQ#1 (4)
HREQ#2 (4)
HREQ#3 (4)
HREQ#4 (4)
RS#0 (4)
RS#1 (4)
RS#2 (4)
HCPUSLP# GMCH
R244
0R
CPUSLP# (4,18)
HTRDY# (4)
DO NOT INSTALL FOR DOTHAN-A AND INSTALL FOR DOTHAN-B(R244)
PROJECT : ZE1
Quanta Computer Inc.
Size
Document Number
ALVISO A (HOST)
Rev
B2A
Date
Monday, August 22, 2005
Sheet 6 of 42

CFG[0:2]=100 FOR FSB 533
CFG[0:2]=101 FOR FSB 400

+VCCP

R231 4.7K

U46C

DMI
DDR MUXING
CFG/RSVD
PM
LCK
NC

(19) DMI_TXN0 AA31 DMIRXN0
(19) DMI_TXN1 AB35 DMIRXN1
(19) DMI_TXN2 AC31 DMIRXN2
(19) DMI_TXN3 AD35 DMIRXN3

(19) DMI_TXP0 Y31 DMIRXP0
(19) DMI_TXP1 AA35 DMIRXP1
(19) DMI_TXP2 AB31 DMIRXP2
(19) DMI_TXP3 AC35 DMIRXP3

(19) DMI_RXN0 AA33 DMITXN0
(19) DMI_RXN1 AB37 DMITXN1
(19) DMI_RXN2 AC33 DMITXN2
(19) DMI_RXN3 AD37 DMITXN3

(19) DMI_RXP0 Y33 DMITXP0
(19) DMI_RXP1 AA37 DMITXP1
(19) DMI_RXP2 AB33 DMITXP2
(19) DMI_RXP3 AC37 DMITXP3

(10) CLK_SDRAM0 AM33 SM_CK0
(10) CLK_SDRAM1 AL1 SM_CK1
T58 AE11 SM_CK2
(10) CLK_SDRAM3 AJ34 SM_CK3
(10) CLK_SDRAM4 AF6 SM_CK4
T65 AC10 SM_CK5

(10) CLK_SDRAM0# AN33 SM_CK0#
(10) CLK_SDRAM1# AK1 SM_CK1#
T59 AE10 SM_CK2#
(10) CLK_SDRAM3# AJ33 SM_CK3#
(10) CLK_SDRAM4# AF5 SM_CK4#
T64 AD10 SM_CK5#

(10,11) CKE0 AP21 SM_CKE0
(10,11) CKE1 AM21 SM_CKE1
(10,11) CKE2 AH21 SM_CKE2
(10,11) CKE3 AK21 SM_CKE3

(10,11) SM_CS0# AN16 SM_CS0#
(10,11) SM_CS1# AM14 SM_CS1#
(10,11) SM_CS2# AH15 SM_CS2#
(10,11) SM_CS3# AG16 SM_CS3#

M_OCDCOMP0 AF22 SM_OCDCOMP0
M_OCDCOMP1 AF16 SM_OCDCOMP1

(10,11) M_ODT0 AP14 SM_ODT0
(10,11) M_ODT1 AL15 SM_ODT1
(10,11) M_ODT2 AM11 SM_ODT2
(10,11) M_ODT3 AN10 SM_ODT3

M_RCOMPN AK10 SMRCOMPN
M_RCOMPP AK11 SMRCOMPP
SMVREF_MCH AE37 SMVREF0
AD1 SMVREF1
AE27 SMXSLEWIN
SMXSLEW AE28 SMXSLEWOUT
AF9 SMYSLEWIN
SMYSLEW AF10 SMYSLEWOUT

ALVISO

It's point to point, 55ohm trace, keep as short as possible.

CFG0 G16 CFG0
H13 CFG1
G14 CFG2
CFG3 F16 CFG3
CFG4 F15 CFG4
CFG5 G15 CFG5
CFG6 E16 CFG6
CFG7 D17 CFG7
CFG8 J16 CFG8
CFG9 D15 CFG9
CFG10 E15 CFG10
CFG11 D14 CFG11
CFG12 E14 CFG12
CFG13 H12 CFG13
CFG14 C14 CFG14
CFG15 H15 CFG15
CFG16 J15 CFG16
CFG17 H14 CFG17
CFG18 G22 CFG18
CFG19 G23 CFG19
CFG20 D23 CFG20
RSVD21 G25
RSVD22 G24
RSVD23 J17
RSVD24 A31
RSVD25 A30
RSVD26 D26
RSVD27 D25

R245 0R SELPSB1_CLK (3,5)
R246 0R SELPSB2_CLK (3,5)

R234 *1K
T85
R230 *1K
R237 1K

FOR DDR533
Low=DMIx2
High=DMIx4

R239 1K

FOR CPU533

R232 *INT@4.99K/F

INT VGA Staff

BM_BUSY# J23 PM_BMBUSY# (19)
EXT_TS0# J21 PM_EXTTS#0
EXT_TS1# H22 PM_EXTTS#1
THRMTRIP# F5 R255 0R THERMTRIP# (4,18)
PWROK AD30 IMVP_PWRGD_NB (19)
RSTIN# AE29 R183 100R PLTRST# (12,16,18,19,26,27,32,33)

DREF_CLKN A24 DOT96# DOT96# (3)
DREF_CLKP A23 DOT96 DOT96 (3)
DREF_SSCLKN C37 DREFSSCLK# DREFSSCLK# (3)
DREF_SSCLKP D37 DREFSSCLK DREFSSCLK (3)

NC1 AP37 TP_NC1 T144
NC2 AN37 TP_NC2 T143
NC3 AP36 TP_NC3 T137
NC4 AP2 TP_NC4 T147
NC5 AP1 TP_NC5 T141
NC6 AN1 TP_NC6 T139
NC7 B1 TP_NC7 T184
NC8 A2 TP_NC8 T187
NC9 B37 TP_NC9 T185
NC10 A36 TP_NC10 T190
NC11 A37 TP_NC11 T188

INT VGA Staff
R483 *INT@150/F INT_TV_C/R
R480 *INT@150/F INT_TV_COMP
R481 *INT@150/F INT_TV_Y/G
R484 *INT@150/F INT_VGA_RED
R485 *INT@150/F INT_VGA_GRN
R482 *INT@150/F INT_VGA_BLU

(12,15,28) DISP_ON DISP_ON R233 *INT@0R INT_DISP_ON
(12,28) BLON BLON R235 *INT@0R INT_BLON
R236 *INT@100K

R207 *40.2/F
R206 *40.2/F

+2.5V
R241 10K PM_EXTTS#0
R240 10K PM_EXTTS#1

Route as short as possible.

+1.8VSUS
R196 80.6/F
M_RCOMPN
M_RCOMPP
R203 80.6/F
Place Close to MCH

+1.8VSUS
R180 10K/F
SMVREF_MCH
R205 10K/F
C336 .1U
C325 2.2U

(28) TXLCLKOUT+ TXLCLKOUT+ RN13 2 4 1 3 *INT@0X2 INT_TXLCLKOUT+
(28) TXLCLKOUT- TXLCLKOUT- INT_TXLCLKOUT-
(28) TXLOUT0+ TXLOUT0+ RN14 4 2 3 1 *INT@0X2 INT_TXLOUT0+
(28) TXLOUT0- TXLOUT0- INT_TXLOUT0-
(28) TXLOUT1- TXLOUT1- RN15 2 4 1 3 *INT@0X2 INT_TXLOUT1-
(28) TXLOUT1+ TXLOUT1+ INT_TXLOUT1+
(28) TXLOUT2+ TXLOUT2+ RN12 2 4 1 3 *INT@0X2 INT_TXLOUT2+
(28) TXLOUT2- TXLOUT2- INT_TXLOUT2-

EXT VGA Staff(Place back RN12/RN13/RN14/RN15)

RN3 3 1 4 2 EXT@0X2 EXT_TXLCLKOUT- EXT_TXLCLKOUT- (12)
EXT_TXLCLKOUT+ EXT_TXLCLKOUT+ (12)
RN2 3 1 4 2 EXT@0X2 EXT_TXLOUT0+ EXT_TXLOUT0+ (12)
EXT_TXLOUT0- (12)
RN1 1 3 2 4 EXT@0X2 EXT_TXLOUT1- EXT_TXLOUT1- (12)
EXT_TXLOUT1+ (12)
RN4 3 1 4 2 EXT@0X2 EXT_TXLOUT2- EXT_TXLOUT2- (12)
EXT_TXLOUT2+ (12)

U46F

MISC
SDVOCTRL_DATA
SDVOCTRL_CLK
GCLKN
GCLKP

(16) SDVO_CTRLDATA H24
(16) SDVO_CTRLCLK H25
(3) CLK_MCH_3GPLL# AB29
(3) CLK_MCH_3GPLL AC29

TV
TVDAC_A
TVDAC_B
TVDAC_C
TV_REFSET
TV_IRTNA
TV_IRTNB
TV_IRTNC

(17) INT_TV_COMP INT_TV_COMP A15
(17) INT_TV_Y/G INT_TV_Y/G C16
(17) INT_TV_C/R INT_TV_C/R A17
TV_REFSET J18
B15
B16
B17

VGA
DDCCLK
DDCDATA
BLUE
BLUE#
GREEN
GREEN#
RED
RED#
VSYNC
HSYNC
REFSET

(17) INT_DDCCLK INT_DDCCLK E24
(17) INT_DDCDAT INT_DDCDAT E23
(17) INT_VGA_BLU INT_VGA_BLU F21
D21
(17) INT_VGA_GRN INT_VGA_GRN C20
B20
(17) INT_VGA_RED INT_VGA_RED A19
B19
(17) INT_VSYNC INT_VSYNC H21
(17) INT_HSYNC INT_HSYNC G21
J20

INT VGA Staff
R229 *INT@255/F REFSET
R242 *INT@1.5K/F

LVDS
LBKLT_CTRL
LBKLT_EN
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LVDD_EN
LIBG
LVBG
LVREFH
LVREFL

T91 INT_BLON E25
T92 F25
T95 C23
C22
(28) I_EDIDCLK F22
(28) I_EDIDDATA F26
INT_DISP_ON C33
T100 C31
T83 F28
T84 F27

INT_TXLCLKOUT- B30
INT_TXLCLKOUT+ B29
T96 C25
T99 C24

LACLKN
LACLKP
LBCLKN
LBCLKP

INT_TXLOUT0- B34
INT_TXLOUT1- B33
INT_TXLOUT2- B32

LADATAN0
LADATAN1
LADATAN2

INT_TXLOUT0+ A34
INT_TXLOUT1+ A33
INT_TXLOUT2+ B31

LADATAP0
LADATAP1
LADATAP2

T79 C29
T88 D28
T94 C27

LBDATAN0
LBDATAN1
LBDATAN2

T106 C28
T77 D27
T90 C26

LBDATAP0
LBDATAP1
LBDATAP2

ALVISO

PCI-EXPRESS GRAPHICS

GMCHEXP_TXP[15..0] (12)
GMCHEXP_TXN[15..0] (12)
GMCHEXP_RXP[15..0] (12,16)
GMCHEXP_RXN[15..0] (12,16)

VCC3G_PCIE
R219 24.9/F

EXP_COMPI D36
EXP_ICOMPO D34

EXP_RXN0 F30 GMCHEXP_RXN0
EXP_RXN1 F34 GMCHEXP_RXN1
EXP_RXN2 G30 GMCHEXP_RXN2
EXP_RXN3 H34 GMCHEXP_RXN3
EXP_RXN4 J30 GMCHEXP_RXN4
EXP_RXN5 K34 GMCHEXP_RXN5
EXP_RXN6 L30 GMCHEXP_RXN6
EXP_RXN7 M34 GMCHEXP_RXN7
EXP_RXN8 N30 GMCHEXP_RXN8
EXP_RXN9 P34 GMCHEXP_RXN9
EXP_RXN10 R30 GMCHEXP_RXN10
EXP_RXN11 T34 GMCHEXP_RXN11
EXP_RXN12 U30 GMCHEXP_RXN12
EXP_RXN13 V34 GMCHEXP_RXN13
EXP_RXN14 W30 GMCHEXP_RXN14
EXP_RXN15 Y34 GMCHEXP_RXN15

EXP_RXP0 D30 GMCHEXP_RXP0
EXP_RXP1 E34 GMCHEXP_RXP1
EXP_RXP2 F30 GMCHEXP_RXP2
EXP_RXP3 G34 GMCHEXP_RXP3
EXP_RXP4 H30 GMCHEXP_RXP4
EXP_RXP5 J34 GMCHEXP_RXP5
EXP_RXP6 K30 GMCHEXP_RXP6
EXP_RXP7 L34 GMCHEXP_RXP7
EXP_RXP8 M30 GMCHEXP_RXP8
EXP_RXP9 N34 GMCHEXP_RXP9
EXP_RXP10 P30 GMCHEXP_RXP10
EXP_RXP11 R34 GMCHEXP_RXP11
EXP_RXP12 T30 GMCHEXP_RXP12
EXP_RXP13 U34 GMCHEXP_RXP13
EXP_RXP14 V30 GMCHEXP_RXP14
EXP_RXP15 W34 GMCHEXP_RXP15

EXT VGA Staff

EXP_TXN0 E32 CGMCHEXP_TXN0 C681 EXT@1U GMCHEXP_TXN0
EXP_TXN1 F36 CGMCHEXP_TXN1 C667 EXT@1U GMCHEXP_TXN1
EXP_TXN2 G32 CGMCHEXP_TXN2 C673 EXT@1U GMCHEXP_TXN2
EXP_TXN3 H36 CGMCHEXP_TXN3 C659 EXT@1U GMCHEXP_TXN3
EXP_TXN4 J32 CGMCHEXP_TXN4 C417 EXT@1U GMCHEXP_TXN4
EXP_TXN5 K36 CGMCHEXP_TXN5 C653 EXT@1U GMCHEXP_TXN5
EXP_TXN6 L32 CGMCHEXP_TXN6 C411 EXT@1U GMCHEXP_TXN6
EXP_TXN7 M36 CGMCHEXP_TXN7 C643 EXT@1U GMCHEXP_TXN7
EXP_TXN8 N32 CGMCHEXP_TXN8 C405 EXT@1U GMCHEXP_TXN8
EXP_TXN9 P36 CGMCHEXP_TXN9 C625 EXT@1U GMCHEXP_TXN9
EXP_TXN10 R32 CGMCHEXP_TXN10 C602 EXT@1U GMCHEXP_TXN10
EXP_TXN11 T36 CGMCHEXP_TXN11 C613 EXT@1U GMCHEXP_TXN11
EXP_TXN12 U32 CGMCHEXP_TXN12 C632 EXT@1U GMCHEXP_TXN12
EXP_TXN13 V36 CGMCHEXP_TXN13 C606 EXT@1U GMCHEXP_TXN13
EXP_TXN14 W32 CGMCHEXP_TXN14 C608 EXT@1U GMCHEXP_TXN14
EXP_TXN15 Y36 CGMCHEXP_TXN15 C604 EXT@1U GMCHEXP_TXN15

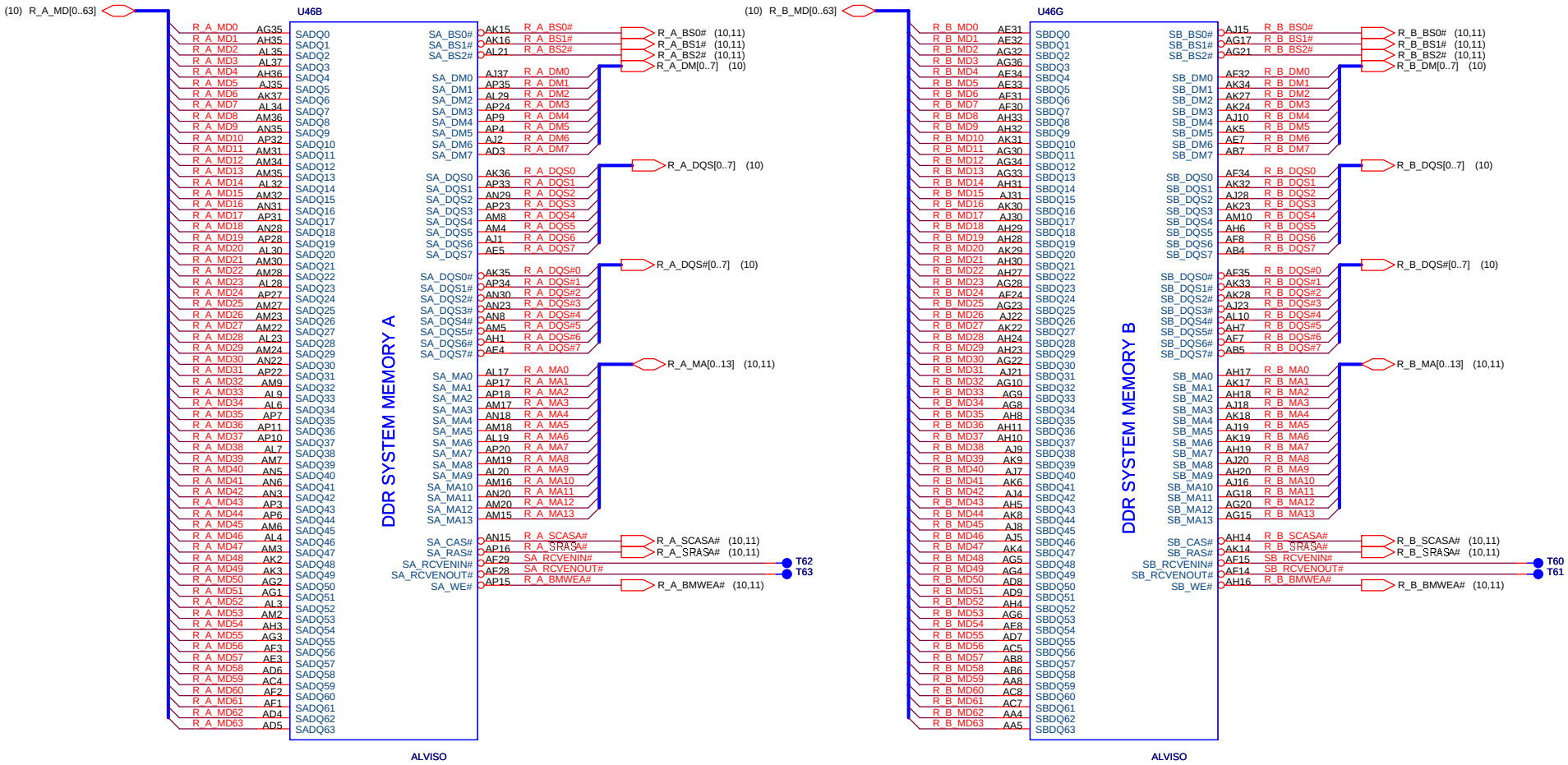
EXP_TXP0 D32 CGMCHEXP_TXP0 C683 EXT@1U GMCHEXP_TXP0
EXP_TXP1 E36 CGMCHEXP_TXP1 C671 EXT@1U GMCHEXP_TXP1
EXP_TXP2 F32 CGMCHEXP_TXP2 C675 EXT@1U GMCHEXP_TXP2
EXP_TXP3 G36 CGMCHEXP_TXP3 C662 EXT@1U GMCHEXP_TXP3
EXP_TXP4 H32 CGMCHEXP_TXP4 C422 EXT@1U GMCHEXP_TXP4
EXP_TXP5 J36 CGMCHEXP_TXP5 C657 EXT@1U GMCHEXP_TXP5
EXP_TXP6 K32 CGMCHEXP_TXP6 C413 EXT@1U GMCHEXP_TXP6
EXP_TXP7 L36 CGMCHEXP_TXP7 C641 EXT@1U GMCHEXP_TXP7
EXP_TXP8 M32 CGMCHEXP_TXP8 C408 EXT@1U GMCHEXP_TXP8
EXP_TXP9 N36 CGMCHEXP_TXP9 C626 EXT@1U GMCHEXP_TXP9
EXP_TXP10 P32 CGMCHEXP_TXP10 C601 EXT@1U GMCHEXP_TXP10
EXP_TXP11 R36 CGMCHEXP_TXP11 C612 EXT@1U GMCHEXP_TXP11
EXP_TXP12 T32 CGMCHEXP_TXP12 C631 EXT@1U GMCHEXP_TXP12
EXP_TXP13 U36 CGMCHEXP_TXP13 C605 EXT@1U GMCHEXP_TXP13
EXP_TXP14 V32 CGMCHEXP_TXP14 C607 EXT@1U GMCHEXP_TXP14
EXP_TXP15 W36 CGMCHEXP_TXP15 C603 EXT@1U GMCHEXP_TXP15

INT VGA Staff(Place back C681/C667/C673/C659/C683/C671/C675/C662)

CGMCHEXP_TXP0 C420 *INT@1U SDVOB_R+ SDVOB_R+ (16)
CGMCHEXP_TXN0 C418 *INT@1U SDVOB_R- SDVOB_R- (16)
CGMCHEXP_TXP1 C409 *INT@1U SDVOB_G+ SDVOB_G+ (16)
CGMCHEXP_TXN1 C406 *INT@1U SDVOB_G- SDVOB_G- (16)
CGMCHEXP_TXP2 C414 *INT@1U SDVOB_B+ SDVOB_B+ (16)
CGMCHEXP_TXN2 C412 *INT@1U SDVOB_B- SDVOB_B- (16)
CGMCHEXP_TXP3 C404 *INT@1U SDVOB_CLK+ SDVOB_CLK+ (16)
CGMCHEXP_TXN3 C399 *INT@1U SDVOB_CLK- SDVOB_CLK- (16)

PROJECT : ZE1
Quanta Computer Inc.

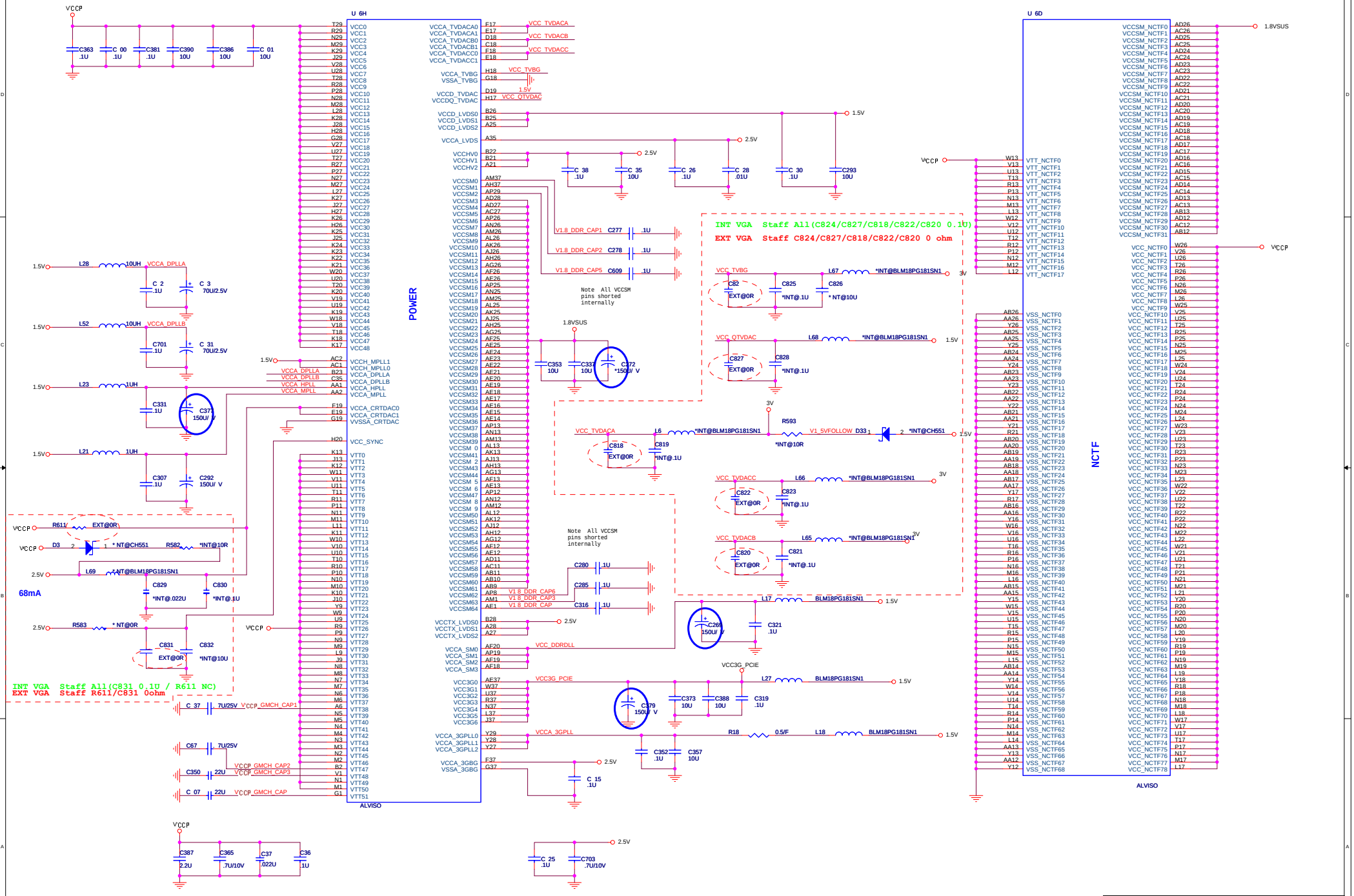
Size	Document Number	Rev
	ALVISO B (DMI & PCIE)	B2A
Date: Monday, August 22, 2005	Sheet 7 of 42	

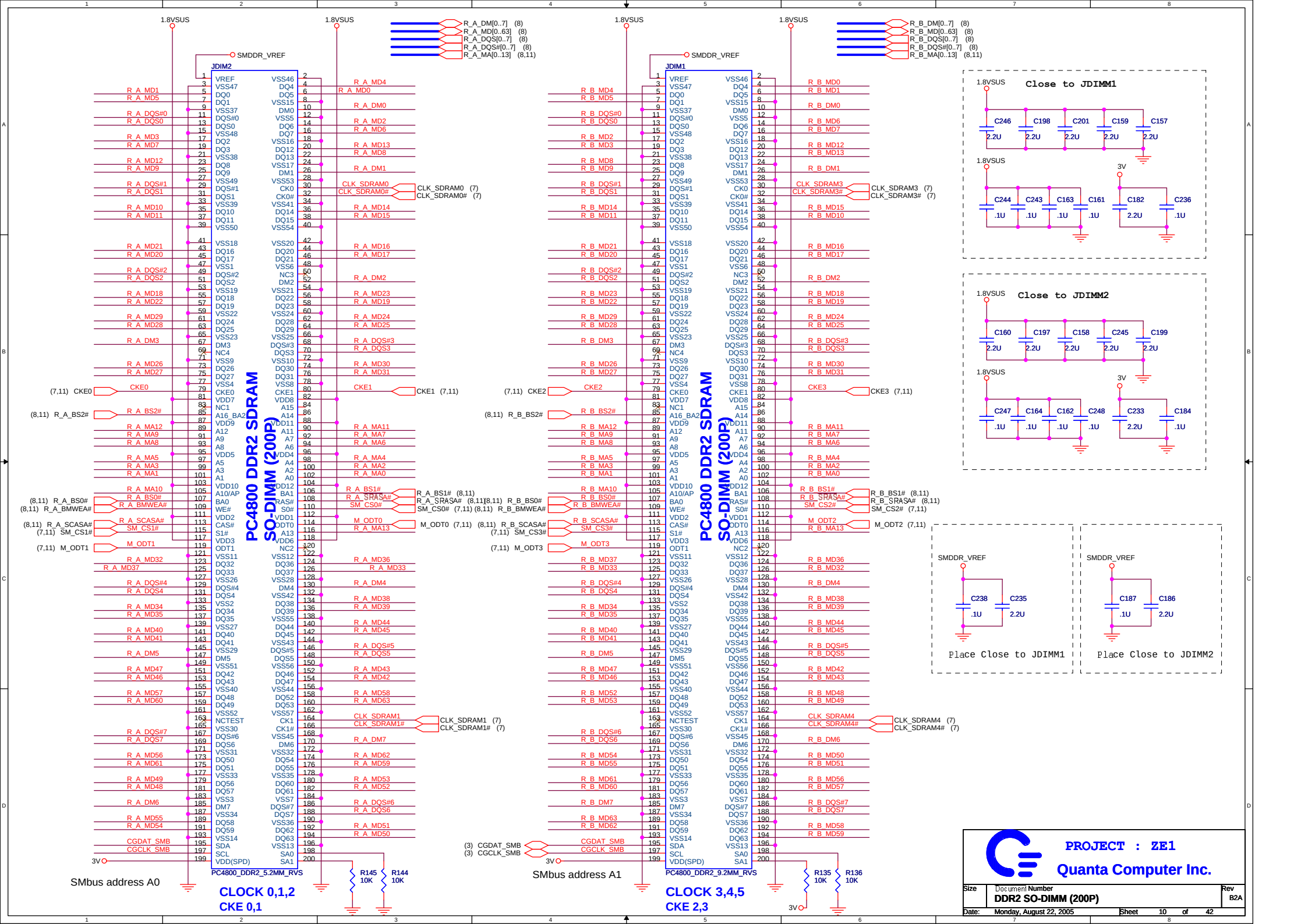


PROJECT : ZE1

Quanta Computer Inc.

Size	Document Number	Rev
	ALVISO_C (DDR2)	B2A
Date: Monday, August 22, 2005	Sheet 8 of 42	


U 6H
POWER
ALVISO
U 6D
NCTF
ALVISO
INT VGA Staff All(C824/C827/C818/C822/C820 0.1U)
EXT VGA Staff C824/C827/C818/C822/C820 0 ohm
INT VGA Staff All(C831 0.1U / R611 NC)
EXT VGA Staff R611/C831 0ohm
68mA
Note All VCCSM pins shorted internally
Note All VCCSM pins shorted internally
PROJECT : ZE1
Quanta Computer Inc.
ALVISO D (POWER)
Monday, August 22, 2005
Sheet 9 of 2


JDIM2
PC4800 DDR2 SDRAM
SO-DIMM (200P)
PC4800_DDR2_5.2MM_RVS
SMDDR_VREF
1.8VSUS
R_A_DM[0..7] (8)
R_A_MD[0..63] (8)
R_A_DQS[0..7] (8)
R_A_DQS#[0..7] (8)
R_A_MA[0..13] (8,11)
CLK_SDRAM0 (7)
CLK_SDRAM0# (7)
CLK_SDRAM1 (7)
CLK_SDRAM1# (7)
CKE0 (7,11)
CKE1 (7,11)
R_A_BS2# (8,11)
R_A_BS0# (8,11)
R_A_BMWEA# (8,11)
R_A_SCASA# (8,11)
SM_CS1# (7,11)
M_ODT1 (7,11)
M_ODT0 (7,11)
SM_CS0# (7,11)
R_A_SRASA# (8,11)
R_A_BS1# (8,11)
CGDAT_SMB (3)
CGCLK_SMB (3)
3V
R145 10K
R144 10K
SMbus address A0
CLOCK 0,1,2
CKE 0,1
JDIM1
PC4800_DDR2_9.2MM_RVS
R_B_DM[0..7] (8)
R_B_MD[0..63] (8)
R_B_DQS[0..7] (8)
R_B_DQS#[0..7] (8)
R_B_MA[0..13] (8,11)
CLK_SDRAM3 (7)
CLK_SDRAM3# (7)
CLK_SDRAM4 (7)
CLK_SDRAM4# (7)
CKE2 (7,11)
CKE3 (7,11)
R_B_BS2# (8,11)
R_B_BS0# (8,11)
R_B_BMWEA# (8,11)
R_B_SCASA# (8,11)
SM_CS3# (7,11)
M_ODT3 (7,11)
M_ODT2 (7,11)
SM_CS2# (7,11)
R_B_SRASA# (8,11)
R_B_BS1# (8,11)
R135 10K
R136 10K
SMbus address A1
CLOCK 3,4,5
CKE 2,3
Close to JDIMM1
C246 2.2U
C198 2.2U
C201 2.2U
C159 2.2U
C157 2.2U
C244 .1U
C243 .1U
C163 .1U
C161 .1U
C182 2.2U
C236 .1U
Close to JDIMM2
C160 2.2U
C197 2.2U
C158 2.2U
C245 2.2U
C199 2.2U
C247 .1U
C164 .1U
C162 .1U
C248 .1U
C233 2.2U
C184 .1U
C238 .1U
C235 2.2U
C187 .1U
C186 2.2U
Place Close to JDIMM1
Place Close to JDIMM2
PROJECT : ZE1
Quanta Computer Inc.
Size
Document Number
DDR2 SO-DIMM (200P)
Rev
B2A
Date: Monday, August 22, 2005
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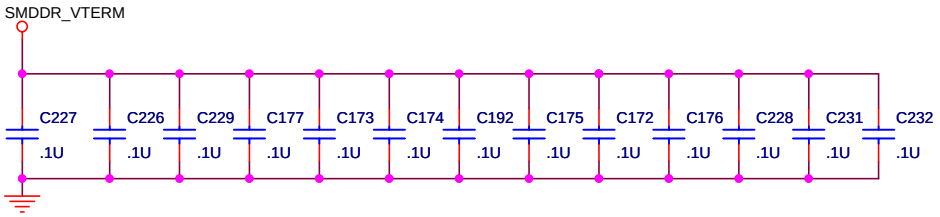
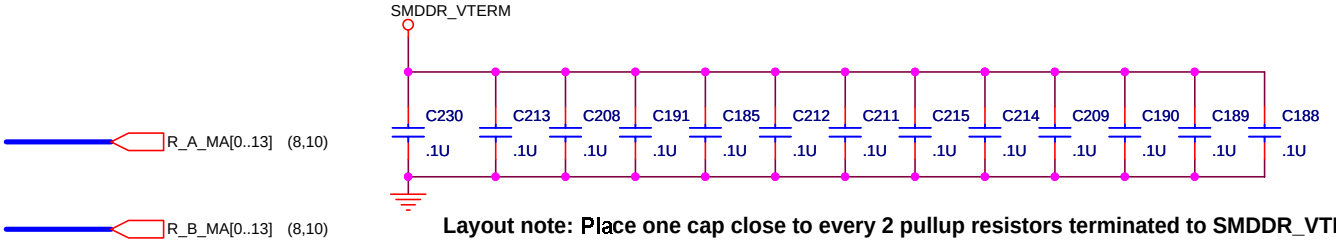
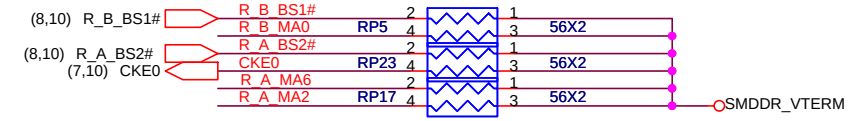
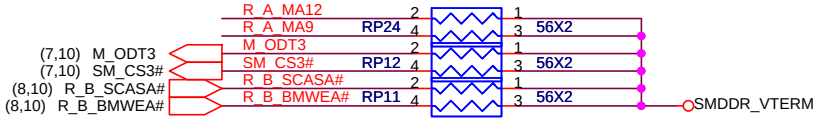


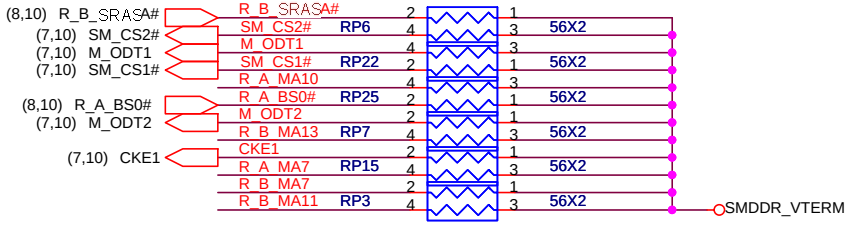
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

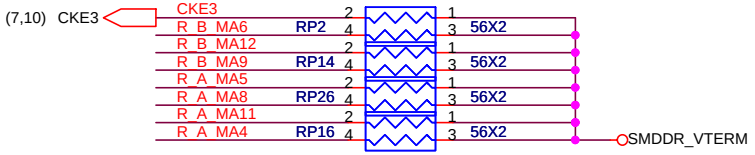


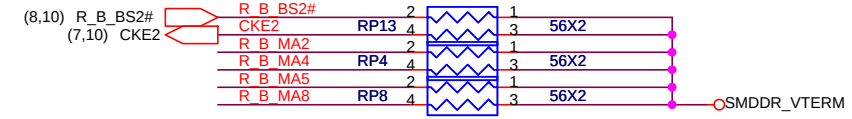
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

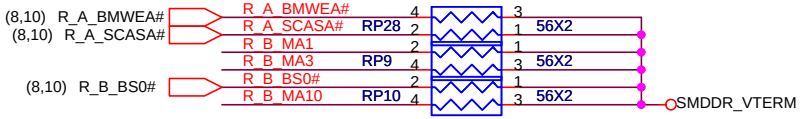


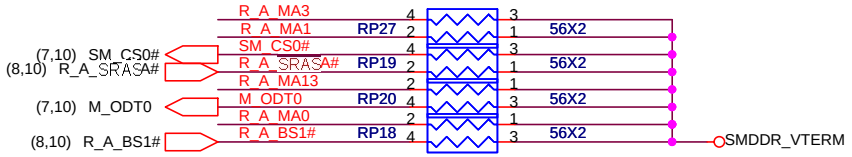












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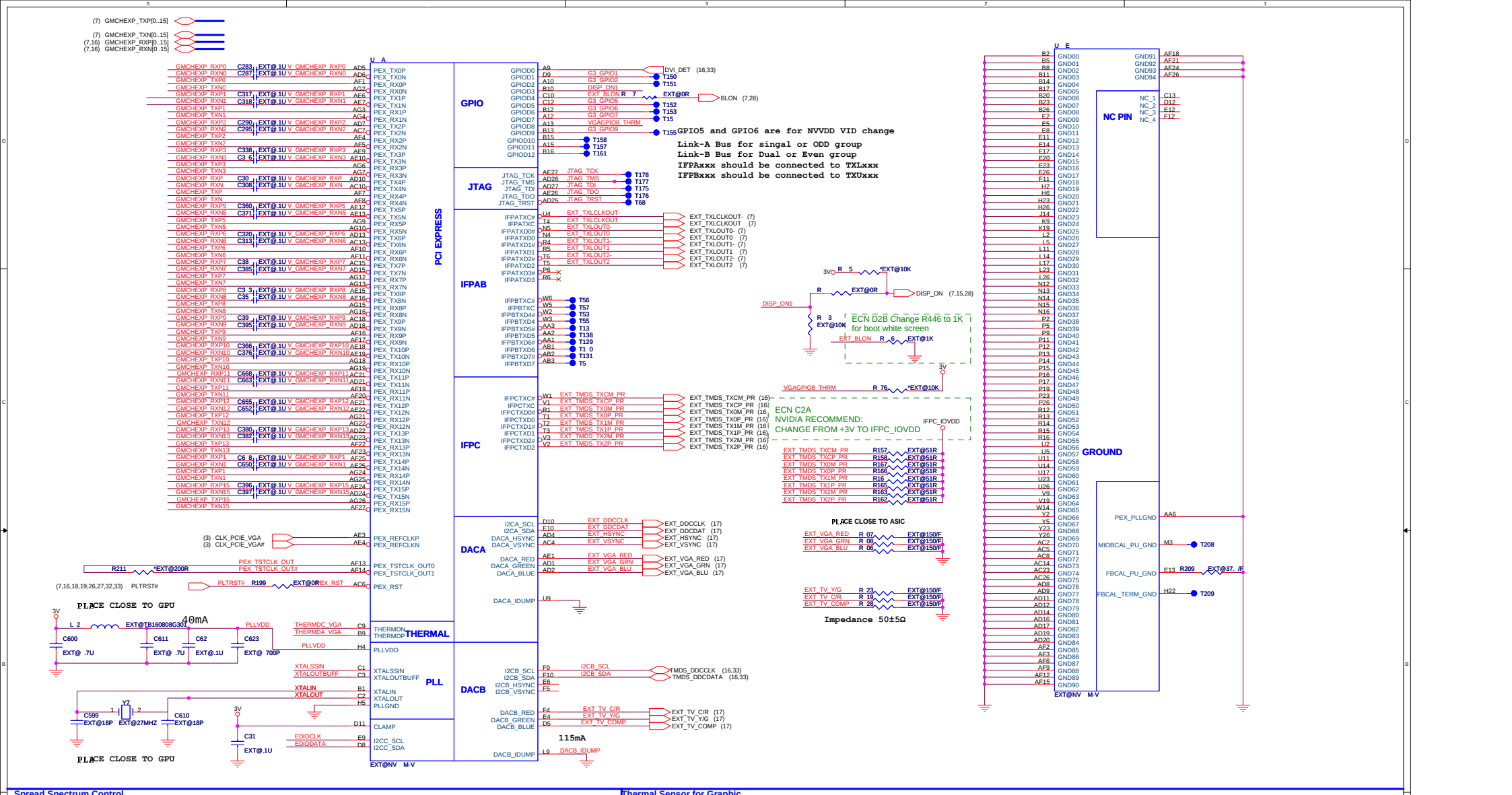
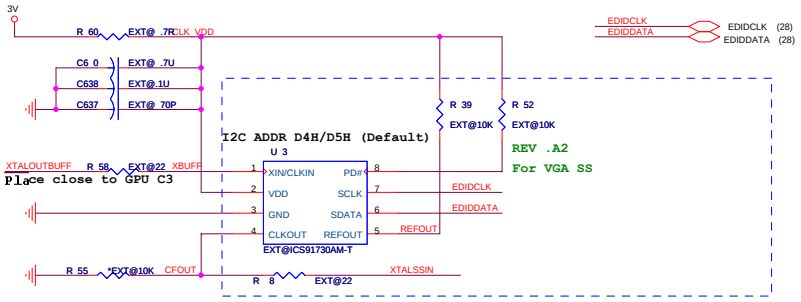
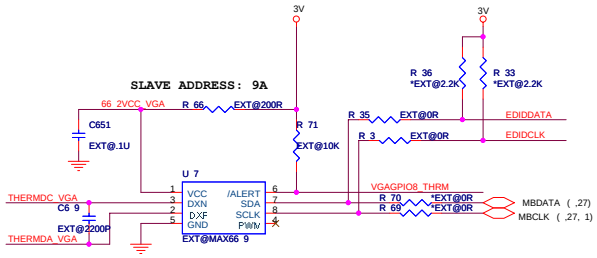


Spread Spectrum Control



Thermal Sensor for Graphic



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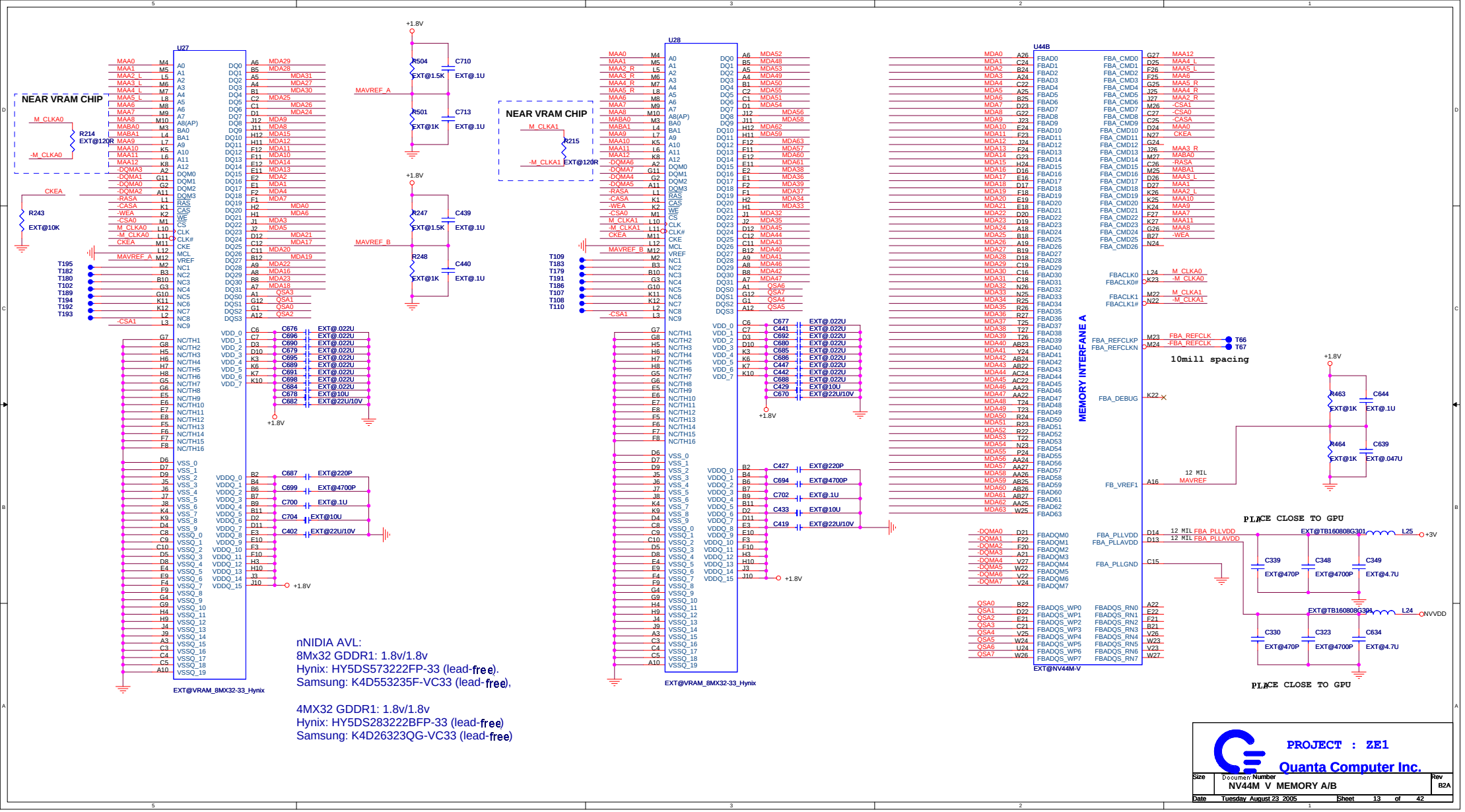

nNIDIA AVL:
8Mx32 GDDR1: 1.8v/1.8v
Hynix: HY5DS573222FP-33 (lead-free).
Samsung: K4D553235F-VC33 (lead-free),

4MX32 GDDR1: 1.8v/1.8v
Hynix: HY5DS283222BFP-33 (lead-free)
Samsung: K4D26323QG-VC33 (lead-free)

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AD23~PEX_IOVDD
280mA
AC16~PEX_IOVDDQ
1580mA

MEP43=1.05V/11.03A
MEP44(400/350)1.25V/9.02A

U44C

POWER

EXT@NV44M-V

PLACE NEAR BALLS

PLACE NEAR BGA

1580mA

180mA

20mA

PEX1V2

NVVDD

+1.2V

+1.8V

+3V

PEX_PLL_AVDD

PEX_PLL_DVDD

MIOB_VREF

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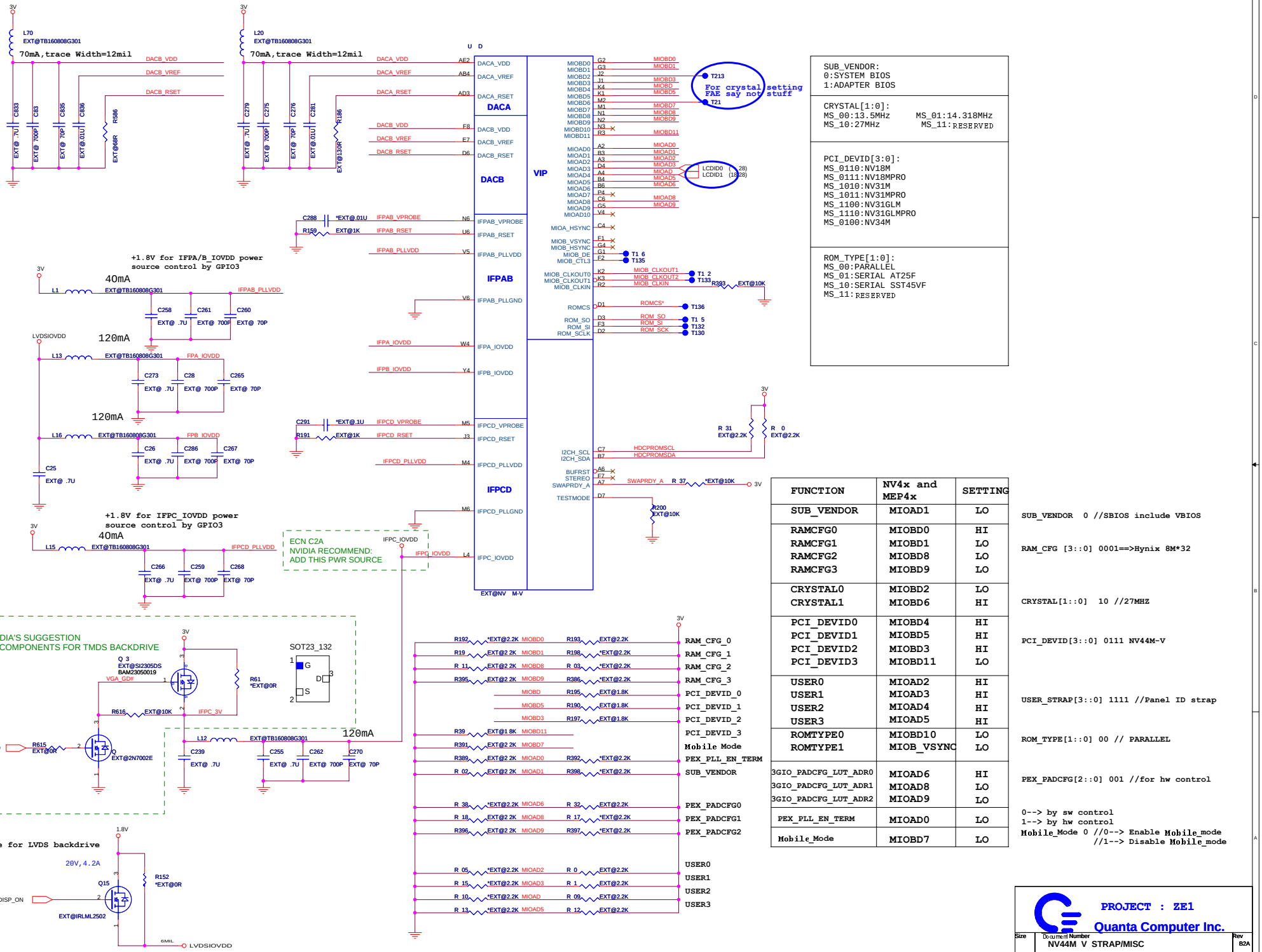

FUNCTION	NV4x and MEP4x	SETTING
SUB_VENDOR	MIOAD1	LO
RAMCFG0	MIOBD0	HI
RAMCFG1	MIOBD1	LO
RAMCFG2	MIOBD8	LO
RAMCFG3	MIOBD9	LO
CRYSTAL0	MIOBD2	LO
CRYSTAL1	MIOBD6	HI
PCI_DEVID0	MIOBD4	HI
PCI_DEVID1	MIOBD5	HI
PCI_DEVID2	MIOBD3	HI
PCI_DEVID3	MIOBD11	LO
USER0	MIOAD2	HI
USER1	MIOAD3	HI
USER2	MIOAD4	HI
USER3	MIOAD5	HI
ROMTYPE0	MIOBD10	LO
ROMTYPE1	MIOB_VSYNC	LO
3GIO_PADCFG_LUT_ADR0	MIOAD6	HI
3GIO_PADCFG_LUT_ADR1	MIOAD8	LO
3GIO_PADCFG_LUT_ADR2	MIOAD9	LO
PEX_PLL_EN_TERM	MIOAD0	LO
Mobile_Mode	MIOBD7	LO

```
SUB_VENDOR  0 //SBIOS include VBIOS

RAM_CFG [3::0] 0001==>Hynix 8M*32

CRYSTAL[1::0]  10 //27MHZ

PCI_DEVID[3::0] 0111 NV44M-V

USER_STRAP[3::0] 1111 //Panel ID strap

ROM_TYPE[1::0] 00 // PARALLEL

PEX_PADCFG[2::0] 001 //for hw control

0--> by sw control
1--> by hw control
Mobile_Mode 0 //0--> Enable Mobile_mode
              //1--> Disable Mobile_mode
```

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DVI control schematic(INT VGA USE)

INT VGA Staff

(7) SDVOB_R+
(7) SDVOB_R-
SDVOB_R+
SDVOB_R-
(7) SDVOB_G+
(7) SDVOB_G-
SDVOB_G+
SDVOB_G-
DVI_AVDD
(7) SDVOB_B+
(7) SDVOB_B-
SDVOB_B+
SDVOB_B-
(7) SDVOB_CLK+
(7) SDVOB_CLK-
SDVOB_CLK+
SDVOB_CLK-

DVI_AVDD

Always not, Reserve only

U4

+2.5V R90 *INT@10K R91 *100K

AVDD3 SDVOB_CLK- SDVOB_CLK+ AGND3 SDVOB_B- SDVOB_B+ AVDD2 SDVOB_G- SDVOB_G+ AGND2 SDVOB_R- SDVOB_R+

+3V L7 *INT@BLM11A601S DVI_AVDD_PLL
C83 *INT@.1U C111 *INT@10U
(7,12,18,19,26,27,32,33) PLTRST#
(7) SDVO_CTRLCLK
(7) SDVO_CTRLDATA
DVODATA
DVOCLK
(12,33) TMDS_DDCDATA
(12,33) TMDS_DDCCLK
+2.5V L3 *INT@BLM11A601S DVI_DVDD
C55 *INT@.1U C58 *INT@.1U C46 *INT@10U

1 AVDD_PLL
2 RESET*
3 AS
4 SPC
5 SPD
6 AGND_PLL
7 DGND1
8 SD_PROM
9 SC_PROM
10 SD_DDC
11 SC_DDC
12 DVDD1

36 AVDD1
35 SDVOB_STALL-
34 SDVOB_STALL+
33 SDVOB_INT-
32 SDVOB_INT+
31 AGND1
30 DGND2
29 HPDET
28 DVDD2
27 ATPG
26 SCEN
25 VSWING

INT- INT+
C85 *INT@.1U C70 *INT@.1U C84 *INT@.1U C77 *INT@10U
DVI_DET (12,33)
DVI_DVDD
R72 *INT@10K
R69 *INT@10K
R66 *INT@1.2K

DVI_AVDD L2 *INT@BLM11A601S +2.5V

13 TLC*
14 TLC
15 TVDD1
16 TDC0*
17 TDC0
18 TGND1
19 TDC1*
20 TDC1
21 TVDD2
22 TDC2*
23 TDC2
24 TGND2

*EXT@CH7307C-DE

DVI_TVDD L6 *INT@BLM11A601S +3V
C48 *INT@.1U C47 *INT@.1U C110 *INT@10U

DVI_CLK-
DVI_CLK+
DVI_TX0-
DVI_TX0+
DVI_TX1-
DVI_TX1+
DVI_TX2-
DVI_TX2+

Always not, Test only

U6

DVOCLK 6 SCL
DVODATA 5 SDA
A0 1
A1 2
A2 3
7 WP
VCC 8
GND 4
*AT24C16

+3V
C75 *1U

+3V R80 *1K DVOCLK
+3V R84 *1K DVODATA

ECN C2A
N-vidia sugges io
Del R584/R585

INT- C65 *INT@.01U/16V R584 *EXT@0R GMCHEXP_RXN1 (7,12)
INT+ C61 *INT@.01U/16V R585 *EXT@0R GMCHEXP_RXP1 (7,12)

+2.5V R89 *INT@1K SDVO_CTRLCLK

+2.5V R88 *INT@1K SDVO_CTRLDATA

PULL Low For DVO Not
Present(Internal PULL LOW In 915GM)

+2.5V 250mA
+3V 190mA

DVI Output select

ECN C2A
CAHGE FROM R TO RN

INT VGA Staff

DVI_CLK+ DVI_CLK- RN16 *INT@0X2 TMDS_TXCP_PR (33) TMDS_TXCM_PR (33)
DVI_TX0+ DVI_TX0- RN17 *INT@0X2 TMDS_TX0P_PR (33) TMDS_TX0M_PR (33)
DVI_TX1+ DVI_TX1- RN18 *INT@0X2 TMDS_TX1P_PR (33) TMDS_TX1M_PR (33)
DVI_TX2+ DVI_TX2- RN19 *INT@0X2 TMDS_TX2P_PR (33) TMDS_TX2M_PR (33)

EXT VGA Staff(Default)

(12) EXT_TMDS_TXCP_PR (12) EXT_TMDS_TXCM_PR RN5 EXT@0X2
(12) EXT_TMDS_TX0P_PR (12) EXT_TMDS_TX0M_PR RN8 EXT@0X2
(12) EXT_TMDS_TX1P_PR (12) EXT_TMDS_TX1M_PR RN7 EXT@0X2
(12) EXT_TMDS_TX2P_PR (12) EXT_TMDS_TX2M_PR RN6 EXT@0X2

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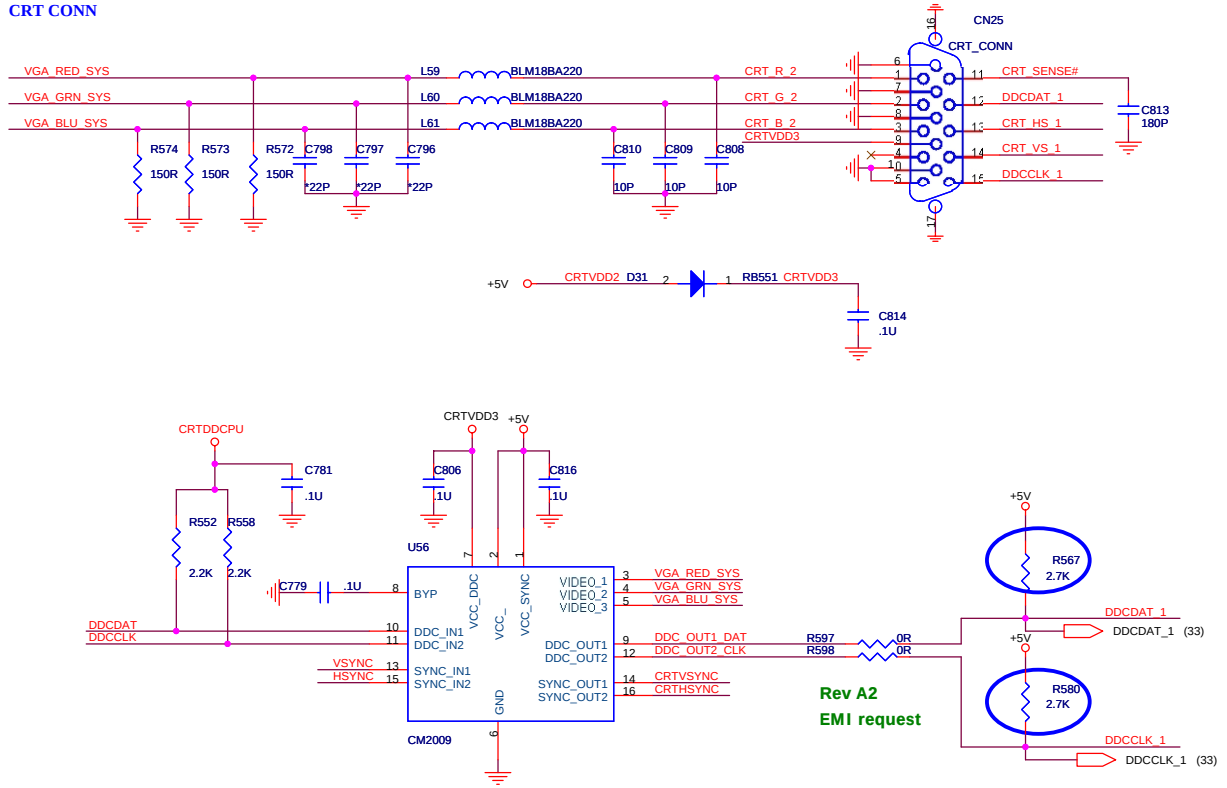
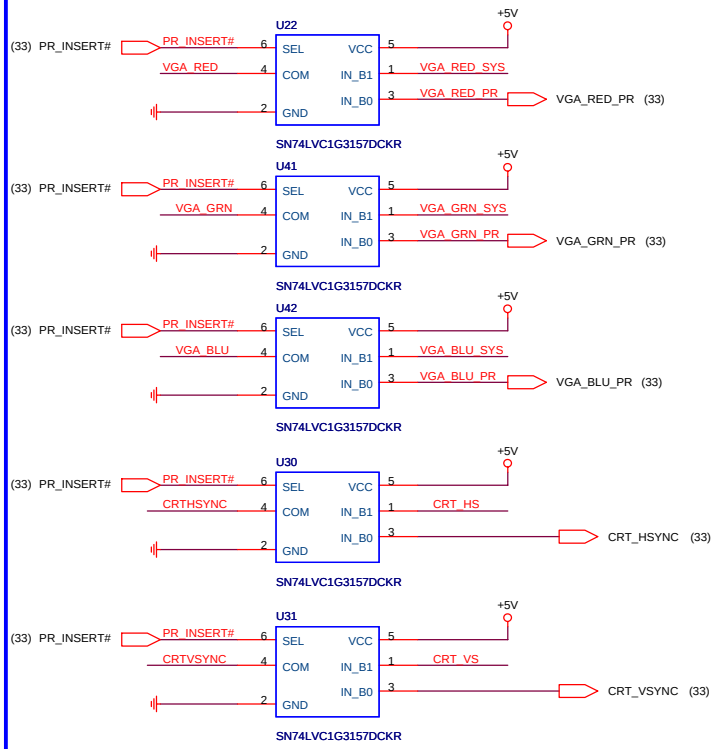
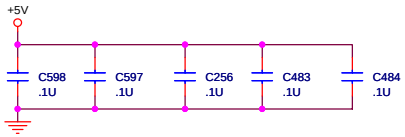
CRT CONN



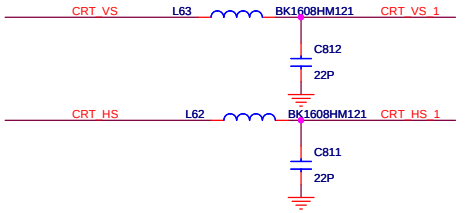
CRT Select

SWITCH CIRCUIT





Place each one capacitor for each one switch



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