Intel Agilex® 7 SoC FPGA Boot User Guide

Updated for Intel® Quartus® Prime Design Suite: **22.4**

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Contents

1. Introduction

This user guide describes the Intel Agilex® 7 SoC FPGA boot flow, boot sources, and how to generate a bitstream required for successful booting of the device. The details provided in this boot user guide include:

- The typical boot flows and boot stages of the Intel Agilex 7 SoC FPGA.
- The supported system layout for different hard processor system (HPS) boot modes.
- How to use Intel® Quartus® Prime Pro Edition to generate the configuration bitstream.

1.1. Glossary

Table 1. Intel Agilex 7 SoC FPGA Boot Glossary

Term	Definition
EMIF	External memory interface
`*.pof`	Programming object file; contains data to configure the FPGA portion of the SoC and additionally, may contain the HPS first-stage payload. This file is typically stored in external flash such as quad serial peripheral interface (Quad SPI) or common flash interface (CFI) flash.
FW	Firmware; Controls and monitors software stored in Secure Device Manager's (SDM) read-only memory.
HPS	Hard Processor System; the SoC portion of the device, consisting of a quad core Arm* Cortex*-A53 processor, hard IPs, and HPS I/Os in the Intel Agilex 7 SoC FPGA.
HPS EMIF I/O section	Part of the raw binary file (`*.rbf`) that configures the EMIF I/O used by the HPS
FPGA I/O section	Part of the `*.rbf` that configures the I/O assigned to the FPGA core
Core `*.rbf`	Core raw binary file; FPGA core image file that includes logic array blocks (LABs), digital signal processing (DSP), and embedded memory. The core image consists of a single reconfigurable region, or both static and reconfigurable regions.
FSBL	First-stage Bootloader for HPS
`*.jic`	JTAG Indirect Configuration file that allows programming through JTAG
OS	Operating system
`*.rbf`	Raw binary file representing the FPGA bitstream
`*.rpd`	Raw Programming Data file for AS devices

continued...

Term	Definition
`*.sof`	SRAM object file which contains the bitstream for the primary FPGA design. Firmware is not part of the `*.sof`.
SSBL	Second-stage Bootloader for HPS
SDM	Secure Device Manager; a triple-redundant processor-based block that manages FPGA configuration and hard processor system (HPS) secure boot process in Intel Agilex 7 devices.

1.2. Intel Agilex 7 SoC FPGA Boot Overview

The Intel Agilex 7 SoC FPGA combines an FPGA with a hard processor system (HPS) that is capable of booting Bare Metal applications or operating systems such as Linux*.

When booting the device from a power-on reset, you can choose between two different methods of booting:

- FPGA Configuration First Mode—When you select the FPGA First option, the SDM fully configures the FPGA, then configures the HPS SDRAM pins, loads the HPS first-stage bootloader (FSBL) and takes the HPS out of reset.

  Note: The FPGA and all of the I/Os are fully configured before the HPS is released from reset. Thus, when the HPS boots, the FPGA is in user mode and is ready to interact with the HPS. Optionally, the SDM can hold the HPS in reset until instructed by the user. To release the HPS from reset, you can use soft IP such as a mailbox client to send a mailbox request to the SDM.

- HPS Boot First Mode—When you select the HPS First option, the SDM first configures the HPS SDRAM pins, loads the HPS FSBL and takes the HPS out of reset. Then the HPS configures the FPGA I/O and FPGA fabric at a later time.

  Note: This mode is also referred to as Early I/O Release Mode or Early I/O Configuration. After power-on, the device configures a minimal amount of I/O required by the HPS before releasing the HPS from reset. This mode allows the HPS to boot quickly without having to wait for the full configuration to complete. Subsequently, the HPS may trigger an FPGA configuration request during the SSBL or OS stage.

2. FPGA Configuration First Mode

2.1. Boot Flow Overview for FPGA Configuration First Mode

You can program the Intel Agilex 7 SoC device to configure the FPGA first and then boot the HPS. The available configuration data sources configure the FPGA core and periphery first in this mode. After completion, you may optionally boot the HPS. All of the I/O, including the HPS-allocated I/O, are configured and brought out of tri-state. If the HPS is not booted:

- The HPS is held in reset.
- HPS-dedicated I/O are held in reset.
- HPS-allocated I/O are driven with reset values from the HPS.

If the FPGA is configured before the HPS boots, the boot flow looks like the example figure below. The flow includes the time from power-on-reset (T_{POR}) to boot completion ($T_{Boot\_Complete}$).

Figure 1. Typical FPGA Configuration First Boot Flow

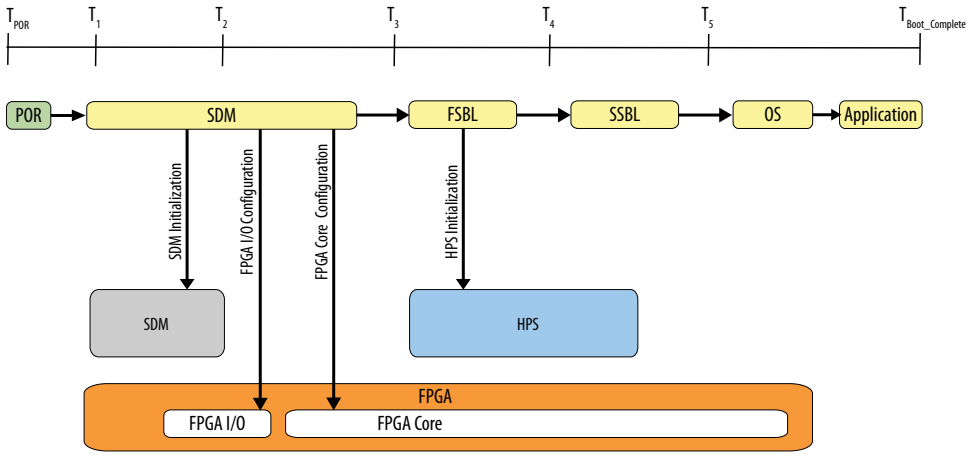


Table 2. FPGA Configuration First Stages

The sections following this table describe each stage in more detail.

Time	Boot Stage	Device State
T_{POR} to T_1	POR	Power-on reset
T_1 to T_2	Secure Device Manager (SDM)-Boot ROM	1. SDM samples the MSEL pins to determine the configuration scheme and boot source. 2. SDM establishes the device security level based on eFuse values. 3. SDM initializes the device by reading the configuration firmware (initial part of the bitstream) from the boot source. 4. SDM authenticates and decrypts the configuration firmware (this process occurs as necessary throughout the configuration). 5. SDM starts executing the configuration firmware.
T_2 to T_3	SDM- configuration firmware	1. SDM I/O are enabled. 2. SDM configures the FPGA I/O and core (full configuration) and enables the rest of your configured SDM I/O. 3. SDM loads the FSBL from the bitstream into HPS on-chip RAM. 4. SDM enables HPS SDRAM I/O and optionally enables HPS debug. 5. FPGA is in user mode. 6. HPS is released from reset. CPU1-CPU3 are in a wait-for-interrupt (WFI) state.
T_3 to T_4	First-Stage Bootloader (FSBL)	1. HPS verifies the FPGA is in user mode. 2. The FSBL initializes the HPS, including the SDRAM. 3. HPS loads SSBL into SDRAM. 4. HPS peripheral I/O pin mux and buffers are configured. Clocks, resets, and bridges are also configured. 5. HPS I/O peripherals are available.
T_4 to T_5	Second-Stage Bootloader (SSBL)	1. HPS bootstrap completes. 2. OS is loaded into SDRAM.
T_5 to $T_{Boot\_Complete}$	Operating System (OS)	The OS boots and applications are scheduled for runtime launch.

Related Information

System Layout for FPGA Configuration First Mode on page 9

2.1.1. Power-On Reset (POR)

Ensure you power each of the power rails according to the power sequencing consideration until they reach the required voltage levels. In addition, the power-up sequence must meet either the standard or the fast power-on reset (POR) delay time.

Related Information

- Intel Agilex 7 Device Data Sheet
  For information about the POR delay specification
- AN 692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria® 10, Intel Stratix® 10, and Intel Agilex 7 Devices

2.1.2. Secure Device Manager

Once the Intel Agilex 7 SoC FPGA exits POR, the SDM samples the MSEL[2:0] pins to determine the boot source. Next, the device configures the SDM I/Os according to the selected boot source interface and the SDM retrieves the configuration bitstream through the interface.

The typical configuration bitstream for FPGA configuration first contains:

1. Configuration firmware for the SDM
2. FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
3. FPGA core configuration data
4. HPS FSBL code and FSBL hardware handoff binary data

The SDM completes the configuration of the FPGA core and I/O, and then copies the HPS FSBL code and HPS FSBL hardware handoff binary to the HPS on-chip RAM.

Related Information

- System Layout for HPS Boot First Mode on page 18
- Intel Agilex 7 Configuration User Guide

2.1.3. First-Stage Bootloader

The first-stage bootloader (FSBL) is the first boot stage for the HPS. In FPGA Configuration First mode, the SDM extracts and loads the FSBL into the on-chip RAM of the HPS. The SDM releases the HPS from reset after the FPGA has entered user mode. After the HPS exits reset, it uses the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals. Typically, the FSBL then loads the SSBL into HPS SDRAM and passes control to the SSBL.

You can create the FSBL from one of the following sources:

- U-Boot secondary program loader (SPL)
  - Intel provides the source code for U-Boot on GitHub.
- Arm Trusted Firmware
  - Intel provides the source code for the Arm Trusted Firmware on GitHub.

Related Information

- Creating the Configuration Files on page 22
- U-Boot Source Code on GitHub
- Arm Trusted Firmware Source Code on GitHub

2.1.4. Second-Stage Bootloader

The second-stage bootloader (SSBL) is the second boot stage for the HPS. The FSBL initiates the copy of the SSBL to the HPS SDRAM. The SSBL typically enables more advanced peripherals such as Ethernet and supports command line interface.

You can create the SSBL from one of the following sources:

- U-Boot
  - Intel provides the source code for U-Boot on GitHub.
- UEFI
  - Intel provides the source code for UEFI on GitHub.
- RTOS
- Bare Metal application

Related Information

- UEFI Source Code on GitHub
- U-Boot Source Code on GitHub
- Arm Trusted Firmware Source Code on GitHub

2.1.5. Operating System

Typically, the SSBL loads the operating system (OS) stage into SDRAM. The OS executes from SDRAM. Depending on your application requirements, you may implement a conventional OS or an RTOS.

Intel provides the Golden System Reference Design (GSRD) which includes the Linux kernel and a root filesystem built with Yocto recipes.

Related Information

Golden System Reference Design and Design Examples on page 52

2.1.6. Application

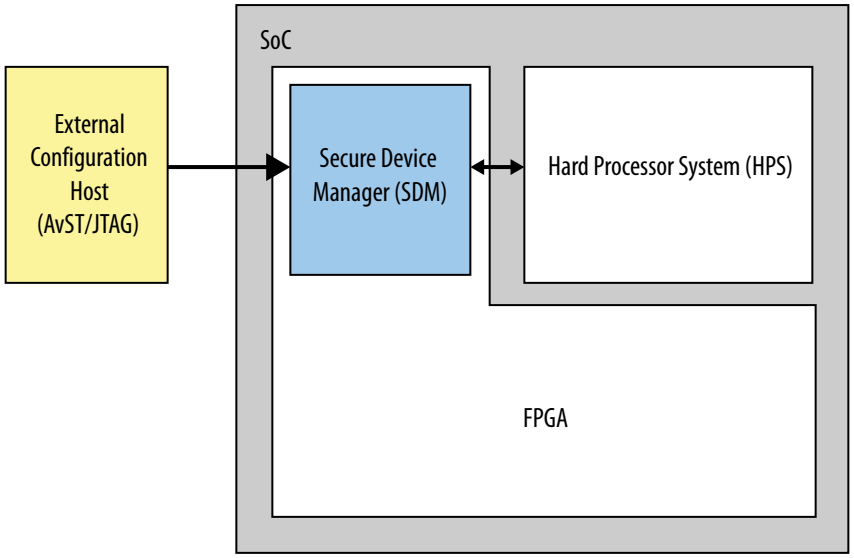
The application that runs on the OS is the last boot stage.

2.2. System Layout for FPGA Configuration First Mode

The following sections describe the supported system layout for FPGA Configuration First mode. The OS is assumed to be Linux in the following examples, but you may replace Linux with other supported operating systems.

2.2.1. External Configuration Host Only

Figure 2. External Configuration Host Only

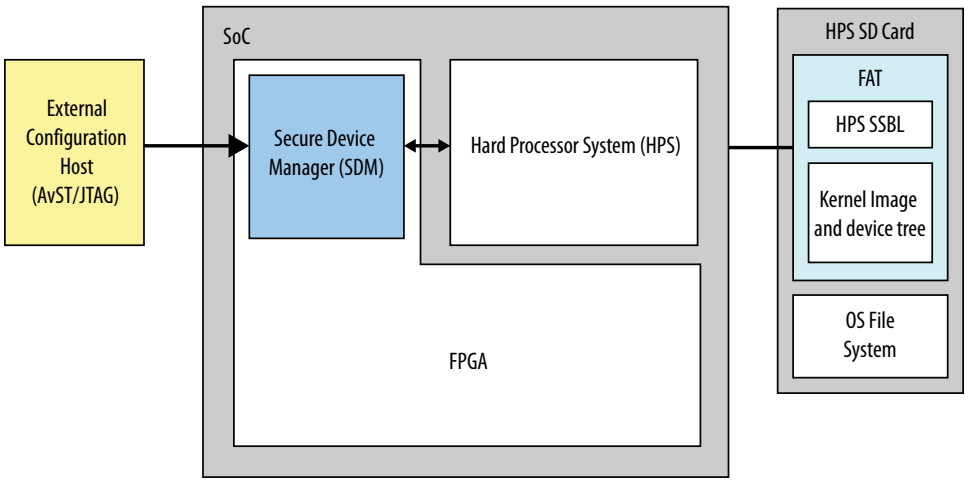


In this example, the external configuration host (Avalon® streaming or JTAG) provides the SDM with a configuration bitstream that consist of:

- SDM configuration firmware
- FPGA I/O and HPS EMIF I/O configuration data
- FPGA core configuration data
- HPS FSBL code and HPS FSBL hardware handoff binary

2.2.2. External Configuration Host with HPS Flash

Figure 3. External Configuration Host with HPS Flash



An external configuration host with HPS flash provides an SDM configuration bitstream containing:

- SDM configuration firmware
- FPGA I/O and HPS EMIF I/O configuration data
- FPGA core configuration data
- HPS FSBL code and HPS FSBL hardware handoff binary

In this system layout, you can use the HPS flash to store the HPS SSBL, Linux image device tree information and OS file system. This layout enables the device to boot into an OS such as Linux.

Table 3. Supported Configuration Boot Source and HPS Flash Combinations

SDM Configuration Host	HPS Flash
Avalon streaming	SD/MMC
JTAG	
Avalon streaming	NAND
JTAG	

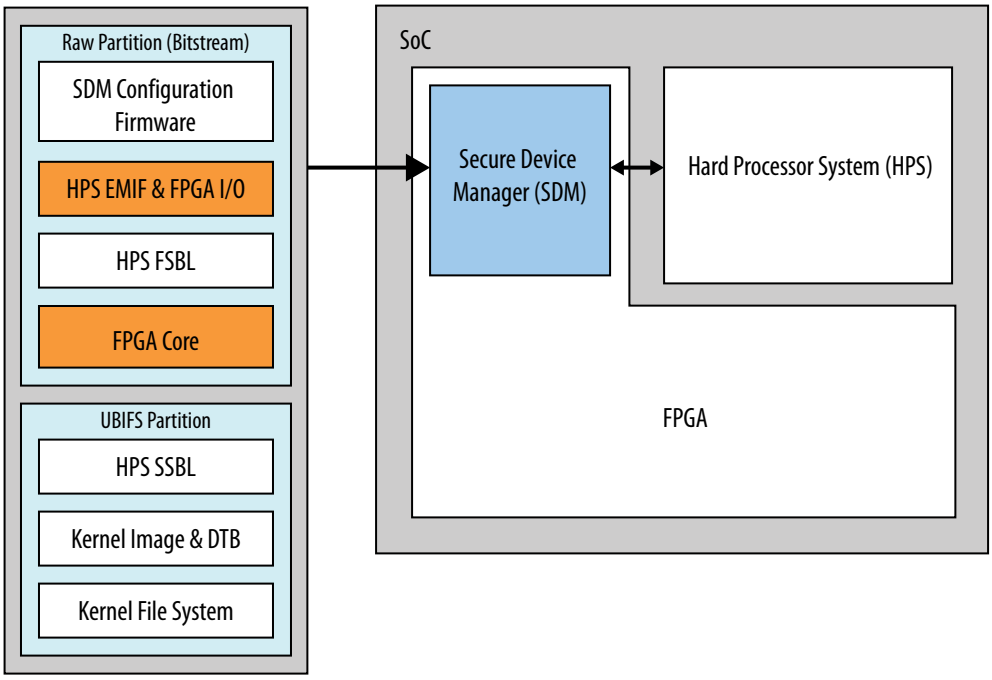
2.2.3. Single SDM Flash

In a single flash attached to SDM layout, the flash contains all of the files required for booting, including the configuration bitstream and OS files.

Software running on the HPS such as the FSBL must request permission from the SDM to access the flash attached to the SDM.

In the Quad SPI flash example, the SSBL, OS and file system reside in the Unsorted Block Image File System (UBIFS).

Figure 4. FPGA Configuration First Layout with Quad SPI



Related Information

- Intel Agilex 7 Hard Processor System Technical Reference Manual
  For more information, refer to the Booting and Configuration Appendix
- Intel Agilex 7 SoC FPGA First Single QSPI Flash Boot

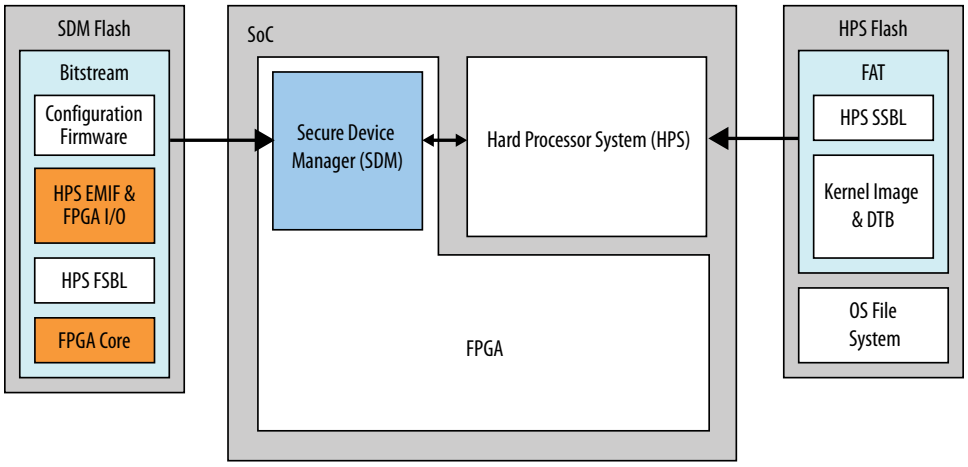
2.2.4. FPGA Configuration - First Dual Flash System

In a dual flash system, the SDM flash stores the configuration bitstream, while the HPS flash stores the HPS SSBL and the rest of the OS files.

Table 4. Dual Flash Combination (SDM and HPS)

SDM Flash Type	HPS Flash Type
Active serial/Quad SPI	SD/MMC
Active serial/Quad SPI	NAND

Figure 5. FPGA Configuration First - Dual Flash devices (SDM and HPS)



Related Information

- RocketBoards: Intel Agilex 7 SoC GSRD
- Golden System Reference Design and Design Examples on page 52