Computer Organization
Part – I
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Lecture – 6
Data path Architecture

In the previous lecture you got some idea about the control, that is, specifically data path control. Now in this lecture, we will take a look at the data path architecture. Let us go back a little and then see the highest level we have, the user point of view, the program; this goes through many levels.

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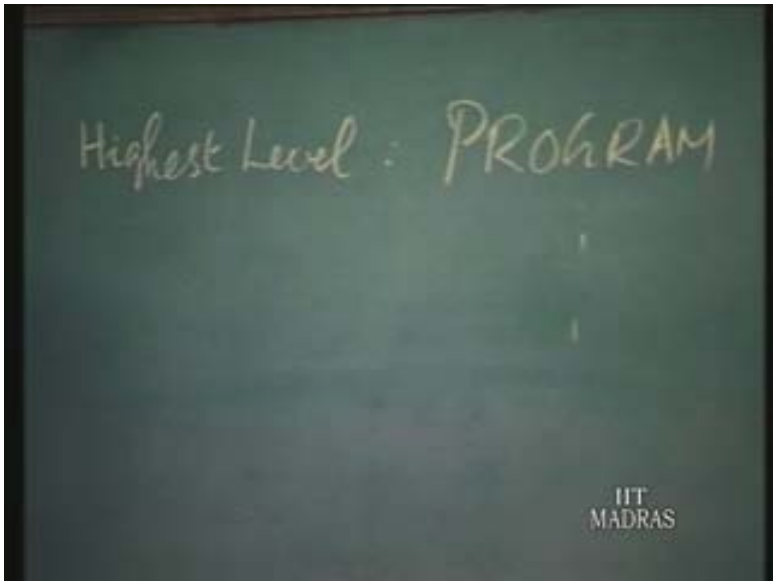

That is, we talk about codes and so on; and at the lowest level, we have the state information, that is, in each state there is a small activity, which we had identified as the registered transfer level activity. So while discussing this RTL activity, we saw that the sequence in which the register transfer actions must take place will be decided by the controller or the control signals, and the activity itself we saw that it consists of moving the data around some specified paths and controlling this.

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So it gave you some idea about these control aspects in the previous lecture. Now we will take a look at the data path part of it, for which we will assume a typical architecture. I hope you would recall we said earlier that architecture is different from organization. That is not precisely what we are talking about here. Here basically it means how you can put the various components together, so that whenever the processor needs, the controller will issue the appropriate signals so that the physical connections will be enabled so that the data will move around.

Now we will see more of it – as I said we must have some idea about the components involved in it. Some of what we knew already is what we had seen. First I said ALU or the arithmetic logic unit, which forms core of the processor. Then, while talking about the processor, we also came across this component, that is, the CPU consisting of registers; we saw some of these registers earlier. Basically it is the one which holds information on the CPU side. Now we will see some more components, after which I will discuss typical data path architecture.

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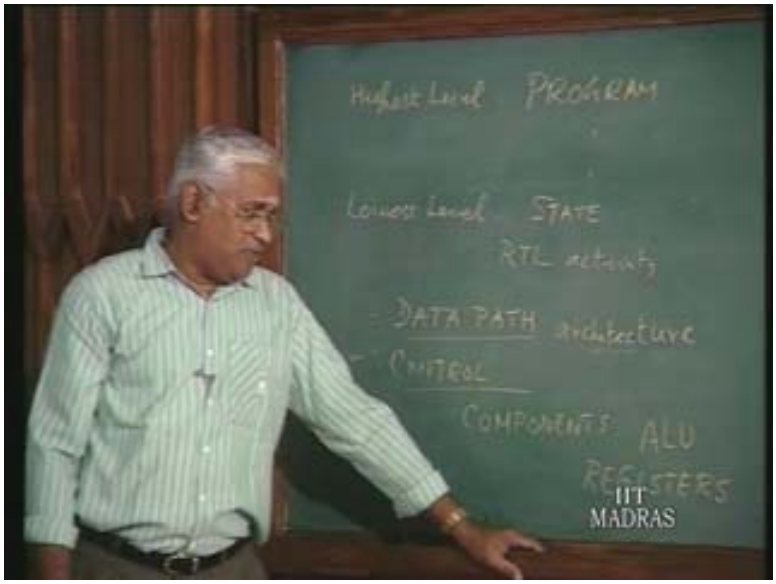

Today I will introduce one more thing; we will see more about ALU. Before that, I will talk about one component, which would be used in the architecture level for the data path; that is called multiplexer. What exactly is a multiplexer? It is sometimes simply referred to as a MUX. Essentially it has multiple inputs, which are called data inputs. They are more than one; it can be many. These are called the data inputs, and depending upon another set of inputs called control inputs, one of these will be output. So the output of the MUX is one of the data inputs – which one will be decided by the control input.

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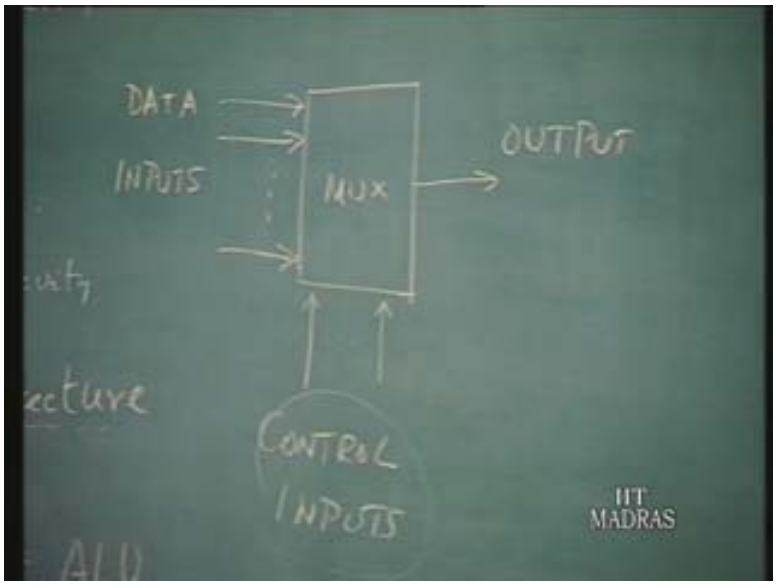

You can see parallel to what we are talking about earlier. We are talking about the path on which the data will move, and that particular path will be decided by a set of control signals. In fact you can see the summary of it even in the single component, that is, multiplexer. So multiplexer is what we will use; for instance, if the multiplexer has two inputs – I will be using a diagrammatic representation like this – that is, a MUX has two inputs called A and B. Sometimes we refer to this as A leg of the multiplexer and B leg of the multiplexer. Now one of these will be output – which one will be decided by a control input. It is easy to visualize. You can have more than one in which appropriately we must have the set of control signals, which uniquely identify them. Similarly, let us take a look at this ALU we have been talking about earlier. ALU is the arithmetic logic unit, that is, a unit which is capable of performing a set of arithmetic functions and a set of logic functions.

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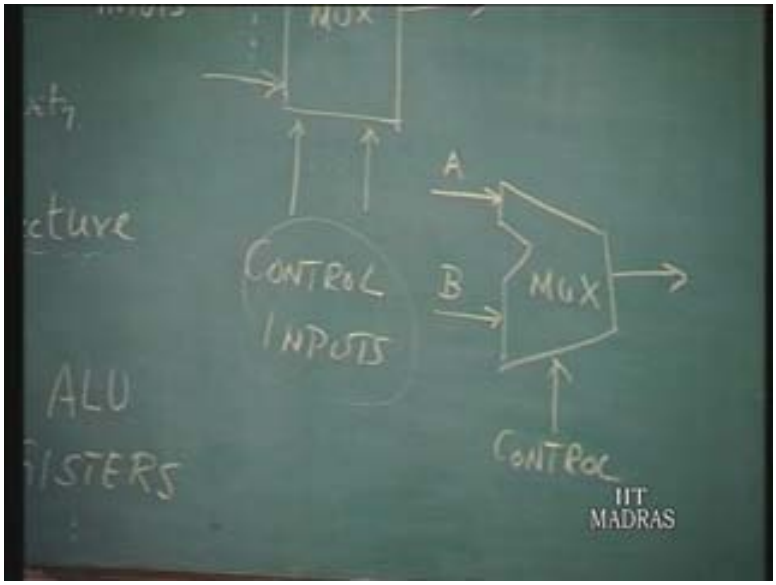

I will assume for a purpose that it is an ALU, which is capable of performing let us say 16 arithmetic functions. We will talk about a set of data and then it will be carrying out some functions – 16 arithmetic functions and, let us say, 16 logic functions, that is, the ALU is capable of executing 32 different functions. Now we have to assume a few other things like what is the data size of the ALU? We will assume again an ALU accepts two sets of inputs – what is the size of the data? In this particular one, I was just mentioning data input; we are not talking about the size.

In the case of ALU we have to talk about that too, because one of the arithmetic functions can be addition. When we talk about addition, we have to indicate whether it is a 4-bit addition or an 8-bit addition – 4 bit or 8 bit actually refers to the size of the data. Now suppose this were a 4-bit ALU, then precisely what we mean is the data input, which comes on the A leg, is going to be of 4-bit size, or is 4-bit wide. Similarly, the one on the B will also be 4-bit wide. If it were an 8-bit ALU then we will be having an 8-bit A input or an 8-bit B input.