H-tile Hard IP for Ethernet Intel® Stratix® 10 FPGA IP Design Example User Guide

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IP Version: **19.3.0**

Online Version
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Contents

1. Quick Start Guide

The H-Tile Hard IP for Ethernet Intel® FPGA IP core provides a simulation testbench and a hardware design example that supports compilation and hardware testing. When you generate the design example, the parameter editor automatically creates the files necessary to simulate, compile, and test the design in hardware.

In addition, you can download the compiled hardware design to the Intel Stratix® 10 MX FPGA Development Kit. Intel provides a compilation-only example project that you can use to quickly estimate IP core area and timing.

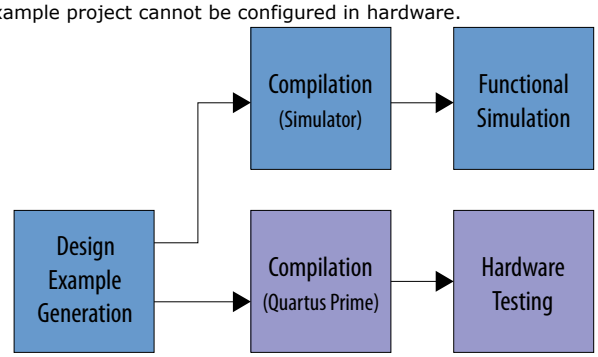
You can generate the design example H-Tile Hard IP for Ethernet Intel FPGA IP core variation:

- 100 Gbps MAC+PCS (supports simulation testbench, compilation-only example project, and hardware design example)
- 100 Gbps PCS only (supports simulation testbench and compilation-only example project, and hardware design example)
- 100 Gbps OTN (supports simulation testbench and compilation-only example project)
- 100 Gbps FlexE (supports simulation testbench and compilation-only example project)

Note: The H-Tile Hard IP for Ethernet Intel FPGA IP provides preliminary support for the OTN feature. For further inquiries, contact your nearest Intel sales representative or file an Intel Premier Support (IPS) case on https://www.intel.com/content/www/us/en/programmable/my-intel/mal-home.html.

Figure 1. Development Steps for the Design Example

Future releases of the IP core also provide a hardware design example you can compile and test in hardware. The compilation-only example project cannot be configured in hardware.



Related Information

- H-Tile Hard IP for Ethernet Intel FPGA IP User Guide
  For detailed information on H-tile Hard IP.

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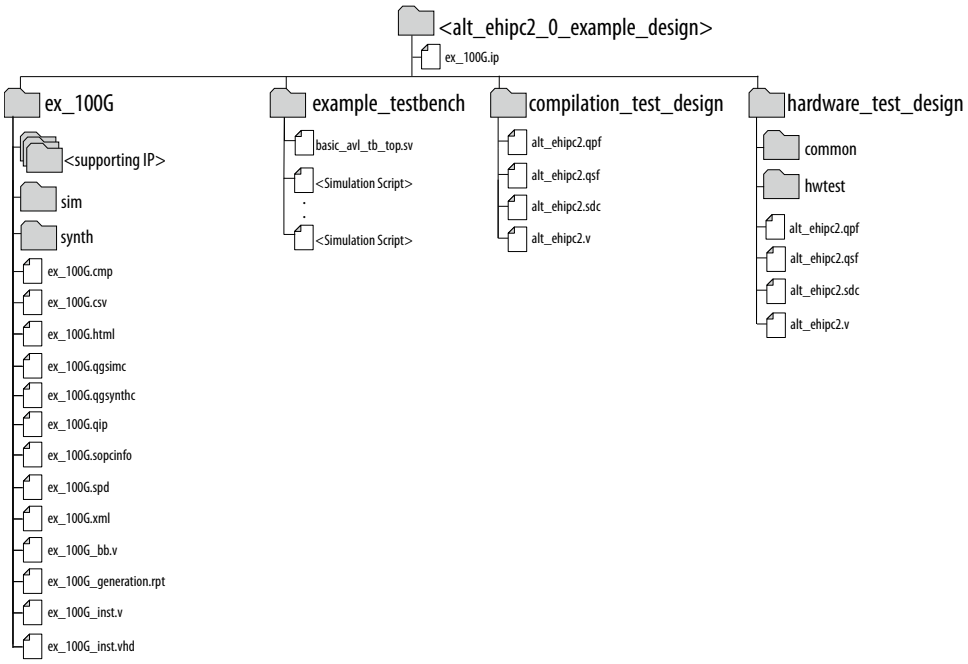
- H-Tile Hard IP for Ethernet Intel Stratix 10 Release Notes
  The IP Release Notes list IP changes in a particular release.

1.1. Directory Structure

Figure 2. H-Tile Hard IP for Ethernet Intel FPGA Design Example Directory Structure



The hardware configuration and test files (the hardware design example) are located in *<design_example_dir>*/hardware_test_design. The simulation files (testbench for simulation only) are located in *<design_example_dir>*/example_testbench. The compilation-only design example is located in *<design_example_dir>*/compilation_test_design.

Table 1. H-Tile Hard IP for Ethernet Intel FPGA IP Core Testbench File Descriptions

File Names	Description
Key Testbench and Simulation Files	
basic_avl_tb_top.sv	Top-level testbench file. The testbench instantiates the DUT and runs Verilog HDL tasks to generate and accept packets.
Testbench Scripts	
run_vsim.do	The Mentor Graphics ModelSim* script to run the testbench.
run_vcs.sh	The Synopsys VCS* script to run the testbench.
run_vcsmx.sh	The Synopsys VCS MX* script (combined Verilog HDL and System Verilog with VHDL) to run the testbench.
run_ncsim.sh	The Cadence NCSim* script to run the testbench.
run_xcelium.sh	The Xcelium* script to run the testbench.

Table 2. H-Tile Hard IP for Ethernet Intel FPGA IP Core Hardware Design Example File Descriptions

File Names	Description
`alt_ehip2.qpf`	Intel Quartus® Prime project file
`alt_ehip2.qsf`	Intel Quartus Prime project settings file
`alt_ehip2.sdc`	Synopsys Design Constraints files. You can copy and modify these files for your own H-Tile Hard IP for Ethernet Intel FPGA design.
`alt_ehip2.v`	Top-level Verilog HDL design example file
`common/`	Hardware design example support files
`hwtest/main.tcl`	Main file for accessing System Console

1.2. Generating the Design

Figure 3. Procedure

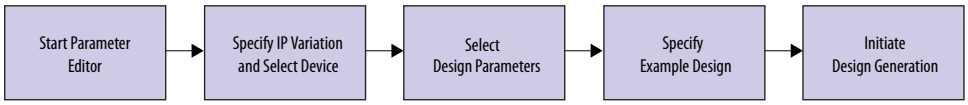
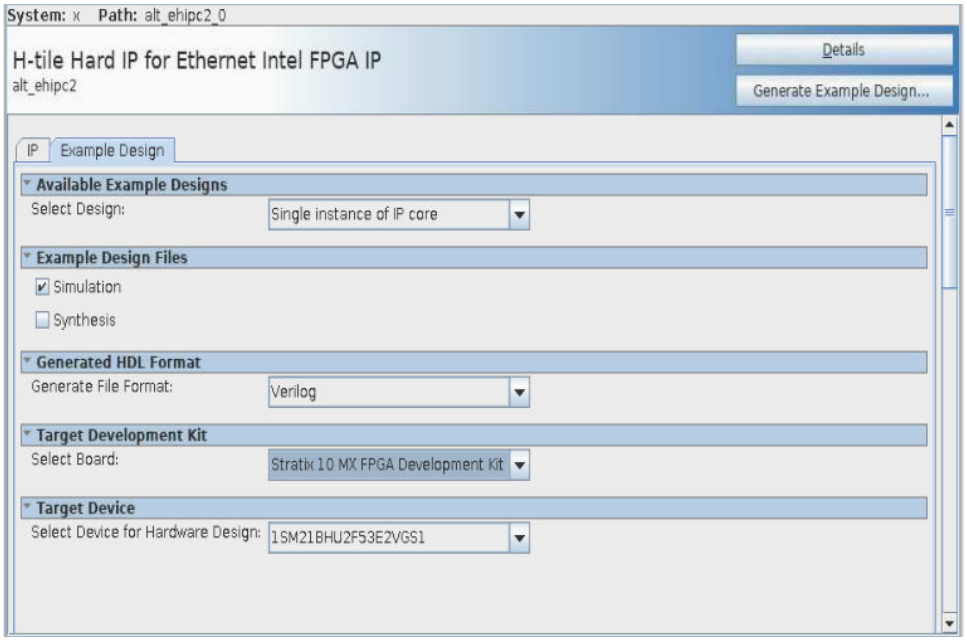


Figure 4. Example Design Tab in the H-Tile Hard IP for Ethernet Intel FPGA IP Parameter Editor



Follow these steps to generate the H-Tile Hard IP for Ethernet Intel FPGA IP hardware design example and testbench:

1. If you do not already have an Intel Quartus Prime Pro Edition project in which to integrate your H-Tile Hard IP for Ethernet Intel FPGA IP core, you must create one.

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