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PCI v4.1 Getting Started Guide

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The following table shows the revision history for this document.

	Version	Revision
7/13/06	1.0	Initial Xilinx release.

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About This Guide

The *PCI v4.1 Getting Started Guide* provides information about the LogiCORE™ Peripheral Component Interconnect (PCI) interface, which provides a fully verified, pre-implemented PCI bus interface targeting devices based on the Virtex™ architecture.

The guide also includes an example design in both Verilog-HDL and VHDL that lets you simulate, synthesize, and implement the interface to understand the PCI design flow.

Guide Contents

This guide contains the following chapters:

- [Chapter 1, “Introduction”](#) describes the PCI core and provides information about additional documentation, getting technical support, and providing feedback to Xilinx about the core and the accompanying documentation.
- [Chapter 2, “Installing and Licensing the Core”](#) provides instructions for installing and obtaining a license for the PCI interface core, which you must do before using it in your designs.
- [Chapter 3, “Getting Started”](#) provides an overview of the PCI example design and instructions for generating the core.
- [Chapter 4, “Functional Simulation”](#) describes the use of supported functional simulation tools, including Cadence NC-Sim v5.7 and Model Technology ModelSim® v6.1e.
- [Chapter 5, “Synthesis and Implementation”](#) describes the use of supported synthesis tools using the *Userapp* example design for step-by-step instructions.
- [Chapter 6, “Timing Simulation”](#) describes the use of supported post-route timing simulation tools, including Cadence NC-Sim and Model Technology ModelSim.

Additional Resources

For additional information, go to [com](#). The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches com/apps/appsweb.htm
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment com/xlnx/xil_tt_home.jsp

Conventions

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	speed grade: - 100
Courier bold	Literal commands you enter in a syntactical statement	ngdbuild <i>design_name</i>

以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：<https://d.book118.com/596130024001010035>