Paralleling Power – Choosing and Applying the Best Technique for Load Sharing

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Redundant and distributed power systems often invoke the need to parallel power stages for a variety of reasons, among them enhanced reliability, enabling the use of standardized designs with varying loads, distributing heat sources, and for improved maintainability. However, paralleling usually requires load sharing to equalize stresses, and while many techniques have been used, there are many compromises between complexity and performance. This topic attempts to simplify the selection process by describing and comparing the more popular approaches and, through analysis and example, provide guidelines for the designer. Load share techniques from simple droop methods to closed loop current control - as well as many variations of each - are included in this material together with the design information to simplify their application.

I. INTRODUCTION

The topic of paralleling power supplies was on the sideline of design engineering tasks for decades. Except in a few specialized application areas like high reliability and redundant systems typically used in space, military, telecommunication central power systems and high end mainframe computers, sharing the load current among several parallel operated power supplies was not required.

Recent efforts in standardization, miniaturization and the proliferation of high current, low voltage power supplies have directed additional attention to various techniques to parallel power stages. The fundamental difficulty using parallel power processing circuits is to ensure that the load current is properly distributed among the parallel connected power modules. Only then, the design can be optimized for the highest reliability and lowest cost by ensuring equal temperature rise and by minimizing the power rating of the individual components.

As a starting point, it is important to establish the purpose and benefits of parallel power supplies and accompanying load sharing techniques in a typical power system design.

Standardization – load sharing enables the use of lower power, standardized modules across several applications promoting design reuse. The standardized approach makes power system solutions easily transferable between different end equipment platforms significantly reducing the time-to-market period. At the same time it increases component selection by allowing to choose from a wider variety of lower power components more readily available from different manufacturers.

Modularity – the resulting modularity provides great flexibility to the user. Systems can be easily reconfigured to accommodate broad variety of output voltage and load current combinations. Expandability of such a system provides a simple way to keep up with increasing load current requirements.

Redundancy – when implemented, maximizes system availability in critical applications. A redundant system has at least one reserve module which provides extra output current above and beyond the maximum current required by the load. Additional benefits of redundant power systems include improved maintainability as faulty units can be exchanged without system interruption. Furthermore, enhanced reliability is achieved through operating the modules below their full output current rating thus reducing their power dissipation and temperature rise.

Thermal management – the primary driver in all paralleling schemes for lower power applications is the decentralized heat dissipation of the parallel power stages. By distributing the power dissipation among a larger number of power components and over an increased surface area, thermal management and airflow requirements can be kept at a more economical level.

Equalizing temperature rise – it is well established knowledge among reliability engineers that operating temperature has a profound effect on the life expectancy of electronic components. A well designed load sharing circuit ensures equal distribution of the load current among the parallel connected power supplies. Matching currents mean equal power dissipation, i.e. very similar temperature rise which will improve the long term reliability of the system.

Minimizing component ratings – voltage and current ratings of electronic components in the power supply are proportional to the continuous power rating of the circuit. Since the accuracy of load sharing has a direct impact on the maximum power each power stage has to process, the chosen load sharing technique has a direct, measurable impact on the cost of the system.

The price to pay for all these benefits is the added complexity introduced by the load share circuit which varies widely depending on the implemented technique.

II. PARALLELING POWER STAGES

The simplest concept of paralleling is demonstrated in Fig. 1 picturing parallel operated power stages controlled by a single control loop. The operation is based on a single feedback loop and pulse width modulator (PWM). The controller generates the duty cycle D which is distributed for the main power switches.

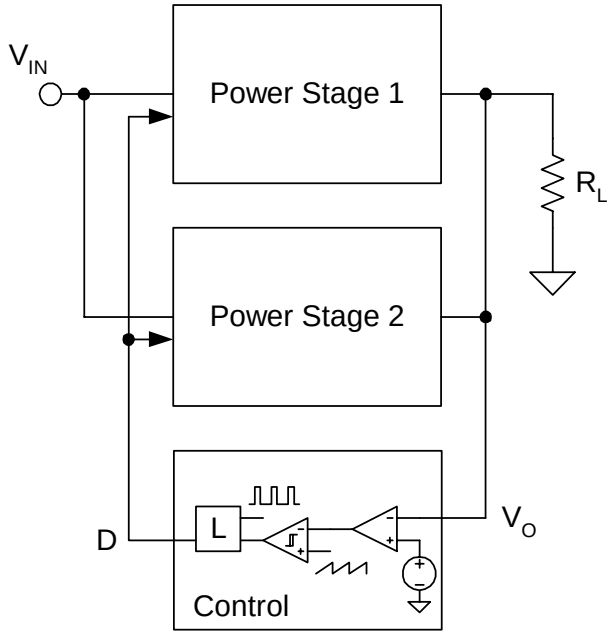

Fig. 1. Concept of parallel power stages.

This approach assumes voltage mode control because the single PWM comparator is unable to control the individual currents of the power stages. Thus, the clock ramp is used to determine the necessary duty ratio. In order to achieve load sharing among the modules, the power stages must be identical. Not only the components, but the printed circuit board layouts of the power stages must match very well.

Unfortunately, 100 percent matching is not achievable in practice, which will have an effect on how well the load current is distributed in this system. Component tolerances and parasitic circuit elements will ultimately introduce minor difference in the effective duty ratio of the power stages even though the control duty ratio, D is identical for each one of them.

Since the input and output voltages are common for all the parallel units there is only one correct duty ratio which satisfies the transfer function of the chosen topology. To demonstrate this phenomenon, Fig. 2 shows the effective duty cycles and energy storage inductor current waveforms of two parallel power stages used in Fig. 1.

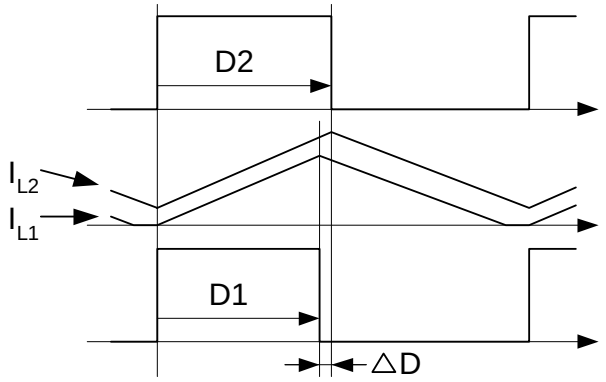

Fig. 2. Effective duty ratio difference and its effect on the inductor current waveforms.

The correct duty cycle always corresponds to the longest conduction period of the main switch, while energy transfer from the input to the output takes place. This can be proven easily by looking at the volt-second balance, i.e. current waveform in the energy storage inductors. In this case the actual output inductor value and switching frequency have no effect, since they will influence the ripple current amplitude only.

As shown in Fig. 2, the duty cycle D2 keeps the current constant as the starting and finishing points of the current waveforms are equal. Accordingly, the shorter D1 duty cycle is insufficient to apply enough volt-second product for balance to be reached. Therefore the average current in L2 will decrease until – in steady state – discontinuous mode operation is established as pictured in Fig. 2.

Based on these observations, the operation of the system can be described as follows: at light load, while all power stages are in discontinuous inductor current mode (DCM), they will share the load current reasonably well. As soon as the operation is in continuous inductor current mode (CCM), the power stage with the largest effective duty ratio will deliver most of the load current while the other stages stay in DCM. Their average output current will remain relatively low and can be estimated as:

$$I_O \approx \frac{I_{L,P-P}}{2}$$

Considering the above findings the system in Fig. 1 would never work, because only one unit – with the largest effective duty cycle – could operate in continuous inductor current mode and it would deliver almost all of the load current. Fortunately, there is a balancing mechanism which makes this approach useable. As current increases in the converter, there are resistive voltage drops which work in our favor. Fig. 3 explains what happens when the resistive voltage drop is taken into consideration.

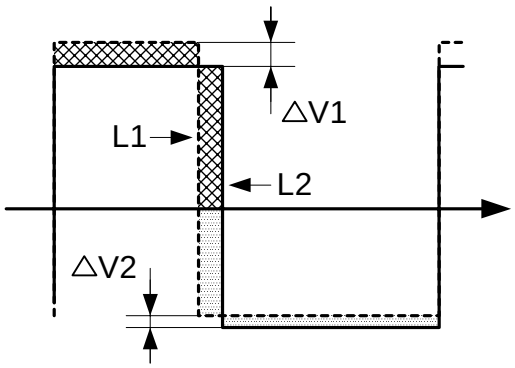

Fig. 3. Volt-second balancing based on parasitic resistive voltage drop.

As current increases in the power stage with the largest duty cycle so does the resistive voltage drop. Fig. 3 depicts a steady state operating point where the voltage drops ΔV1 and ΔV2 provide the necessary balancing mechanism. The required voltage drops correspond to a very well defined constant current difference between the two output currents. Once this ΔI is developed between the two outputs, both inductor can operate in CCM thus they will share the load. ΔI depends on the input and output voltages, V_{IN} and V_O respectively, transformer turns ratio where it is applicable ($N=N_P/N_S$), the duty cycle difference, ΔD and the equivalent resistance, R_{EQV} in the path of the current.

ΔI can be calculated based on the equivalent circuit of Fig. 4 which represents a generic power stage where all components are transformed to the energy storage inductor side of the circuit. In this model, R'_P is the primary side resistance transformed to the secondary side by the turns ratio, R_{SEC} is the resistance of the secondary winding of the transformer, R_{SW} is the resistance of the forward switch, R_{IND} is the winding resistance of the inductor and R_{SR} is the resistance of the freewheeling rectifier element. Depending on the power stage topology, some components might not be present in the equivalent circuit.

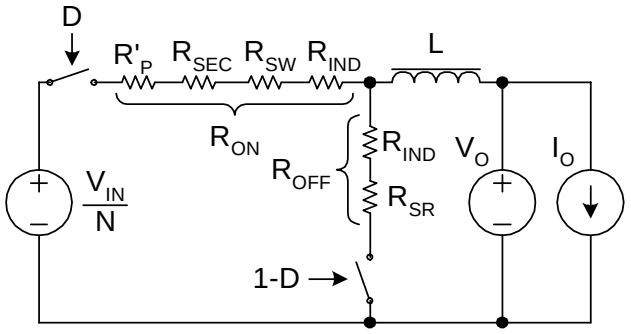

Fig. 4. Simplified power stage model.

The calculation is based on the fact that the average voltage applied on the left hand side of the inductor must be equal to the output voltage V_O. This condition can be expressed as:

$$\left(\frac{V_{IN}}{N} - I_O \cdot R_{ON}\right) \cdot D - I_O \cdot R_{OFF}(1-D) = V_O$$

which expression can be rearranged as:

$$\frac{V_{IN}}{N} \cdot D = V_O + I_O \cdot \left(R_{ON} \cdot D + R_{OFF} \cdot (1-D)\right)$$

From this, the equivalent resistance can be found as:

$$R_{EQV} = R_{ON} \cdot D + R_{OFF} \cdot (1-D)$$

Although R_{EQV} is a function of the duty cycle, it can be assumed that for small duty cycle change its value is constant. After substituting R_{EQV} and looking at the effect of small change in duty cycle:

$$\frac{V_{IN}}{N} \cdot \Delta D = \Delta I_O \cdot R_{EQV}$$

which gives:

$$\Delta I_O = \frac{V_{IN}}{N \cdot R_{EQV}} \cdot \Delta D$$

This equation shows that the current difference is constant. The equation can be further modified for percentage errors at a chosen operating point (I_O). It is the ratio of the module's output current deviation to the load current divided by the number of parallel power stages (n):

$$\%E(I_O) = \frac{(n-1) \cdot V_{IN} \cdot D}{n \cdot N \cdot R_{EQV} \cdot I_O} \cdot \%D$$

The above equation can be used to calculate the current sharing accuracy as a function of the load current and effective duty cycles of the power stages. Since the output current shows up in the denominator on the right hand side, the percentage of error diminishes at higher output currents which is consistent with a fixed current error. Finally, Fig. 5 summarizes the load sharing characteristic of the system in Fig. 1 using two power trains.

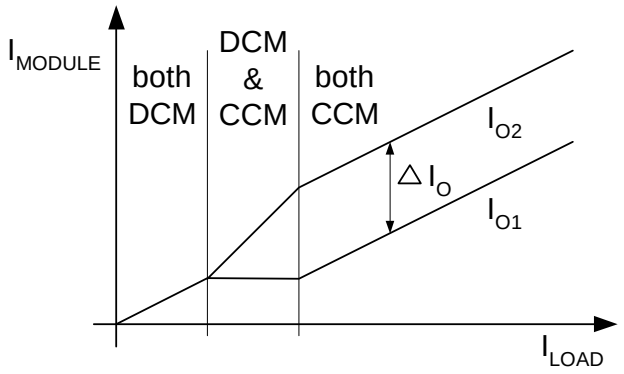

Fig. 5. Load share profile of parallel power stages (single voltage mode controller).

As mentioned before, one of the main disadvantages of this technique is that it can not be implemented with current mode control. Even simple current limiting can be troublesome using only one current sense signal representing the sum of the currents in the parallel power stages.

In order to implement cycle-by-cycle current limiting in the individual power stages, parts of the PWM logic must be implemented locally as shown in Fig. 6.

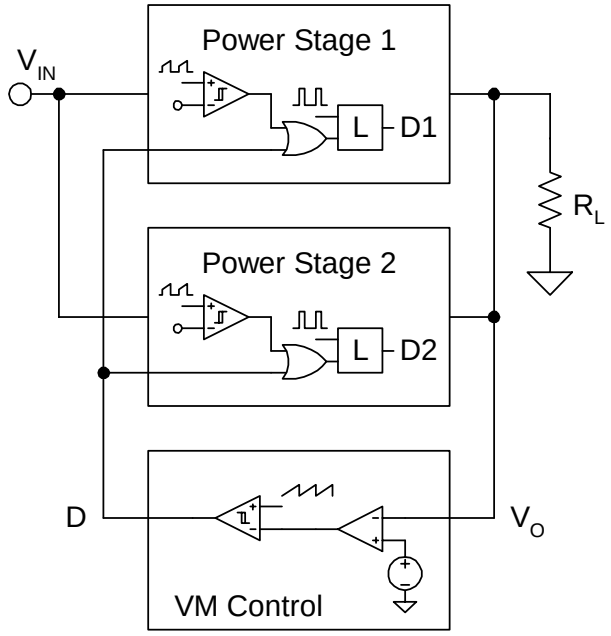

Fig. 6. Parallel power stages with independent cycle-by-cycle current limit.

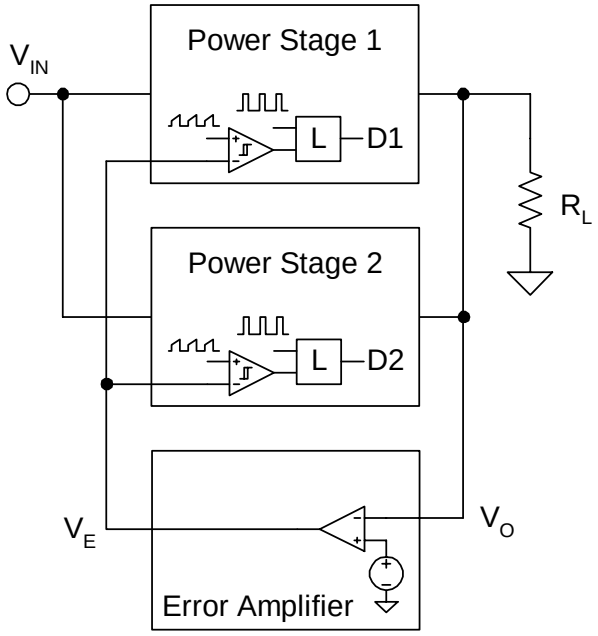

Fig. 7. Current mode control for parallel power stages.

In voltage mode control, it is still desirable to use a single PWM controller to determine the operating duty cycle and distribute D between the parallel power stages. This master duty ratio can be truncated by the cycle-by-cycle current limit comparator to protect the individual circuits against over current.

This technique is preferred over duplicating the PWM comparators at the power stage level because it prevents additional errors due to variation between local ramps. Inequality in ramp amplitude and ground potentials can easily turn into duty cycle difference when using a common feedback signal. As shown previously, duty cycle difference can cause large discrepancy in output currents in absence of a balancing mechanism.

Of course, once a current comparator is introduced to the system for cycle-by-cycle protection, current mode control can be readily implemented which can maintain equilibrium for the parallel connected power stages. Fig. 7 displays the simplified schematic of a current mode configuration for parallel power stages.

This approach still uses a single voltage error amplifier for output voltage regulation. The error signal, V_E is distributed throughout the system. The control is based on comparing the peak currents of the parallel power stages to this common error voltage. The duty cycles now can be individually adjusted to maintain similar current levels in the parallel connected power circuits. Consequently, peak current mode control eradicates the large error caused by duty cycle inequality. Unfortunately it has its own error sources which will determine the performance of the system. These error terms are demonstrated in the simplified schematic of Fig. 8 and will help to quantify the potential accuracy of the technique.

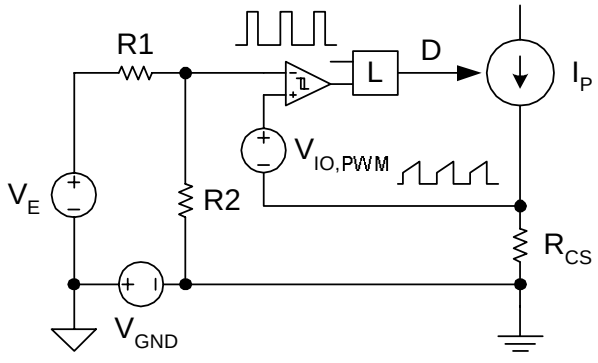

Fig. 8. Error sources in peak current mode control.

Since each power stage determines its own unique operating duty ratio to control the peak current in the circuit, the PWM comparator and logic must be locally duplicated. The common error signal is than compared to the measured current sense signal at the input terminals of the PWM comparator in each power stage. There are three components which affect the accuracy of the peak current measurements. According to Fig. 8, V_{GND} is the potential difference between the analog ground of the error signal V_E and the respective power grounds which serve as the reference potential for the current sense resistor. The tolerance of the resistor value itself is another source for error. Finally, the input offset voltage of the PWM comparator contributes to the inaccuracies as well. The following equation gives the relationship between the controlled peak current and the variables in the measurement circuit:

$$(V_E + V_{GND}) \cdot G_{DIV} = I_P \cdot R_{CS} + V_{IO,PWM}$$

where the divider gain is defined as:

$$G_{DIV} = \frac{R2}{R1 + R2}$$

The peak current, I_P can be expressed as:

$$I_P = \frac{G_{DIV} \cdot (V_E + V_{GND}) + V_{IO,PWM}}{R_{CS}}$$

This peak current is the sum of the peak magnetizing and the peak output inductor currents as shown in Fig. 9. Therefore, the effect of the magnetizing and output inductor value on the average output current should be analyzed next. These errors are not related to measurement accuracy. They stem from the fundamental operation of peak current mode control and a systematic peak-to-average error.

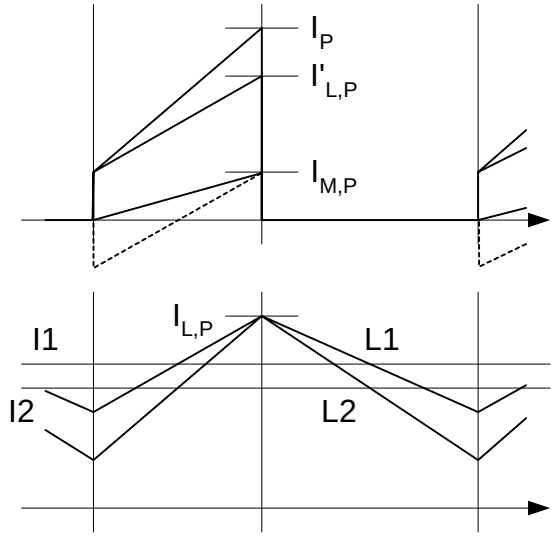

Fig. 9. Contributions of magnetizing and output inductor tolerances to load share error.

According to the waveforms, the peak current can be expressed as:

$$I_P = I_{M,P} + I'_{L,P}$$

where

$$I_{M,P} = \frac{V_{IN}}{L_M} \cdot D \cdot T$$

and

$$I'_{L,P} = \frac{1}{N} \cdot \left(I_O + \frac{(V_{IN} - V_O \cdot N) \cdot D \cdot T}{2 \cdot N \cdot L_O} \right)$$

The first expression describes the effect of the magnetizing inductance while the second equation gives the peak-to-average error as a function of the output inductor value. Equating the two expressions of I_P and solving it for I_O yields:

$$I_O = \left(G_{DIV} \cdot (V_E + V_{GND}) + V_{IO,PWM}\right) \cdot \frac{N}{R_{CS}} - N \cdot V_{IN} \cdot D \cdot T \cdot \frac{1}{L_M} - \frac{(V_{IN} - V_O \cdot N) \cdot D \cdot T}{2 \cdot N} \cdot \frac{1}{L_O}$$