EECS 247

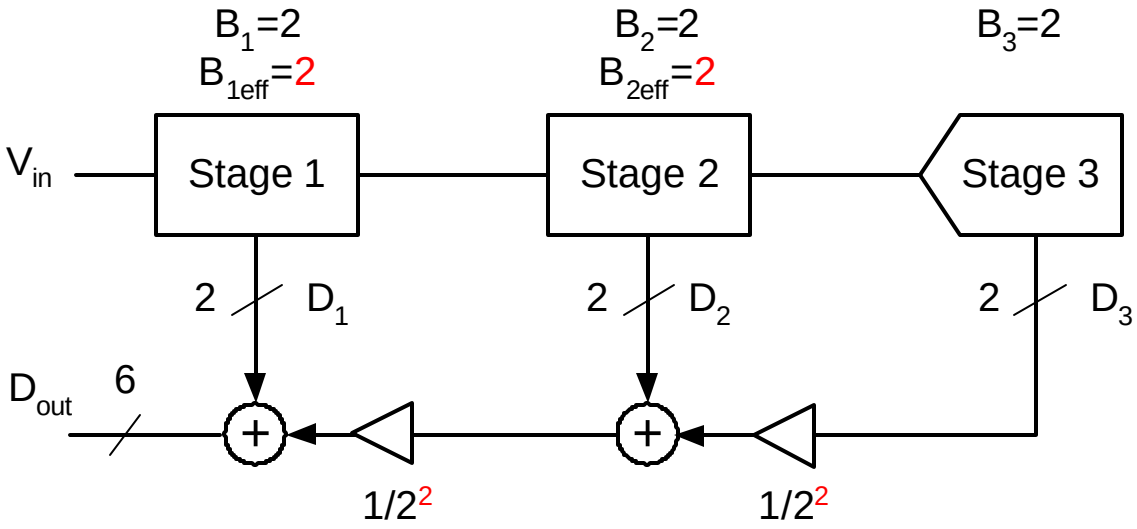
Lecture 14:
Pipelined ADCs
Figures of Merit and Trends

Today's Lecture

- Pipelined ADCs
  - Combining the bits
  - Stage implementation
    - Circuits
    - Noise budgeting
- Figures of Merit and Trends
  - How to use/not use FOMs
  - FOMs over time

Combining the Bits

- Example: Three 2-bit stages, no redundancy

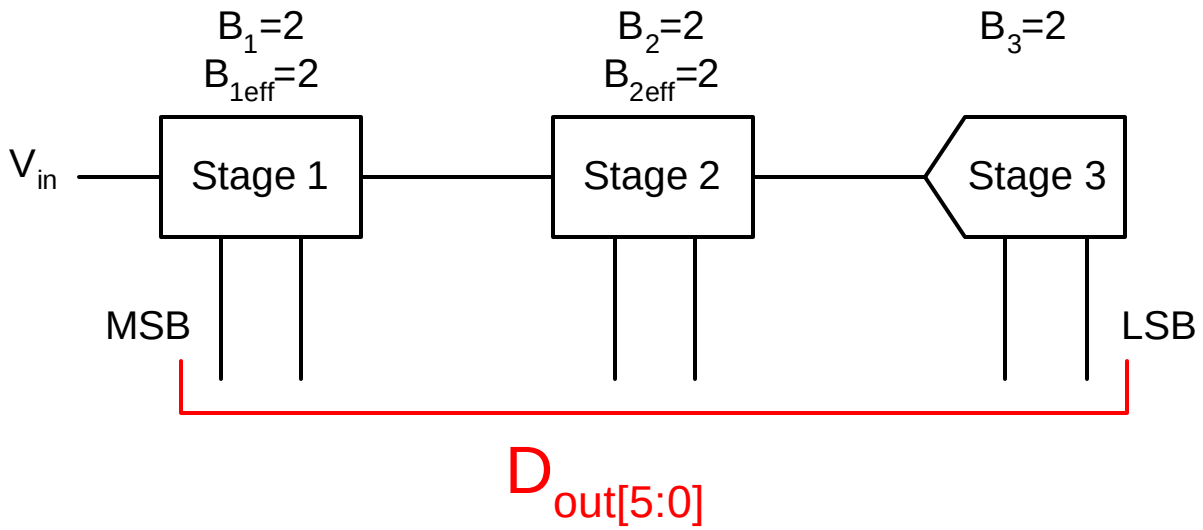


$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$

Combining the Bits

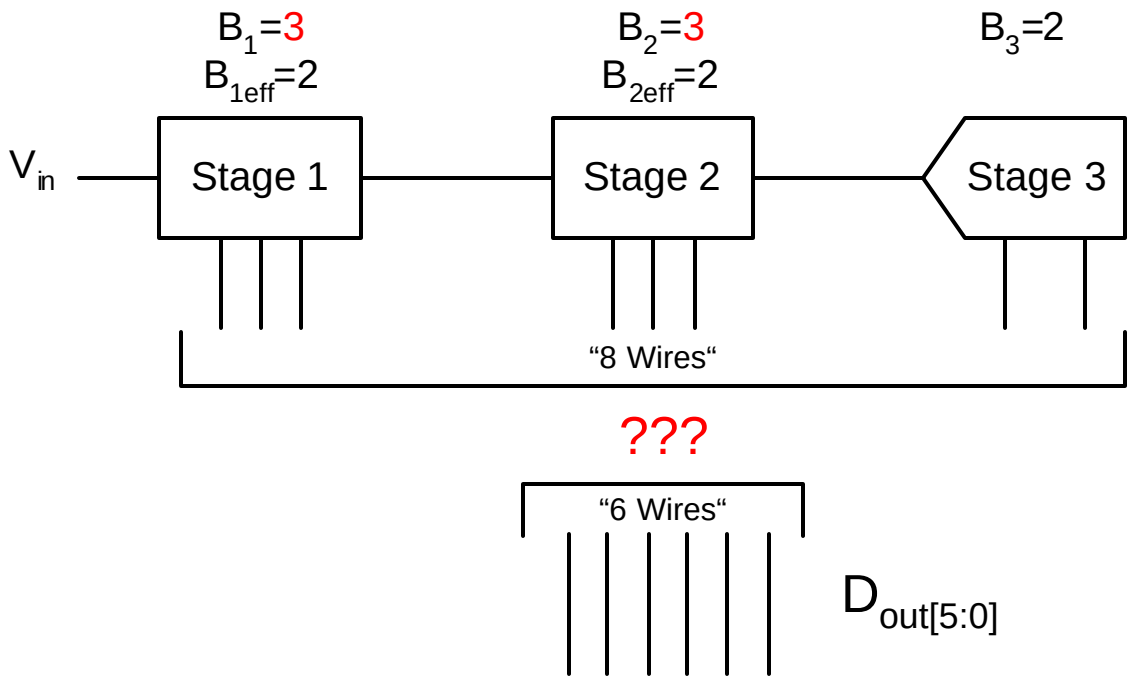
```
D1     XX
D2       XX
D3         XX
-------------
Dout   DDDDDD
```

- Only bit shifts
- No arithmetic circuits needed



Combining the Bits

- Example: Three 2-bit stages, one bit redundancy in stages 1 and 2



Combining the Bits

$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$

```
D1     XXX
D2       XXX
D3         XX
-------------
Dout   DDDDDD
```

- Bits overlap
- Need adders