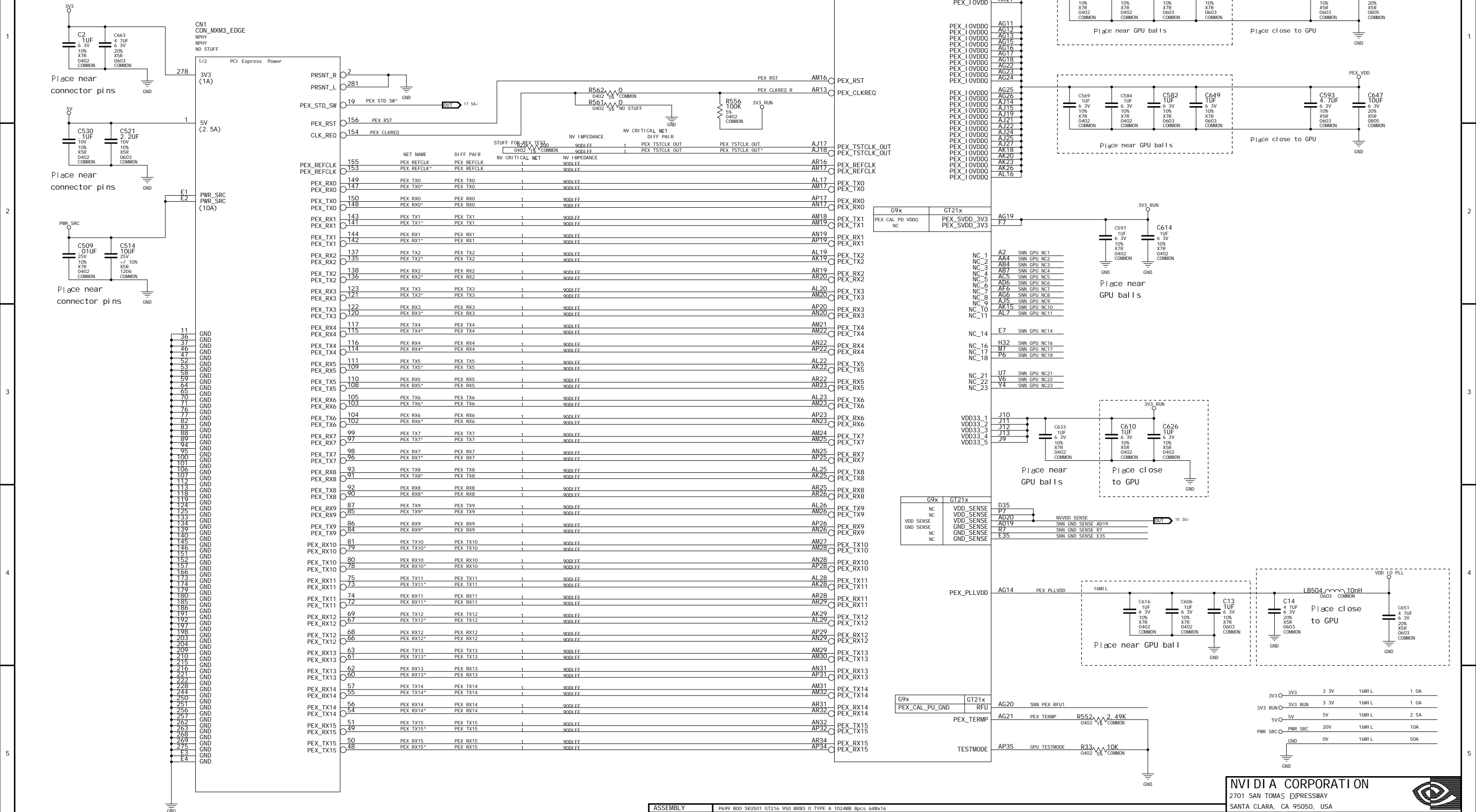


## 2. MXM 3.0 CONNECTOR, PCI EXPRESS INTERFACE



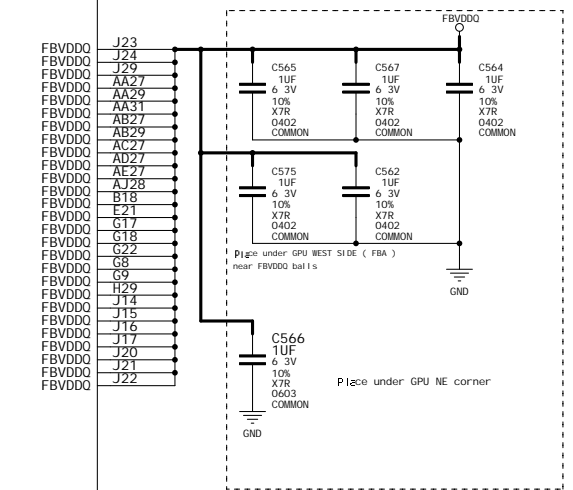
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# 3. GPU MEMORY INTERFACE

G1  
GT216 630 A1  
BGA699  
CHANGED

2/16 FBA

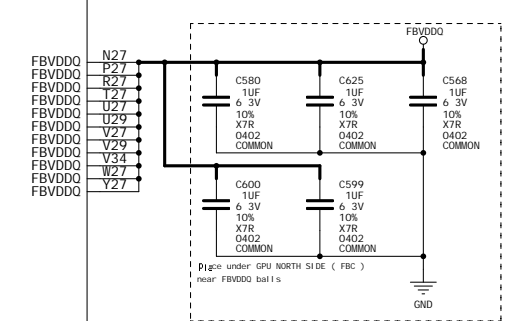
GT21x	G9x
FBA_D0	FBA_D14
FBA_D1	FBA_D15
FBA_D2	FBA_D16
FBA_D3	FBA_D17
FBA_D4	FBA_D18
FBA_D5	FBA_D19
FBA_D6	FBA_D20
FBA_D7	FBA_D21
FBA_D8	FBA_D22
FBA_D9	FBA_D23
FBA_D10	FBA_D24
FBA_D11	FBA_D25
FBA_D12	FBA_D26
FBA_D13	FBA_D27
FBA_D14	FBA_D28
FBA_D15	FBA_D29
FBA_D16	FBA_D30
FBA_D17	FBA_D31
FBA_D18	FBA_D32
FBA_D19	FBA_D33
FBA_D20	FBA_D34
FBA_D21	FBA_D35
FBA_D22	FBA_D36
FBA_D23	FBA_D37
FBA_D24	FBA_D38
FBA_D25	FBA_D39
FBA_D26	FBA_D40
FBA_D27	FBA_D41
FBA_D28	FBA_D42
FBA_D29	FBA_D43
FBA_D30	FBA_D44
FBA_D31	FBA_D45
FBA_D32	FBA_D46
FBA_D33	FBA_D47
FBA_D34	FBA_D48
FBA_D35	FBA_D49
FBA_D36	FBA_D50
FBA_D37	FBA_D51
FBA_D38	FBA_D52
FBA_D39	FBA_D53
FBA_D40	FBA_D54
FBA_D41	FBA_D55
FBA_D42	FBA_D56
FBA_D43	FBA_D57
FBA_D44	FBA_D58
FBA_D45	FBA_D59
FBA_D46	FBA_D60
FBA_D47	FBA_D61
FBA_D48	FBA_D62
FBA_D49	FBA_D63
FBA_D50	
FBA_D51	
FBA_D52	
FBA_D53	
FBA_D54	
FBA_D55	
FBA_D56	
FBA_D57	
FBA_D58	
FBA_D59	
FBA_D60	
FBA_D61	
FBA_D62	
FBA_D63	



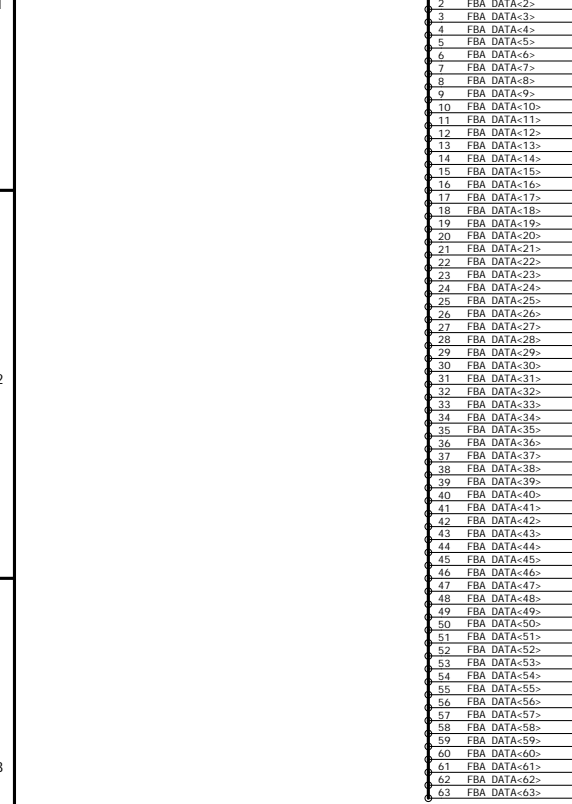
G1  
GT216 630 A1  
BGA699  
CHANGED

3/16 FBC

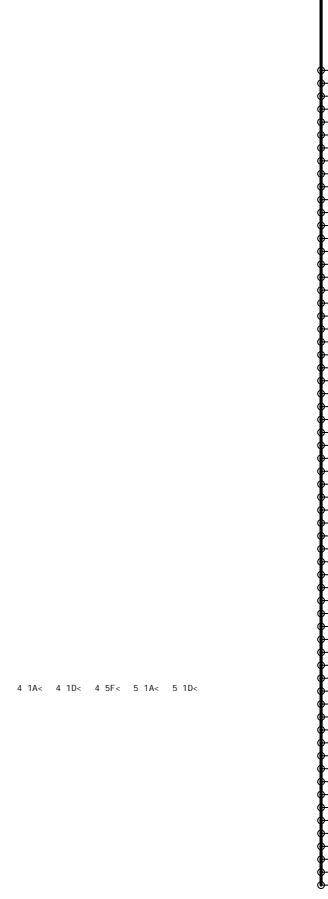
GT21x	G9x
FBC_D0	FBC_D26
FBC_D1	FBC_D27
FBC_D2	FBC_D28
FBC_D3	FBC_D29
FBC_D4	FBC_D30
FBC_D5	FBC_D31
FBC_D6	FBC_D32
FBC_D7	FBC_D33
FBC_D8	FBC_D34
FBC_D9	FBC_D35
FBC_D10	FBC_D36
FBC_D11	FBC_D37
FBC_D12	FBC_D38
FBC_D13	FBC_D39
FBC_D14	FBC_D40
FBC_D15	FBC_D41
FBC_D16	FBC_D42
FBC_D17	FBC_D43
FBC_D18	FBC_D44
FBC_D19	FBC_D45
FBC_D20	FBC_D46
FBC_D21	FBC_D47
FBC_D22	FBC_D48
FBC_D23	FBC_D49
FBC_D24	FBC_D50
FBC_D25	FBC_D51
FBC_D26	FBC_D52
FBC_D27	FBC_D53
FBC_D28	FBC_D54
FBC_D29	FBC_D55
FBC_D30	FBC_D56
FBC_D31	FBC_D57
FBC_D32	FBC_D58
FBC_D33	FBC_D59
FBC_D34	FBC_D60
FBC_D35	FBC_D61
FBC_D36	FBC_D62
FBC_D37	FBC_D63



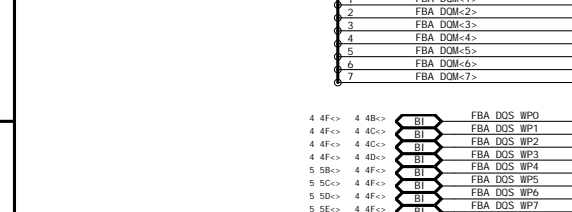
5 4k<-> 4 5F<-> 4 4k<-> BI FBA\_DATA<0>-



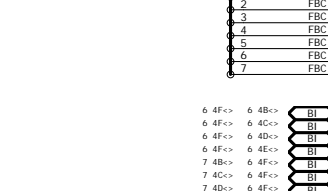
7 4k<-> 6 5F<-> 6 4k<-> BI FBC\_DATA<0>-



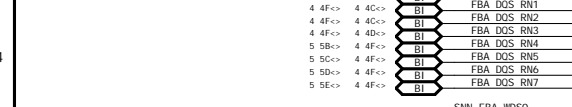
5 5k<-> 4 5F<-> 4 5k<-> BI FBA\_DOM<0>-



7 5k<-> 6 5F<-> 6 5k<-> BI FBC\_DOM<0>-



4 4F<-> 4 4k<-> BI FBA\_DOS\_WP0



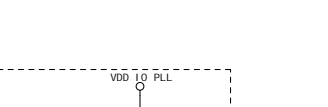
6 4F<-> 6 4k<-> BI FBC\_DOS\_WP0



4 4F<-> 4 4k<-> BI FBA\_DOS\_RN0



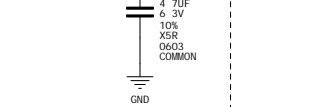
6 4F<-> 6 4k<-> BI FBC\_DOS\_RN0



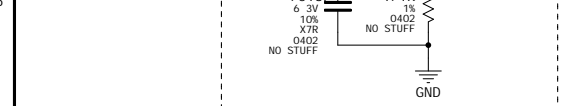
SNN FBA\_WDS0\* FBA\_WCK0



SNN FBC\_WDS0\* FBC\_WCK0



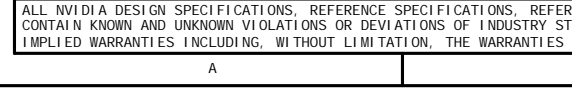
5 5k<-> 4 5F<-> 4 5k<-> BI FBA\_VREF



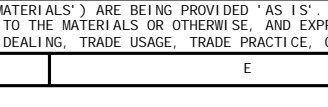
7 7k<-> 6 7F<-> 6 7k<-> BI FBC\_VREF



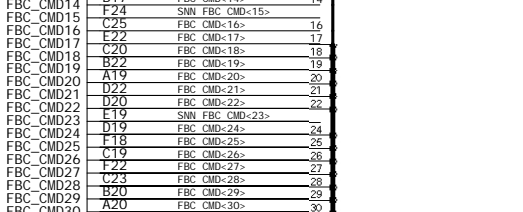
FB\_DLLAVDD FB\_PLLAVDD



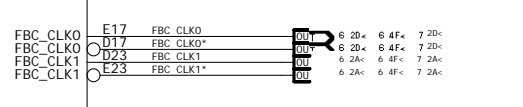
T30 FBA\_DEBUG R544 10K



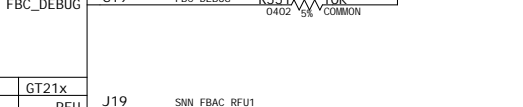
6 1k<-> 6 10k<-> 6 5F<-> 7 1k<-> BI FBC\_CMD<0>-



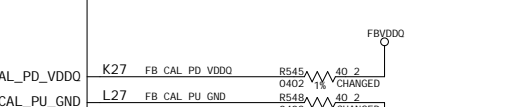
6 4F<-> 6 4k<-> BI FBC\_DOS\_WP0



6 4F<-> 6 4k<-> BI FBC\_DOS\_RN0



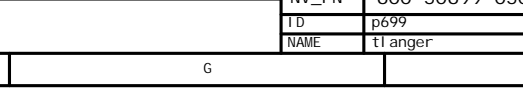
FBCAL\_PD\_VDD0



FBCAL\_PD\_VDD0



FBCAL\_PD\_VDD0



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SANTA CLARA, CA 95050, USA

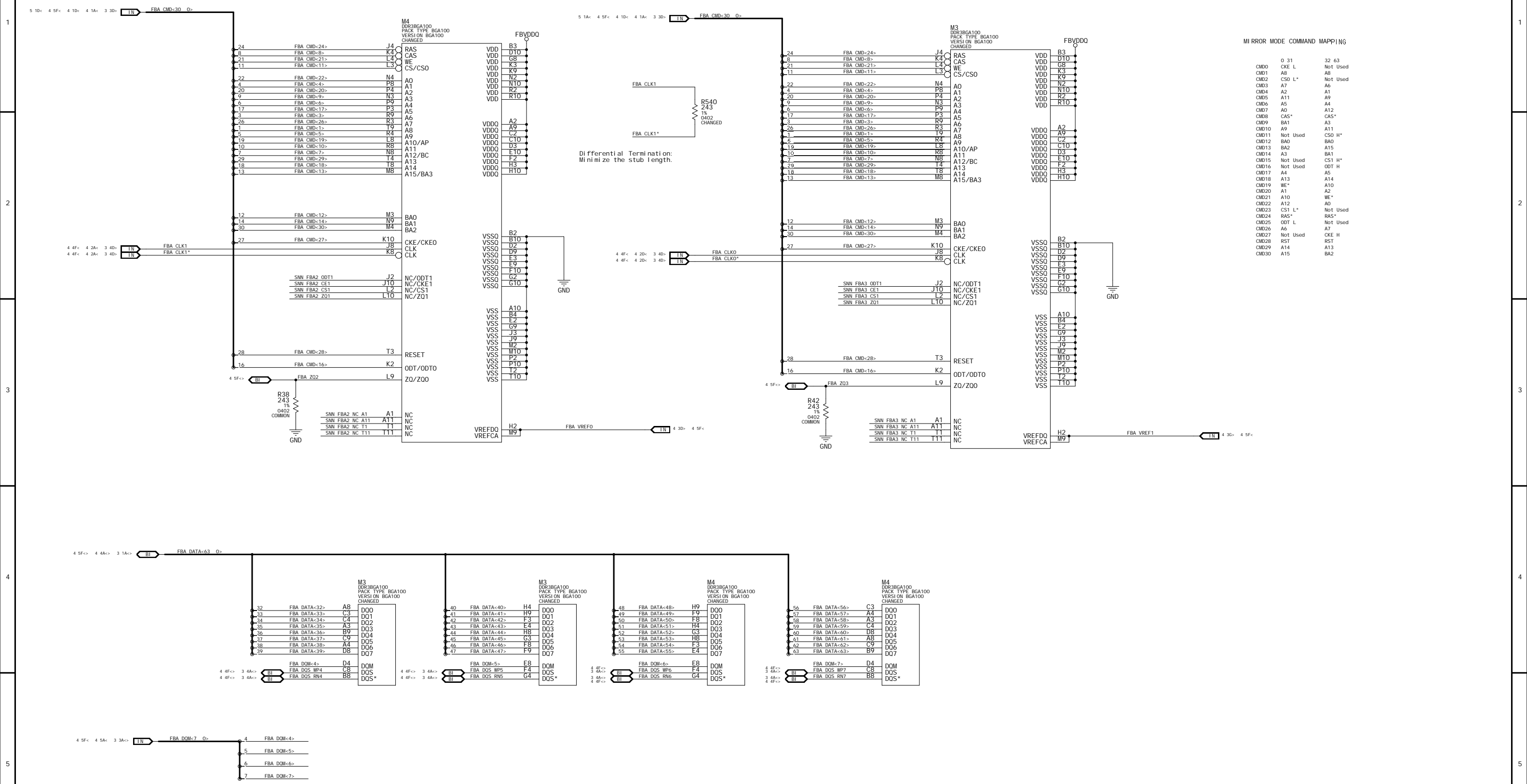
NV_PN	600-50699-0501-100 D
ID	p699
NAME	tlanger
PAGE	3 OF 17
DATE	15-APR-2009

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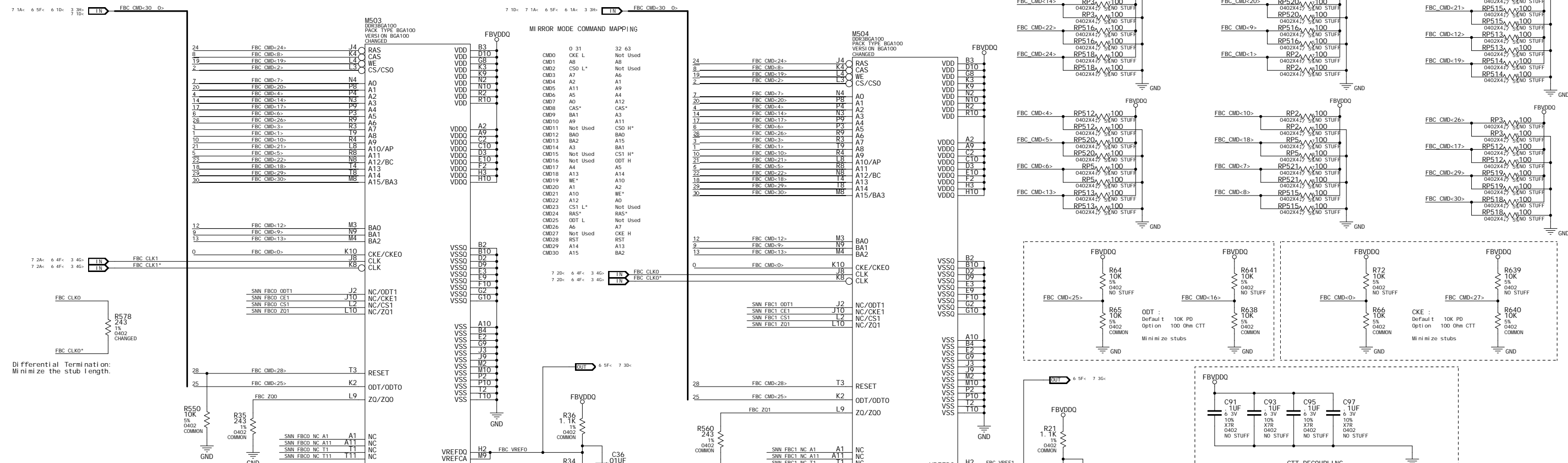
ASSEMBLY P699 B00 SKU501 GT216 950 MMX3 0 TYPE A 1024MB 8pc3 64Mx16  
PAGE DETAIL Frame Buffer GPU Interface



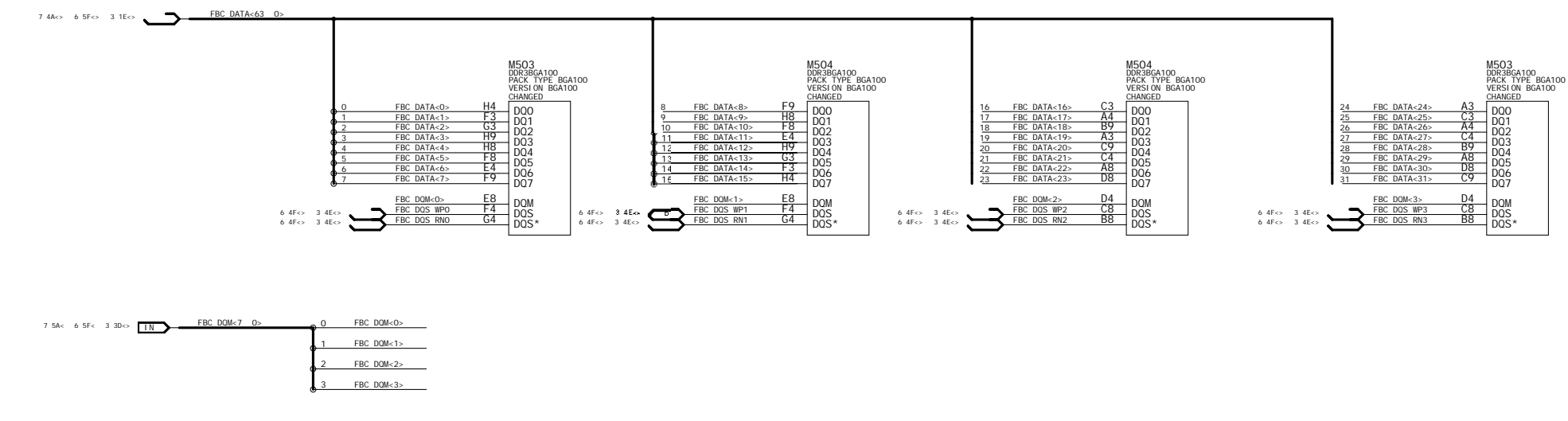
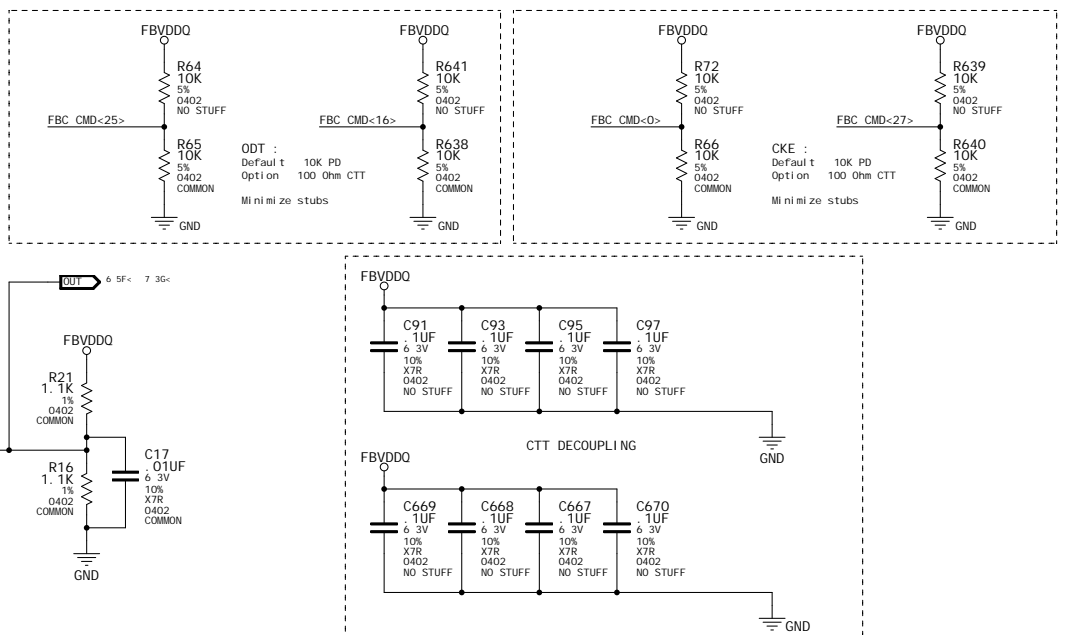
# 5. MEMORY PARTITION A UPPER 32 BITS



# 6. MEMORY PARTITION C LOWER 32 BITS



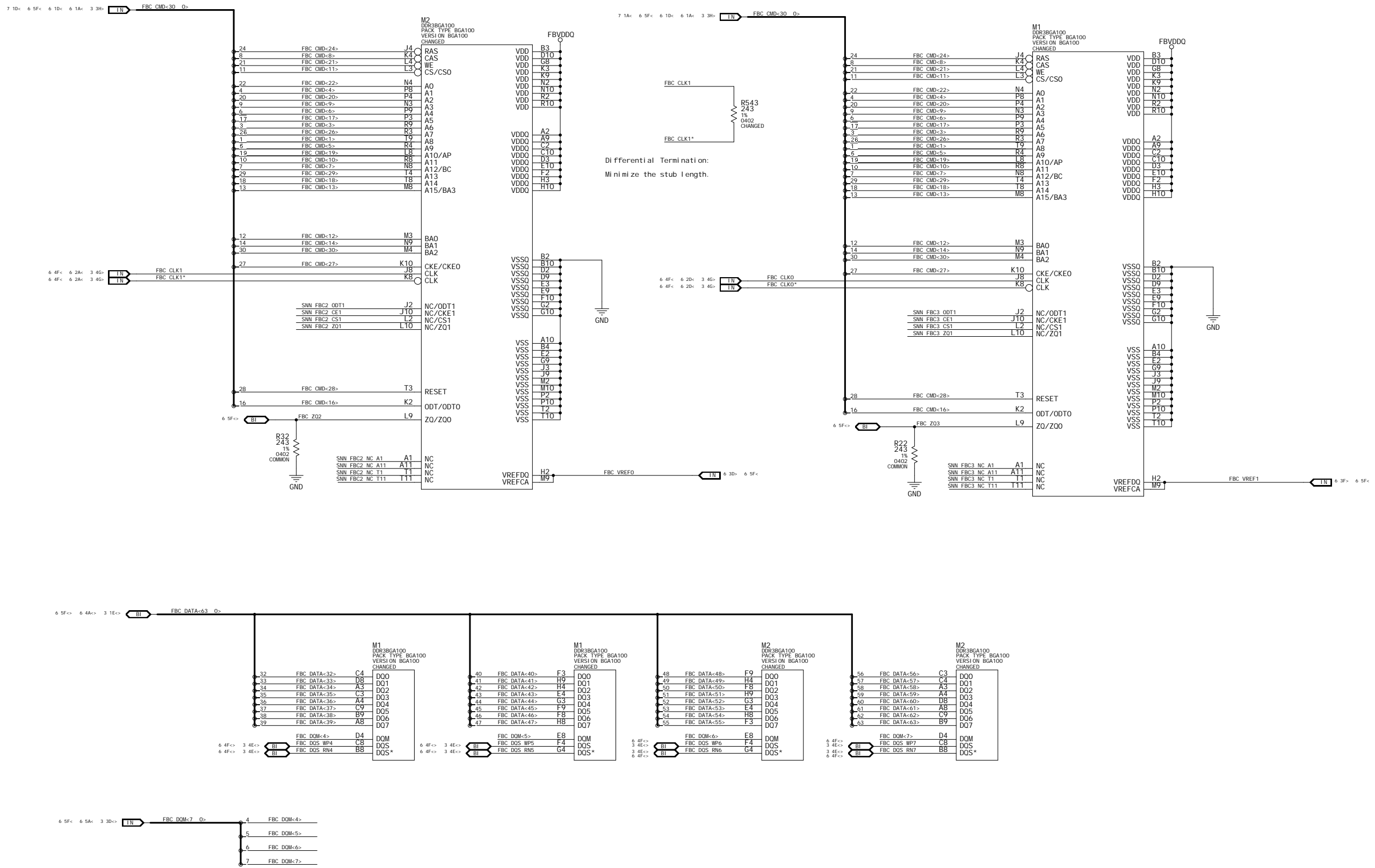
Differential Termination: Minimize the stub length.



### MEMORY PARTITION C SIGNAL CONSTRAINTS

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBVDDQ	FBVDDQ	1	100 OHM
FBC_CLK0	FBC_CLK0	1	70 OHM FF
FBC_CLK1	FBC_CLK1	1	70 OHM FF
FBC_CLK2	FBC_CLK2	1	70 OHM FF
FBC_CLK3	FBC_CLK3	1	70 OHM FF
FBC_CLK4	FBC_CLK4	1	70 OHM FF
FBC_CLK5	FBC_CLK5	1	70 OHM FF
FBC_CLK6	FBC_CLK6	1	70 OHM FF
FBC_CLK7	FBC_CLK7	1	70 OHM FF
FBC_CLK8	FBC_CLK8	1	70 OHM FF
FBC_CLK9	FBC_CLK9	1	70 OHM FF
FBC_CLK10	FBC_CLK10	1	70 OHM FF
FBC_CLK11	FBC_CLK11	1	70 OHM FF
FBC_CLK12	FBC_CLK12	1	70 OHM FF
FBC_CLK13	FBC_CLK13	1	70 OHM FF
FBC_CLK14	FBC_CLK14	1	70 OHM FF
FBC_CLK15	FBC_CLK15	1	70 OHM FF
FBC_CLK16	FBC_CLK16	1	70 OHM FF
FBC_CLK17	FBC_CLK17	1	70 OHM FF
FBC_CLK18	FBC_CLK18	1	70 OHM FF
FBC_CLK19	FBC_CLK19	1	70 OHM FF
FBC_CLK20	FBC_CLK20	1	70 OHM FF
FBC_CLK21	FBC_CLK21	1	70 OHM FF
FBC_CLK22	FBC_CLK22	1	70 OHM FF
FBC_CLK23	FBC_CLK23	1	70 OHM FF
FBC_CLK24	FBC_CLK24	1	70 OHM FF
FBC_CLK25	FBC_CLK25	1	70 OHM FF
FBC_CLK26	FBC_CLK26	1	70 OHM FF
FBC_CLK27	FBC_CLK27	1	70 OHM FF
FBC_CLK28	FBC_CLK28	1	70 OHM FF
FBC_CLK29	FBC_CLK29	1	70 OHM FF
FBC_CLK30	FBC_CLK30	1	70 OHM FF
FBC_CLK31	FBC_CLK31	1	70 OHM FF
FBC_CLK32	FBC_CLK32	1	70 OHM FF
FBC_CLK33	FBC_CLK33	1	70 OHM FF
FBC_CLK34	FBC_CLK34	1	70 OHM FF
FBC_CLK35	FBC_CLK35	1	70 OHM FF
FBC_CLK36	FBC_CLK36	1	70 OHM FF
FBC_CLK37	FBC_CLK37	1	70 OHM FF
FBC_CLK38	FBC_CLK38	1	70 OHM FF
FBC_CLK39	FBC_CLK39	1	70 OHM FF
FBC_CLK40	FBC_CLK40	1	70 OHM FF
FBC_CLK41	FBC_CLK41	1	70 OHM FF
FBC_CLK42	FBC_CLK42	1	70 OHM FF
FBC_CLK43	FBC_CLK43	1	70 OHM FF
FBC_CLK44	FBC_CLK44	1	70 OHM FF
FBC_CLK45	FBC_CLK45	1	70 OHM FF
FBC_CLK46	FBC_CLK46	1	70 OHM FF
FBC_CLK47	FBC_CLK47	1	70 OHM FF
FBC_CLK48	FBC_CLK48	1	70 OHM FF
FBC_CLK49	FBC_CLK49	1	70 OHM FF
FBC_CLK50	FBC_CLK50	1	70 OHM FF
FBC_CLK51	FBC_CLK51	1	70 OHM FF
FBC_CLK52	FBC_CLK52	1	70 OHM FF
FBC_CLK53	FBC_CLK53	1	70 OHM FF
FBC_CLK54	FBC_CLK54	1	70 OHM FF
FBC_CLK55	FBC_CLK55	1	70 OHM FF
FBC_CLK56	FBC_CLK56	1	70 OHM FF
FBC_CLK57	FBC_CLK57	1	70 OHM FF
FBC_CLK58	FBC_CLK58	1	70 OHM FF
FBC_CLK59	FBC_CLK59	1	70 OHM FF
FBC_CLK60	FBC_CLK60	1	70 OHM FF
FBC_CLK61	FBC_CLK61	1	70 OHM FF
FBC_CLK62	FBC_CLK62	1	70 OHM FF
FBC_CLK63	FBC_CLK63	1	70 OHM FF
FBC_CLK64	FBC_CLK64	1	70 OHM FF
FBC_CLK65	FBC_CLK65	1	70 OHM FF
FBC_CLK66	FBC_CLK66	1	70 OHM FF
FBC_CLK67	FBC_CLK67	1	70 OHM FF
FBC_CLK68	FBC_CLK68	1	70 OHM FF
FBC_CLK69	FBC_CLK69	1	70 OHM FF
FBC_CLK70	FBC_CLK70	1	70 OHM FF
FBC_CLK71	FBC_CLK71	1	70 OHM FF
FBC_CLK72	FBC_CLK72	1	70 OHM FF
FBC_CLK73	FBC_CLK73	1	70 OHM FF
FBC_CLK74	FBC_CLK74	1	70 OHM FF
FBC_CLK75	FBC_CLK75	1	70 OHM FF
FBC_CLK76	FBC_CLK76	1	70 OHM FF
FBC_CLK77	FBC_CLK77	1	70 OHM FF
FBC_CLK78	FBC_CLK78	1	70 OHM FF
FBC_CLK79	FBC_CLK79	1	70 OHM FF
FBC_CLK80	FBC_CLK80	1	70 OHM FF
FBC_CLK81	FBC_CLK81	1	70 OHM FF
FBC_CLK82	FBC_CLK82	1	70 OHM FF
FBC_CLK83	FBC_CLK83	1	70 OHM FF
FBC_CLK84	FBC_CLK84	1	70 OHM FF
FBC_CLK85	FBC_CLK85	1	70 OHM FF
FBC_CLK86	FBC_CLK86	1	70 OHM FF
FBC_CLK87	FBC_CLK87	1	70 OHM FF
FBC_CLK88	FBC_CLK88	1	70 OHM FF
FBC_CLK89	FBC_CLK89	1	70 OHM FF
FBC_CLK90	FBC_CLK90	1	70 OHM FF
FBC_CLK91	FBC_CLK91	1	70 OHM FF
FBC_CLK92	FBC_CLK92	1	70 OHM FF
FBC_CLK93	FBC_CLK93	1	70 OHM FF
FBC_CLK94	FBC_CLK94	1	70 OHM FF
FBC_CLK95	FBC_CLK95	1	70 OHM FF
FBC_CLK96	FBC_CLK96	1	70 OHM FF
FBC_CLK97	FBC_CLK97	1	70 OHM FF
FBC_CLK98	FBC_CLK98	1	70 OHM FF
FBC_CLK99	FBC_CLK99	1	70 OHM FF
FBC_CLK100	FBC_CLK100	1	70 OHM FF

# 7. MEMORY PARTITION C UPPER 32 BITS

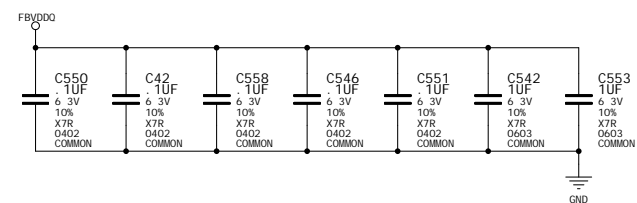


MI ERROR MODE COMMAND MAPPING

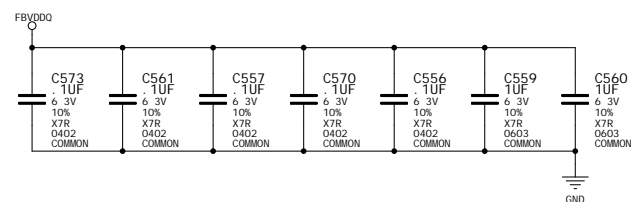
0	31	32	63
CMD0	CKE L	Not Used	
CMD1	AB	AB	
CMD2	CS0 L*	Not Used	
CMD3	A7	A6	
CMD4	A2	A1	
CMD5	A11	A9	
CMD6	A5	A4	
CMD7	A0	A12	
CMD8	CAS*	CAS*	
CMD9	BA1	A3	
CMD10	A9	A11	
CMD11	Not Used	CS0 H*	
CMD12	BA0	BA0	
CMD13	BA2	A15	
CMD14	A3	BA1	
CMD15	Not Used	CS1 H*	
CMD16	Not Used	ODT H	
CMD17	A4	A5	
CMD18	A13	A14	
CMD19	WE*	A10	
CMD20	A1	A2	
CMD21	A10	WE*	
CMD22	A12	A0	
CMD23	CS1 L*	Not Used	
CMD24	RAS*	RAS*	
CMD25	ODT L	Not Used	
CMD26	A6	A7	
CMD27	Not Used	CKE H	
CMD28	RST	RST	
CMD29	A14	A13	
CMD30	A15	BA2	

# 8. MEMORY DECOUPLING CAPS

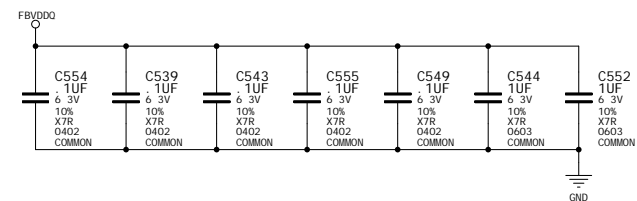
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



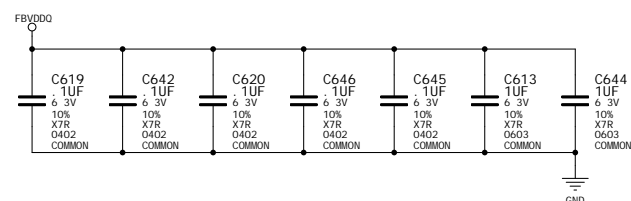
DECOUPLING CAPS FOR ONE MEMORY OF PARTION C LOWER BITS 0-15



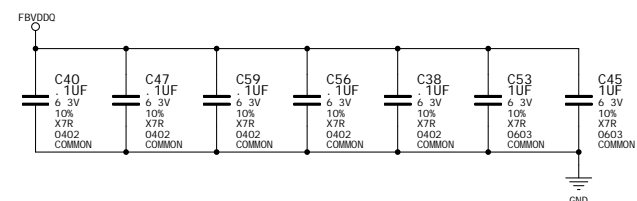
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



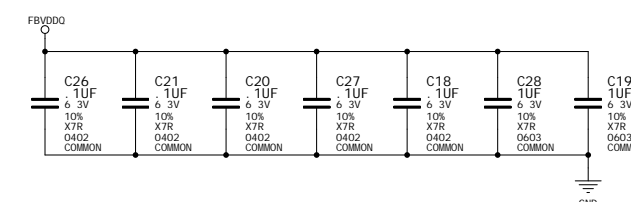
DECOUPLING CAPS FOR ONE MEMORY OF PARTION C LOWER BITS 16-31



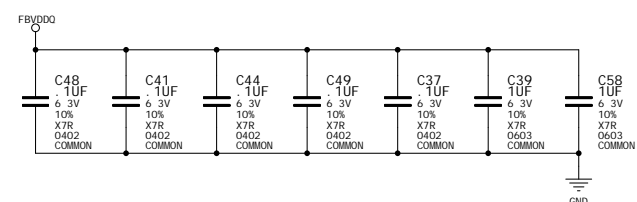
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 32-47



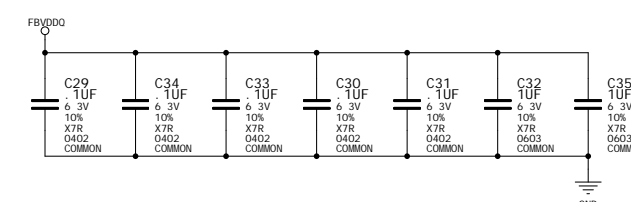
DECOUPLING CAPS FOR ONE MEMORY OF PARTION C UPPER BITS 32-47



DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 48-63



DECOUPLING CAPS FOR ONE MEMORY OF PARTION C UPPER BITS 48-63



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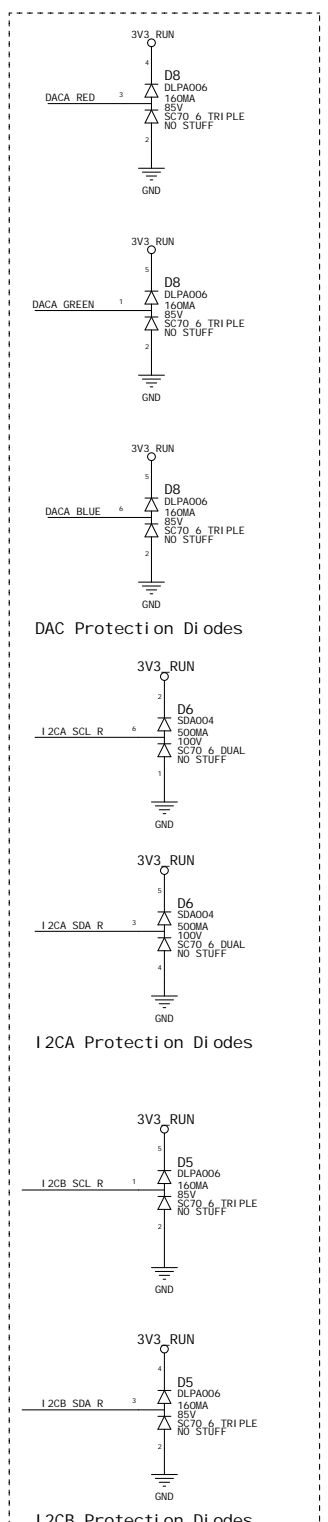
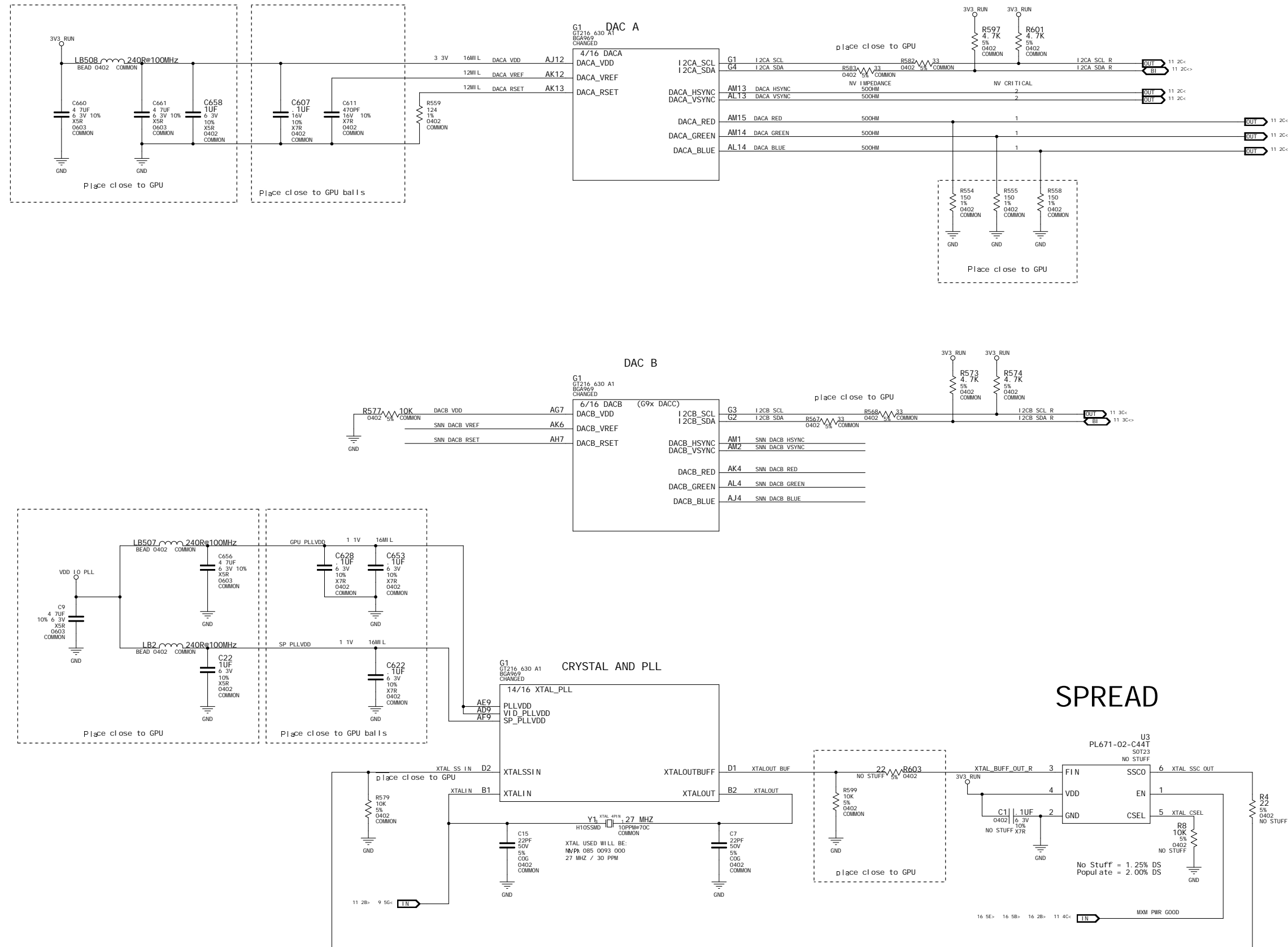


ASSEMBLY	P699 B00 SKUS01 GT216 950 MXM3 0 TYPE A 1024MB @pc3 64Mx16
PAGE DETAIL	Memory Decoupling Caps

NV_PN	600-50699-0501-100 D		
ID	p699	PAGE	8 OF 17
NAME	tlanger	DATE	15-APR-2009

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# 9. DAC\_A, DAC\_B, SPREAD, PLL, CRYSTAL



NV NET NAME	NV IMPEDANCE	NV CRITICAL NET
XTALOUT	500HM	1
XTALIN	500HM	1
XTALOUT BUF	500HM	2
XTAL SSC OUT	500HM	2

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NV_PN	600-50699-0501-100 D	
ID	p699	PAGE 9 OF 17
NAME	tlanger	DATE 15-APR-2009



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