ACX502BMU-7

Transflective 3.5 Type Polysilicon TFT LCD with Backlight

Revision Record

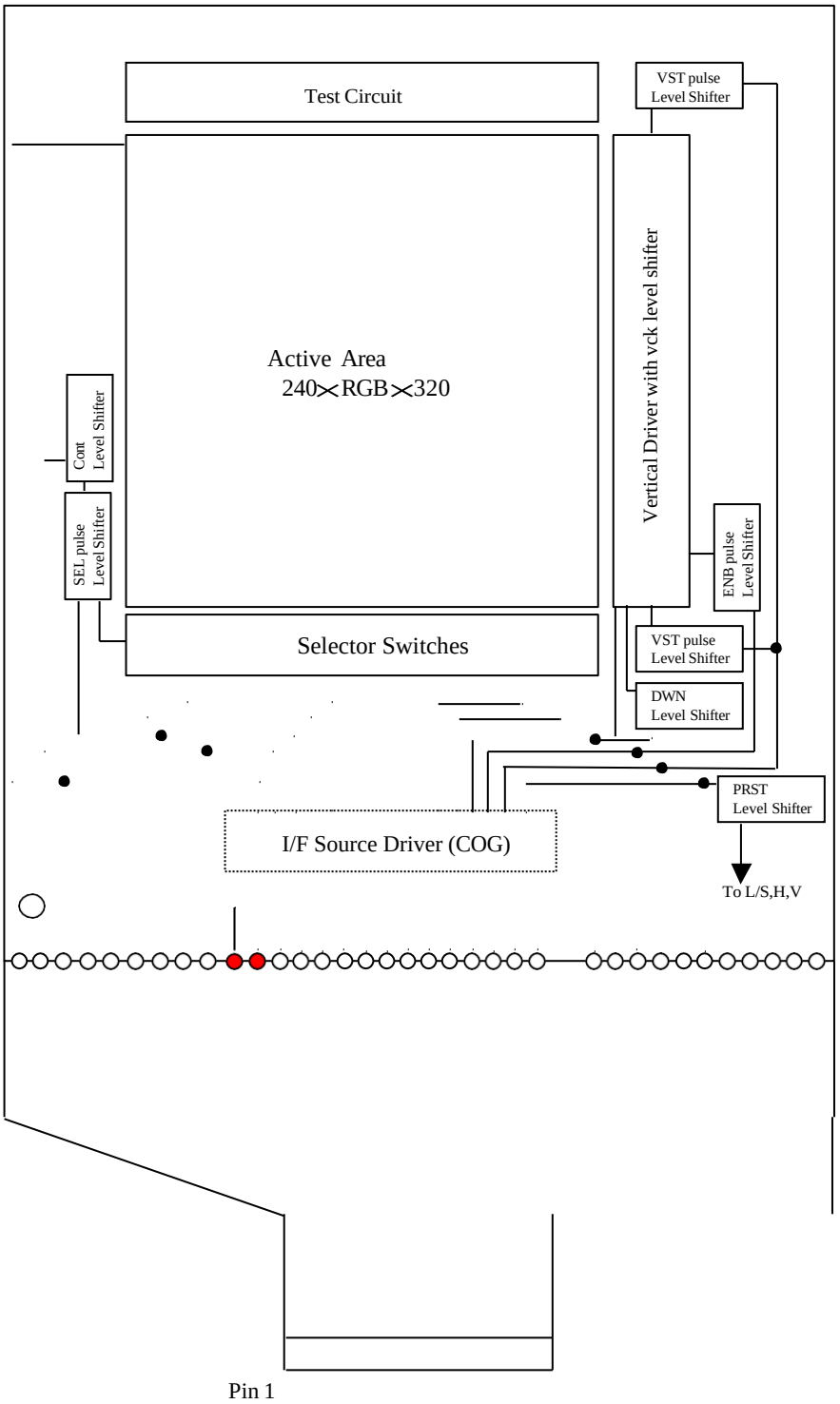
Tentative Ver 0.0	19-Dec-02	Tentative Release
Tentative Ver 1.0	8-Jan-03	VDD2 Specification,Backlight
		specification
Tentative Ver 2.0	9-Jan-03	Discruption of Function
		Delete HSYNC and VSYNC
Tentative Ver 3.0	21-Jan-03	Defect Limitation
		Pin Description
		Leak Current of Logic Defined
		Uniformity revised
Tentative Ver 4.0	3-Mar-03	Color Specification(p25)
Tentative Ver 5.0		VVSS2 revised
Tentative Ver.6.0	31-Mar-03	Optical Spec revised
Tentative Ver.7.0	4-Apr-03	Defect & LED spec. revised(p14,26~28)
Tentative Ver.8.0	28-Apr-03	Reliability test condition
Tentative Ver.9	30-Apr-03	Vcom center added
Final Ver.1	12-May-03	White spec revised
		Noise spec

Front Page

See Other File

1. Block Diagram

The panel block diagram is as shown below.

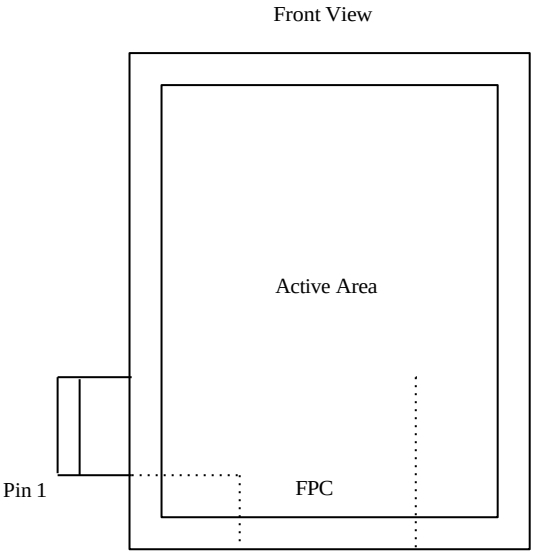


2. Absolute Maximum Ratings (VSS=0V)

•H driver power supply voltage	HVDD	-1.0 to +10.5 V
•V driver power supply voltage	VVDD	-1.0 to +10.5 V
•H driver power supply voltage	HVSS3	-7.5 to +1.0 V
•V driver power supply voltage	VVSS2	-7.5 to +1.0 V
•Output voltage	VCOM-OC,VBS	-0.3 to VDD2+0.3 V
•Input voltage	DENB,MCK,PCI,RST,VCOM-IC, U/D,L/R	-0.3 to VDD1+0.3 V
•Source Driver logic supply voltage	VDD1	-0.3 to +4.6 V
•Source Driver analog supply voltage	VDD2	-0.3 to +6.0 V
•Data signal input pin voltage	R00-05,G00-05,B00-05	-0.3 to VDD1+0.3 V
•Operating Temperature	Topr	0 to 40 C
•Storage Temperature	Tstg	-20 to 60 C
•Back light current(@1LED)	Ibl	30 mA
•LED input voltage	LED(R+), LED(R-), LED(L+), LED(L-)	4.0 V
•T/P input voltage	yU,xR,yL,xL	7.0 V

3. Pin Location of Panel Block

The FPC pin assignment is described in the next page. The location of Pin 1 is shown below.



4. Pin Description of FPC Connector

Pin No.	Name	I/O	Function		Pin No.	Name	I/O	Function
1	GND				31	G02	I	Data Bit Input
2	yU	I	Lower electrode Y		32	G03	I	Data Bit Input
3	xR	I	Lower electrode X		33	G04	I	Data Bit Input
4	yL	I	Upper electrode Y		34	G05	I	Data Bit Input
5	xL	I	Upper electrode X		35	GND		
6	VSS		GND		36	R00	I	Data Bit Input
7	VCOM-IC	I	VCOM Signal Input for LCD Panel		37	R01	I	Data Bit Input
8	VCOM-IC	I	VCOM Signal Input for LCD Panel		38	R02	I	Data Bit Input
9	VSS		GND		39	R03	I	Data Bit Input
10	HVSS3		-3V Input (LCD Panel Power Source)		40	R04	I	Data Bit Input
11	HVDD		9V Input (LCD Panel Power Source)		41	R05	I	Data Bit Input
12	VCOM-OC	O	VCOM Signal of IC Output		42	GND		
13	VCOM-OC	O	VCOM Signal of IC Output		43	VDD1		3V Input (IC Power Source)
14	VBS	O	VBS Output		44	VSS1		GND
15	VSS2		GND		45	VSS1		GND
16	VDD2		5V Input (IC Power Source)		46	MCK	I	Master Clock Input
17	RST	I	Reset Input		47	VSS1		GND
18	NC		NC		48	DENB	I	Data Enable Signal Input
19	VSS2		GND		49	PCI	I	Power Control Input
20	VDD1		3V Input (IC Power Source)		50	TEST1	I	Connect to GND
21	VSS1		GND		51	TEST2	I	Connect to GND
22	B00	I	Data Bit Input		52	PINV	I	Up/down and right/left inversion
23	B01	I	Data Bit Input		53	VSS2		GND
24	B02	I	Data Bit Input		54	VDD2		5V Input (IC Power Source)
25	B03	I	Data Bit Input		55	PCO	O	Power Control Output
26	B04	I	Data Bit Input		56	VVDD		9V Input (LCD Panel Power Source)
27	B05	I	Data Bit Input		57	VVSS2		-6.5V Input (LCD Panel Power Source)
28	GND				58	LED(-)	I	Cathode of LED
29	G00	I	Data Bit Input		59	LED(+)	I	Anode of LED
30	G01	I	Data Bit Input		60	VVSS		GND

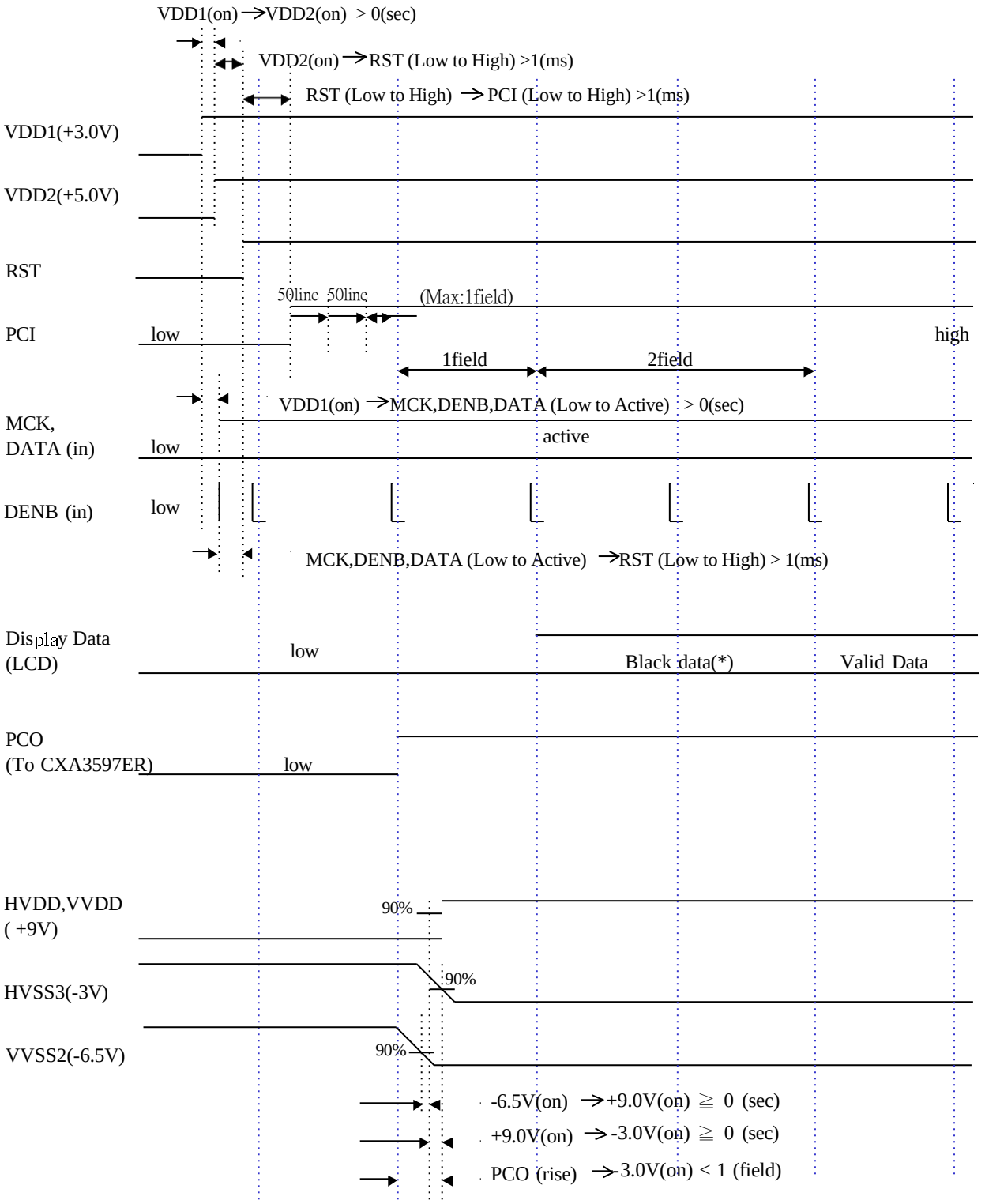
5. Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit	Pin/Remark
Power supply 1	HVDD	8.5	9.0	9.5	V	HVDD
Power supply 2	VVDD	8.5	9.0	9.5	V	VVDD
Power supply 3	HVSS3	-3.5	-3.0	-2.5	V	HVSS3
Power supply 4	VVSS2	-6.5	-6.0	-5.7	V	VVSS2
Power supply 5	VDD1	2.7	3.0	3.6	V	VDD1
Power supply 6	VDD2	4.75	5.00	5.25	V	VDD2(*1)
Ripple voltage	Vrp	—	—	100	mVpp	HVDD,VVDD,HVSS3,VVSS2, VDD1,VDD2(*2)
Data/pulse input (Low)	VIL	—	—	0.3VDD1	V	All data input pins
Data/pulse input (High)	VIH	0.7VDD1	—	—	V	
Pull Down Resister	Rpd	1M	3.8M	6.7M	Ohm	All data input pins, DENB, MCK, PINV, PCI, RST, TEST1, TEST2
Pull Up Resister	Rpu	50K	250K	500K	Ohm	RST
Common voltage center	VcomC	1.70	2.05	2.30	V	VCOM
Common voltage swing	VcomA	4.75	5.00	5.25	V	VCOM
Vertical frequency	fv	50	60	65	Hz	
Horizontal frequency	fh	16.8	20.16	21.84	kHZ	
CLK frequency	fdot	4.57	5.48	5.94	MHz	MCK
CLK pulse width	tclk	168.4	182.5	218.8	nsec	MCK
CLK high pulse width	tch	20	—	—	nsec	MCK
CLK low pulse width	tcl	20	—	—	nsec	MCK
Data setup time	tds	20	—	—	nsec	DATA
Data hold time	tdh	20	—	—	nsec	DATA
DENB setup time	tdes	20	—	—	nsec	DENB
DENB hold time	tdeh	20	—	—	nsec	
PCI setup time	tpcs	20	—	—	nsec	PCI
PCI hold time	tpch	20	—	—	nsec	
Horizontal Blanking Time	HBLK	-	32	-	clk	DENB
Vertical Blanking Time	VBLK	-	16	-	line	DENB

(*1) : The gamma correction voltage is set to achieve the optimum at VDD2=5.0V. Use the voltage at a level as close to 5.0V as possible.

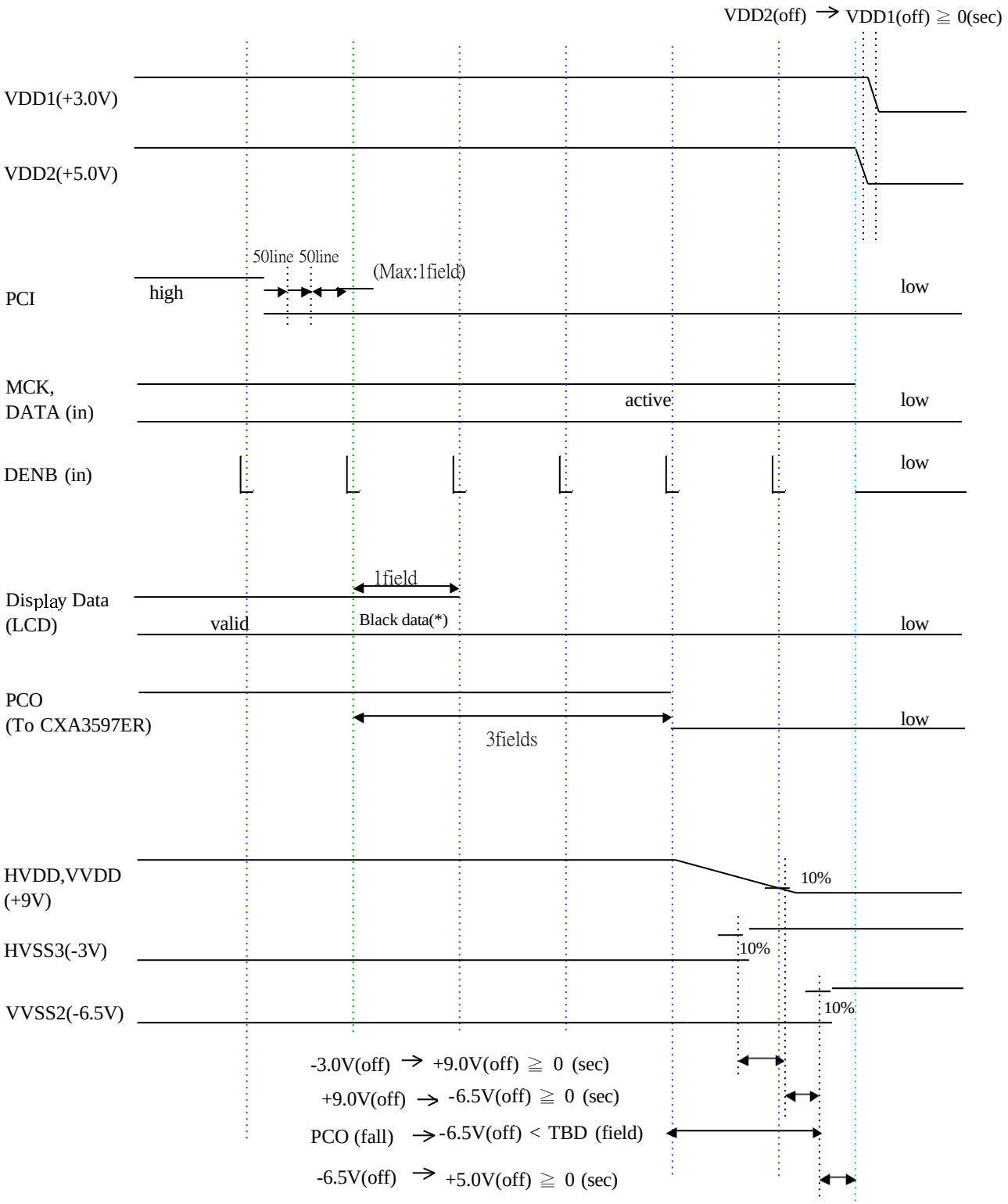
(*2) : VDD2 is analog voltage supply therefore use as less ripple as possible.

6. Power ON Sequence



(*)Driver IC outputs black data automatically.

7. Power OFF Sequence



(*)Driver IC outputs black data automatically.