Integrated Circuit Systems, Inc.

ICS91309I
Preliminary Product Preview

High Performance Communication Buffer

General Description

The **ICS91309I** is a high performance, low skew, low jitter zero delay buffer. It uses a phase lock loop (PLL) technology to align, in both phase and frequency, the REF input with the CLKOUT signal. It is designed to distribute high speed clocks in communication systems operating at speeds from 10 to 133 MHz.

The **ICS91309I** provides synchronization between the input and output. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than +/- 350 pS, the part acts as a zero delay buffer.

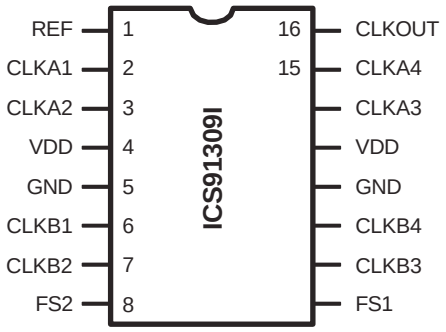
ICS91309I has two banks of four outputs controlled by two address lines. Depending on the selected address line, bank B or both banks can be put in a tri-state mode. In this mode, the PLL is still running and only the output buffers are put in a high impedance mode. The test mode shuts off the PLL and connects the input directly to the output buffers (see table below for functionality).

ICS91309I comes in a 16-pin 150 mil SOIC, SSOP or 4.40mm TSSOP package. In the absence of REF input, the device will enter a powerdown mode. In this mode, the PLL is turned off and the output buffers are pulled low. Power down mode provides the lowest power consumption for a standby condition.

Features

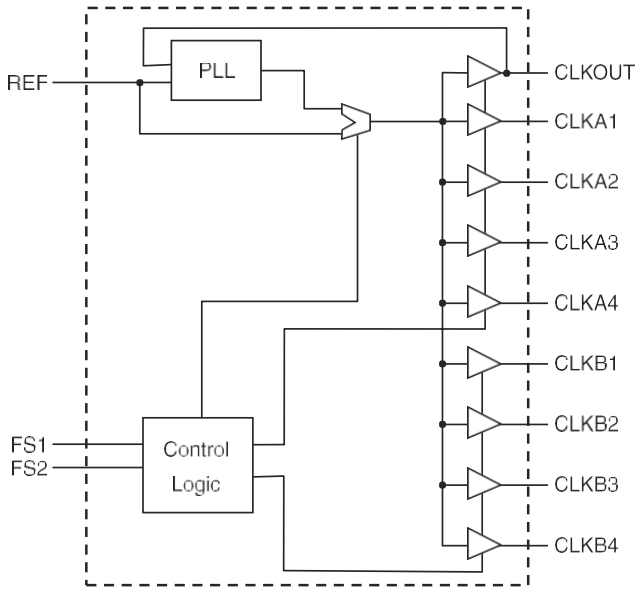
- Zero input - output delay
- Frequency range 10 - 133 MHz (3.3V)
- 5V tolerant input REF
- High loop filter bandwidth ideal for Spread Spectrum applications.
- Less than 125 ps cycle to cycle Jitter
- Skew controlled outputs
- Available in 16 pin, 150 mil SSOP, SOIC & 4.40mm TSSOP packages
- Skew: Group-to-Group: <215 ps
- Skew within Group: <100 ps
- Industrial temperature range: -40°C to +85°C

Pin Configuration



16 pin SSOP, SOIC & TSSOP

Block Diagram



Functionality

FS2	FS1	CLKA(1:4)	CLKB(1:4)	CLKOUT	Ouput Source	PLL Shutdown
0	0	Tristate	Tristate	Driven	PLL	N
0	1	Driven	Tristate	Driven	PLL	N
1	0	PLL Bypass Mode	PLL Bypass Mode	PLL Bypass Mode	REF	Y
1	1	Driven	Driven	Driven	PLL	N

0770A—04/30/03

PRODUCT PREVIEW documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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High Performance Communication Buffer

General Description

The **ICS91309I** is a high performance, low skew, low jitter zero delay buffer designed to distribute high speed clocks. It uses IDT's 3rd generation FAST PLL technology to align, in both phase and frequency, the REF input with the CLKOUT signal. It is designed to distribute high speed clocks in communication systems operating at speeds from 10 to 133 MHz.

The **ICS91309I** provides synchronization between the input and output. The synchronization is established via CLKOUT and lock time is less than 1 ms. Phase error between the input and output is less than +/- 350 pS, the part acts as a zero delay buffer.

ICS91309I has two banks of four outputs controlled by two address lines. Depending on the selected address line, bank B or both banks can be put in a tri-state mode. In this mode, the PLL is still running and only the output buffers are tri-stated. Alternatively, bank B can be used to shuts off the PLL and connects the input directly to the output buffers (see table below for functionality).

ICS91309I comes in a 16-pin 150 mil SOIC, SSOP or 4.40mm TSSOP package. In the absence of REF input, the device will enter a powerdown mode. In this mode, the PLL is turned off and the output buffers are pulled low, which effectively minimizes the lowest power consumption for a standby condition.

Features

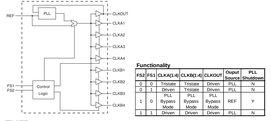
- Zero input - output delay
- Frequency range 10 - 133 MHz (3.3V)
- 5V tolerant input REF
- Jitter filter for wider bandwidth ideal for Spread Spectrum applications
- Less than 125 ps cycle to cycle Jitter
- Skew controlled outputs
- Available in 16 pin, 150 mil SSOP, SOIC & 4.40mm TSSOP packages
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0	0	Tristate	Tristate	Driven	PLL	N
0	1	Driven	Tristate	Driven	PLL	N
1	0	Bypass Mode	Bypass Mode	Bypass Mode	REF	Y
1	1	Driven	Driven	Driven	PLL	N

07/04--060903

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Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	REF[1]	IN	Input reference frequency, 5V tolerant input
2	CLKA1[2]	OUT	Buffered clock output, Bank A
3	CLKA2[2]	OUT	Buffered clock output, Bank A
4	VDD	PWR	Power Supply
5	GND	PWR	Ground
6	CLKB1[2]	OUT	Buffered clock output, Bank B
7	CLKB2[2]	OUT	Buffered clock output, Bank B
8	FS2[3]	IN	Function select input, bit 2
9	FS1[3]	IN	Function select input, bit 1
10	CLKB3[2]	OUT	Buffered clock output, Bank B
11	CLKB4[2]	OUT	Buffered clock output, Bank B
12	GND	PWR	Ground
13	VDD	PWR	Power Supply
14	CLKA3[2]	OUT	Buffered clock output, Bank A
15	CLKA4[2]	OUT	Buffered clock output, Bank A
16	CLKOUT[2]	OUT	Buffered clock output, internal feedback

Notes:

1. Weak pull-down
2. Weak pull-down on all outputs
3. Weak pull-ups on these inputs

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7	CLKB2[2]	OUT	Buffered clock output, Bank B
8	FS2[3]	IN	Function select input, bit 2
9	FS1[3]	IN	Function select input, bit 1
10	CLKB3[2]	OUT	Buffered clock output, Bank B
11	CLKB4[2]	OUT	Buffered clock output, Bank B
12	GND	PWR	Ground
13	VDD	PWR	Power Supply
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15	CLKA4[2]	OUT	Buffered clock output, Bank A
16	CLKOUT[2]	OUT	Buffered clock output, internal feedback

Notes:

1. Weak pull-down
2. Weak pull-down on all outputs
3. Weak pull-ups on these inputs

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs (Except REF) . . . . . GND –0.5 V to V_{DD} + 0.5 V
Logic Input REF . . . . . GND –0.5 V to GND + 5.5 V
Ambient Operating Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input & Supply

T_A = -40 - 85°C; Supply Voltage V_{DD} = 3.3 V +/-10%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	250	uA
Input Low Current	I_{IL}	V_{IN} = 0 V		19	100	uA
Output High Voltage	Vo_H	Io_H = -12 mA	2.4			V
Output Low Voltage	Vo_L	Io_L = 12 mA			0.4	V
Operating Supply Current	I_{DD}	Outputs Unloaded; REF = 66 MHz		30	45	mA
Powerdown Current	I_{DD}	REF = 0 Mhz		0.3	50	uA
Input Frequency	F_i		10		133	MHz
Input Capacitance[1]	C_{IN}				5	pF

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Notes:
1. Guaranteed by design and characterization, not 100% tested in production.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
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Input Frequency	F_i		10		133	MHz
Input Capacitance[1]	C_{IN}				5	pF

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Electrical Characteristics - Outputs

T_A = -40 - 85°C; V_{DD} = 3.3 V +/-10%; C_L = 30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Rise Time[1]	t_r	Measure between 0.8 V and 2.0 V		1.2	2	ns
Fall Time[1]	t_f	Measure between 2.0 V and 0.8 V		1.2	2	ns
PLL Lock Time[1]	T_{LOCK}	Stable V_{DD}, valid clock on REF			1	mS
Output Frequency	f_1	C_L = 30 pF	10		100	MHz
	f_1	C_L = 10 pF	10		133	MHz
Duty Cycle[1]	Dt1	Measured at 1.4 V, Fout = 66.7 MHz	40	50	60	%
	Dt2	Measured at V_{DD}/2, Fout < 50.0 MHz	45	50	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	Measured at 66.7 MHz, loaded outputs			125	ps
Jitter, Absolute[1]	Tjabs	10,000 cycles, C_L = 30 pF	-100	70	100	ps
Jitter, 1-Sigma[1]	Tj1s	10,000 cycles, C_L = 30 pF		14	30	ps
Skew, Group-to-Group[1]	Tsk	Measured at 1.4 V			215	ps
Skew, Output-to-Output[1]	Tsk	Measured at 1.4 V, within a group			100	ps
Skew, Device-to-Device[1]	Tdsk-Tdsk	Measured at V_{DD}/2,on CLKOUT pins			700	ps
Delay, Input-to-Output[1]	Dr1	Measured at 1.4 V			700	ps

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Electrical Characteristics - Outputs

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Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Rise Time[1]	t_r	Measure between 0.8 V and 2.0 V		1.2	2	ns
Fall Time[1]	t_f	Measure between 2.0 V and 0.8 V		1.2	2	ns
PLL Lock Time[1]	T_{LOCK}	Stable V_{DD}, valid clock on REF			1	mS
Output Frequency	f_1	C_L = 30 pF	10		100	MHz
	f_1	C_L = 10 pF	10		133	MHz
Duty Cycle[1]	Dt1	Measured at 1.4 V, Fout = 66.7 MHz	40	50	60	%
	Dt2	Measured at V_{DD}/2, Fout < 50.0 MHz	45	50	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	Measured at 66.7 MHz, loaded outputs			125	ps
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Skew, Device-to-Device[1]	Tdsk-Tdsk	Measured at V_{DD}/2,on CLKOUT pins			700	ps
Delay, Input-to-Output[1]	Dr1	Measured at 1.4 V			700	ps

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SUBJECT TO CHANGE
PRELIMINARY
PRODUCT
CHARACTERIZATION

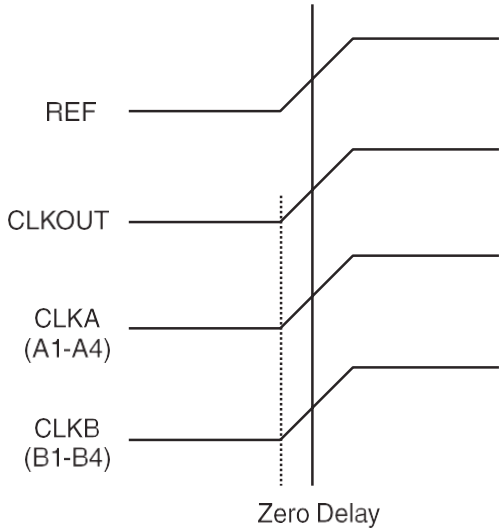
Output to Output Skew

The skew between CLKOUT and the CLKA/B outputs is not dynamically adjusted by the PLL. Since CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF to CLKOUT. If all outputs are equally loaded, zero phase difference will maintained from REF to all outputs.

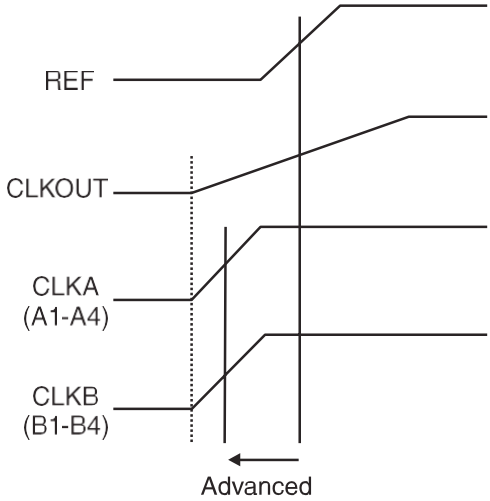
If applications requiring zero output-output skew, all the outputs must equally loaded.

If the CLKA/B outputs are less loaded than CLKOUT, CLKA/B outputs will lead it; and if the CLKA/B is more loaded than CLKOUT, CLKA/B will lag the CLKOUT.

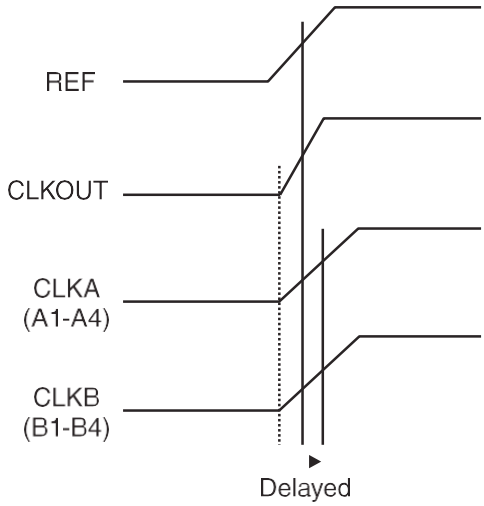
Since the CLKOUT and the CLKA/B outputs are identical, they all start at the same time, but different loads cause them to have different rise times and different times crossing the measurement thresholds.



REF input and all outputs loaded Equally



REF input and CLKA/B outputs loaded equally, with CLKOUT loaded More.



REF input and CLKA/B outputs loaded equally, with CLKOUT loaded Less.

Timing diagrams with different loading configurations

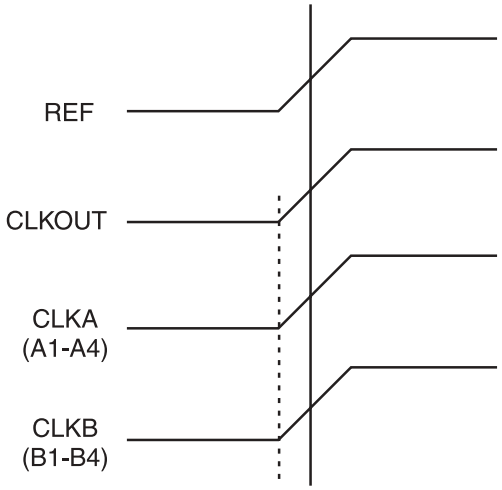
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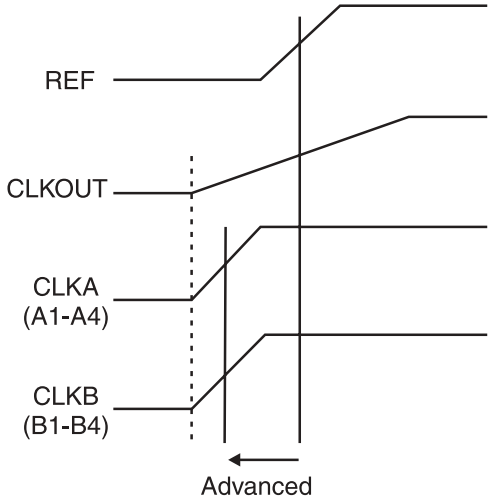
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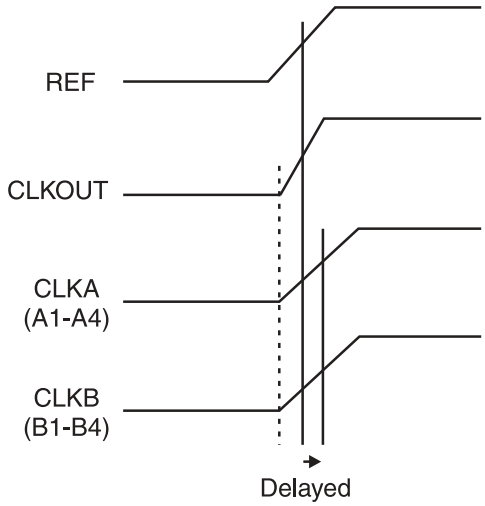
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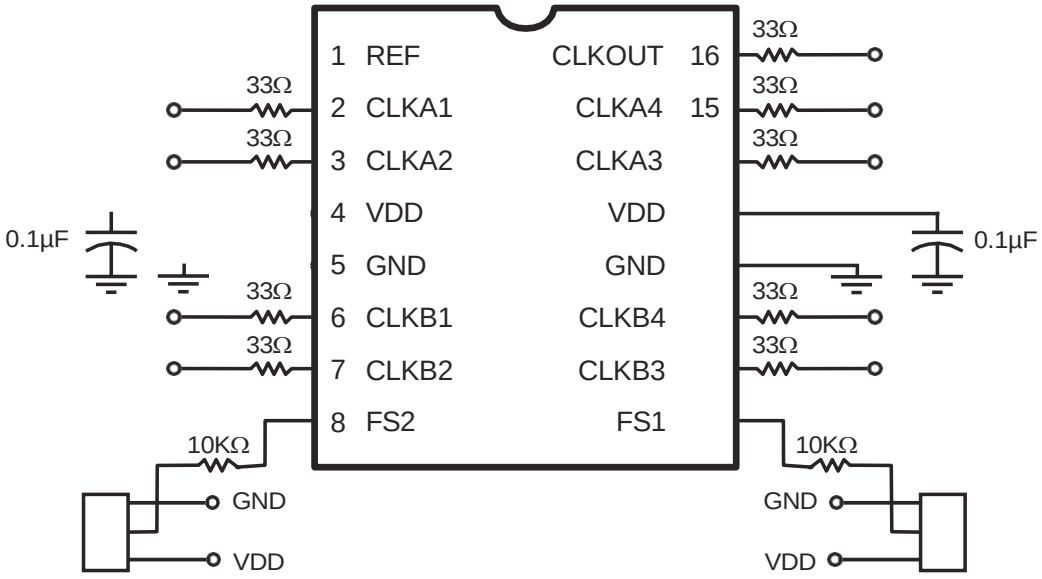


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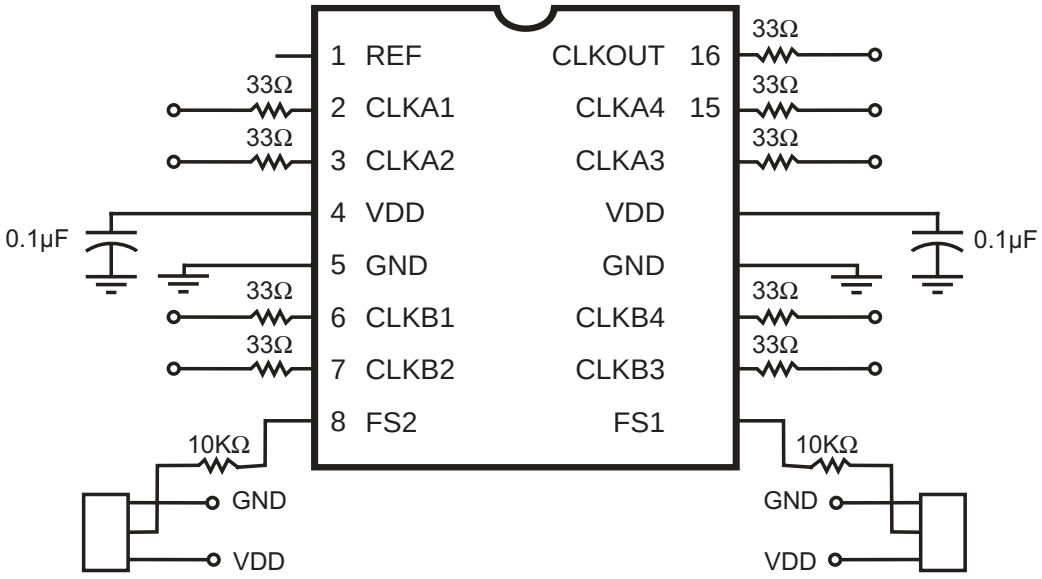
Application Suggestion:

ICS91309I is a mixed analog/digital product. The analog portion of the PLL is very sensitive to any random noise generated by charging or discharging of internal or external capacitor on the power supply pins. This type of noise will cause excess jitter to the outputs of **ICS91309I**. Below is a recommended lay out to alleviate any addition noise. For additional information on FT. layout, please refer to our AN07. The 0.1 uF capacitors should be connected as close as possible to power pins (4 & 13). An Isolated power plane with a 2.2 uF capacitor to ground will enhance the power line stability.



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