Agilex™ 7 LVDS SERDES User Guide

M-Series

Updated for Quartus® Prime Design Suite: **24.2**

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1. Agilex™ 7 M-Series LVDS SERDES Overview

The Agilex™ 7 M-Series I/O system includes three types of I/O interfaces: general purpose I/Os (GPIO-B), Secure Device Manager (SDM) I/O, and Hard Processor System (HPS) I/O. Each I/O interface caters to different interfacing requirements.

M-Series devices support LVDS serializer/deserializer (SERDES) through True Differential Signaling and SLVS-400 I/O standards in the GPIO-B banks. The true differential I/Os are capable of supporting LVDS interfaces, including subsets such as:

- RSDS
- Mini-LVDS
- SLVS
- Any differential I/O standards using equivalent electrical specifications

M-Series devices support SERDES in all GPIO-B banks with the following features:

- Configurable transmitter or receiver on all I/O pins
- Serialize and deserialize functions up to 1.6 Gbps.
- Clock data recovery (CDR) function on specific differential channel
- Configurable 100 Ω differential on-chip termination (OCT R_D)
- Serializer or deserializer factors of 4 and 8(1)
- I/O standards support for the LVDS SERDES:
  - Transmitter—True Differential Signaling I/O standard at 1.3 V
  - Receiver:
    - DPA mode—True Differential Signaling and SLVS-400 I/O standards
    - Non-DPA mode—True Differential Signaling I/O standard only

Related Information

- Intel Agilex® 7 General-Purpose I/O User Guide: M-Series
  Provides more information about the GPIO-B, HPS, and SDM I/Os.
- Supported I/O Standards for GPIO-B Banks, Intel Agilex® 7 General-Purpose I/O User Guide: M-Series
- Agilex 7 FPGAs and SoCs Device Data Sheet: M-Series
  Provides the specifications for the maximum data rate of the transmitter, the receiver in DPA, non-DPA, and soft-CDR modes, and the LVDS SERDES Intel® FPGA IP.

(1) Serialization factor of 8 is available only in M-Series FPGAs production devices.

- Agilex 7 LVDS SERDES User Guide: M-Series
  Get the latest and previous versions of this user guide. If an IP or software version is not listed, the user guide for the previous IP or software version applies.

1.1. LVDS SERDES Usage Modes

You can use the M-Series LVDS SERDES through the LVDS SERDES Intel® FPGA IP. The LVDS SERDES IP supports four SERDES functional modes.

Table 1. Summary of the M-Series LVDS SERDES Usage Modes

All usage modes in this table support SERDES factors of 4 and 8.

Functional Mode	Description
Transmitter (**TX**)	• The SERDES block acts as a serializer. • A PLL generates these signals: — `fast_clock` — `load_enable`
Non-DPA receiver (**RX Non-DPA**)	• The SERDES block acts as a deserializer that bypasses the DPA and DPA-FIFO. • A PLL generates the `fast_clock` signal. • The SERDES captures the incoming data at the bit slip with the `fast_clock` signal. Therefore, you must ensure the correct clock–data alignment.
DPA-FIFO receiver (**RX DPA-FIFO**)	• The SERDES block acts as a deserializer that uses the DPA block. • The DPA block uses a set of eight DPA clocks to select the optimal phase for sampling data. — The DPA clocks run at the `fast_clock` frequency with each clock phase-shifted 45° apart. — The DPA-FIFO, a circular buffer, samples the incoming data with the selected DPA clock and forwards the data to LVDS clock domain. — The bit slip circuitry then samples the data and inserts latencies to realign the data to match the desired word boundary of the deserialized data.
Soft-CDR receiver (**RX Soft-CDR**)	• The LVDS SERDES IP forwards these clocks: — The optimal DPA clock (DPACLK) into the LVDS clock domain as the `fast_clock` signal. — The `rx_divfwdclk`, produced by the local clock generator, to the device core. • Each bank has only 12 soft-CDR channels available. Refer to the device pin-out files to determine which pin pairs can support soft-CDR channels in each bank.

Related Information

Agilex 7 Device Pin-Out Files
Each device pinout file lists the available GPIO-B banks for each package, the GPIO-B banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

2. Agilex 7 M-Series LVDS SERDES Architecture

Each GPIO-B bank in M-Series devices consists of two sub-banks. Each sub-bank contains its own V_{CCIO_PIO} and PLL. Each LVDS SERDES pair has its own dynamic phase alignment (DPA) and SERDES circuitry blocks.

You can configure each SERDES channel as a transmitter or a receiver.

Table 2. Differential Pairs and Channel Mode Support in Each Bank and Sub-Bank

This table lists the number of SERDES channels supported. Refer to the device pin-out files for the exact location of the SERDES and Soft-CDR pins.

Total Transmitter or Receiver Pairs Per Bank	Channel Mode	Maximum Pairs Per Sub-Bank	
		Top Index Sub-Bank	Bottom Index Sub-Bank
47(2)	Transmitter	24	24
	DPA	24	24
	Non-DPA	24	24
	Soft-CDR	4	8

Related Information

- Agilex 7 Device Pin-Out Files
  Each device pinout file lists the available GPIO-B banks for each package, the GPIO-B banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.
- I/O PLLs Driving LVDS SERDES Transmitter and Receiver Channels on page 61

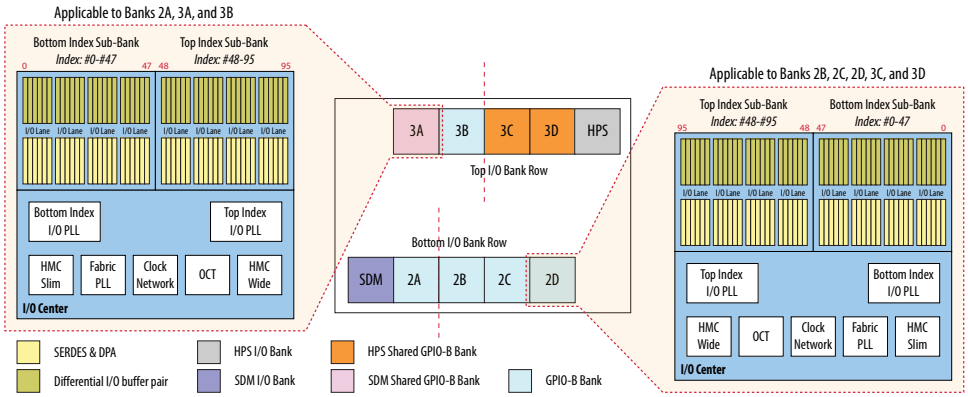
(2) One LVDS SERDES pair is used for the reference clock.

2.1. Agilex 7 M-Series GPIO-B Banks, SERDES, and DPA Locations

The GPIO-B banks are located at the top and bottom I/O bank rows.

Figure 1. M-Series I/O Bank Structure (Die Top View)

This figure shows the GPIO-B bank structure of the M-Series device. The figure shows the view of the die as shown in the Quartus® Prime **Chip Planner**. In the **Pin Planner**, this corresponds to the "Bottom View". Different device packages have different number of GPIO-B banks. Refer to the device pin-out files for available GPIO-B banks and the locations of the SDM shared and HPS shared GPIO-B banks for each device package.



Related Information

Agilex 7 Device Pin-Out Files

Each device pinout file lists the available GPIO-B banks for each package, the GPIO-B banks shared with the HPS and SDM, the DQ groups, the pin functions, and the pin locations.

2.2. SERDES Blocks, Modes, and Clock Domains

Figure 2. SERDES Circuitry

This figure shows a transmitter and receiver block diagram for the SERDES circuitry with the interface signals of the transmitter and receiver data paths. The figure shows a transmitter and a receiver sharing an I/O PLL as they are in the same sub-bank and using the same I/O PLL resource. In single data rate (SDR) and double data rate (DDR) modes, the data widths are 1 and 2 bits, respectively.

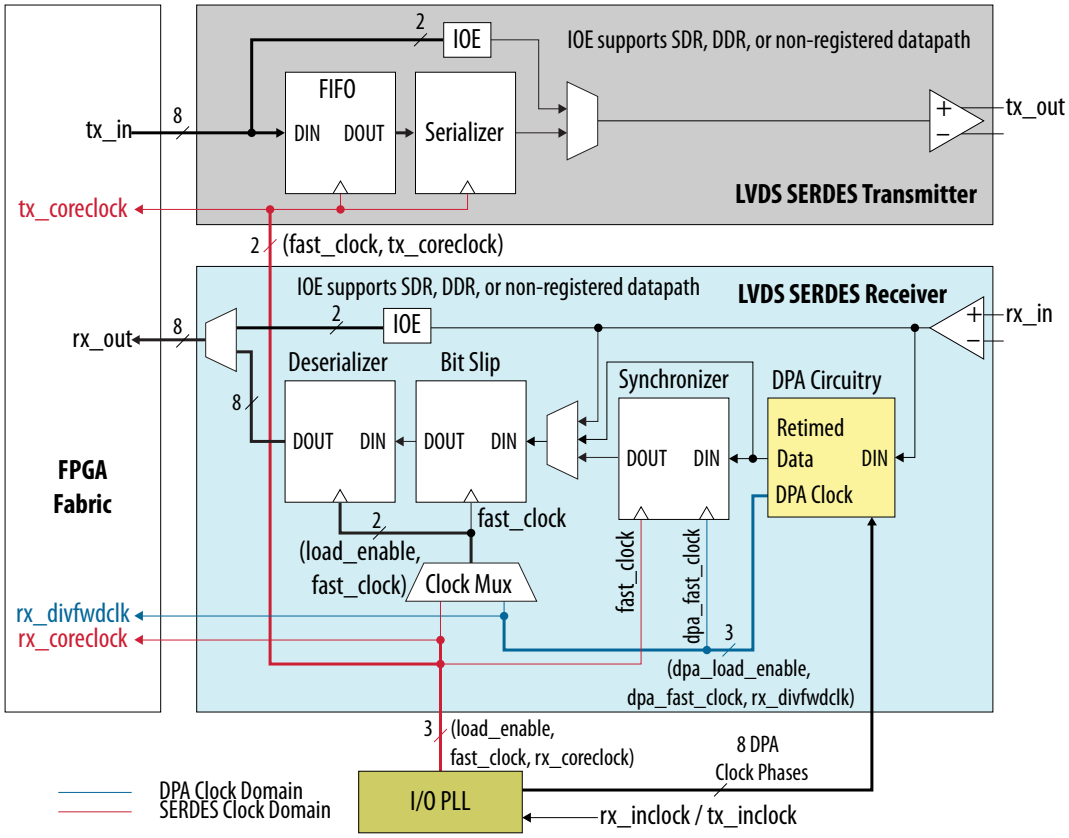


Table 3. Supported Modes, Blocks, and Clocks for the Data Paths

Data Path	Mode	Block	Clock Domain
Transmitter	**TX**	Serializer	SERDES clock domain
Receiver	**DPA-FIFO**	DPA	DPA clock domain
		Synchronizer	DPA-SERDES clock domain crossing
		Bit Slip	SERDES clock domain
		Deserializer	SERDES clock domain
	Non-DPA	DPA	Not used
		Synchronizer	Not used
		Bit Slip	SERDES clock domain
		Deserializer	SERDES clock domain

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Data Path	Mode	Block	Clock Domain
	Soft-CDR	DPA	DPA clock domain
		Bit Slip	DPA clock domain
		Deserializer	DPA clock domain

3. Agilex 7 M-Series LVDS SERDES Transmitter

The M-Series LVDS SERDES transmitters are dedicated circuitries.

Each dedicated transmitter circuitry consists of:

- A transmitter buffer
- A serializer
- PLL shared with other SERDES within the same I/O bank

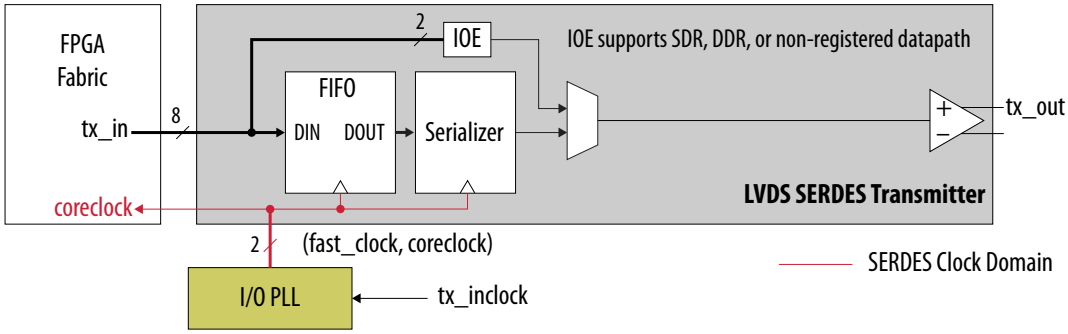
Table 4. Dedicated Circuitry and Features of the LVDS SERDES Transmitter

Dedicated Circuitry / Feature	Description
Differential I/O buffer	Supports True Differential Signaling I/O standard, which is compatible with LVDS, RSDS, SLVS, and Mini-LVDS.
Serializer (3)	4-bit or 8-bit(4) wide serializer
Phase-locked loops (PLLs)	Clocks the registers
Programmable V_{OD}	Adjusts the output voltage swing
Programmable pre-emphasis	Boosts output current

3.1. LVDS SERDES Transmitter Blocks

In the M-Series LVDS SERDES transmitter, the serializer receives up to 8 bits(4) wide parallel data from the FPGA fabric.

Figure 3. LVDS SERDES Transmitter



(3) Serialization factors of 1 and 2 are supported through the GPIO Intel FPGA IP.

(4) Serialization factor of 8 is available only in M-Series FPGAs production devices.

- The serializer clocks the data into the registers and serializes the data using a multiplexer.
- The I/O PLL that drives the data to the differential buffer clocks the shift registers.
- The multiplexer transmits the MSB of the parallel data first.

Note: The PLL that drives the SERDES channel must operate in integer PLL mode.

3.2. Serializer

The serializer consists of two sets of registers. The first set of registers (FIFO) captures the parallel data from the core using the LVDS fast clock and then transfers the data to the serializer block. The MSB of the serializer feeds the LVDS SERDES output buffer. Consequently, higher order bits precede lower order bits in the output bitstream.

Figure 4. LVDS SERDES ×8 Serializer Bit Position

This figure shows the waveforms specific to the serialization factor of 8. These are functional waveforms and do not convey timing information.

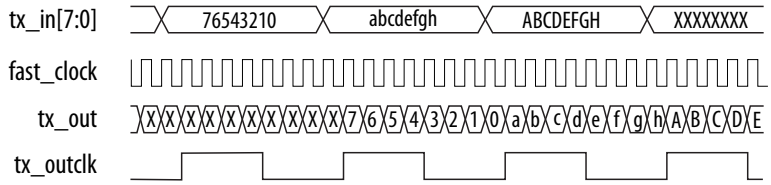


Table 5. LVDS SERDES Serializer Signals

Signal	Description
`tx_in[7:0]`	Data for serialization (Supported serialization factors: 4 and 8[5])
`fast_clock`	Clock for the transmitter
`tx_out`	LVDS SERDES output data stream

3.2.1. Serializer Bypass for DDR and SDR Operations

The I/O element (IOE) contains two data output registers. Each data output register can operate in double data rate (DDR) or single data rate (SDR) mode. Use the GPIO Intel FPGA IP to bypass the serializer and operate in DDR and SDR modes.

(5) Serialization factor of 8 is available only in M-Series FPGAs production devices.

Figure 5. Serializer Bypass

This figure shows the serializer bypass path.

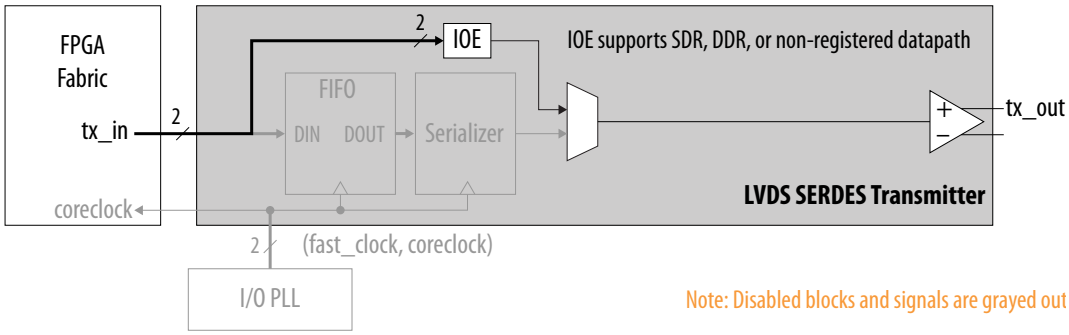


Table 6. SDR and DDR Transmitter Modes

Mode	Description
SDR (×1)	• The IOE data width is 1 bit. • Serialization factor of 1. • Registered output path requires a clock. • Data is passed directly through the IOE.
DDR (×2)	• The IOE data width is 2 bits. • Serialization factor of 2. • The GPIO IP requires a clock. • `tx_inclock` clocks the IOE register.

Related Information

GPIO Intel FPGA IP, Intel Agilex® 7 General-Purpose I/O User Guide: M-Series

3.2.2. Differential I/O Bit Position

Table 7. Differential Bit Naming

This table lists the differential bit naming conventions for 12 differential channels. The MSB and LSB positions increase with the number of channels a system uses.

Transmitter Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56
9	71	64

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