MY-Semi

MY9221
12-Channel LED Driver With Grayscale Adaptive Pulse Density Modulation Control

General Description

The MY9221, 12-channels (R/G/B x 4) constant current APDM (Adaptive Pulse Density Modulation) LED driver, operates over a 3.3V ~ 5V input voltage range (±10%). The device provides 12 open-drain constant current sinking outputs that are rated to 24 V and delivers up to 60mA of high accuracy current to each string of LED. The current at each output is programmable by means of three external current setting resistors. MY9221 features a 10MHz EMI reduction data clock input. MY9221 also offers a 2-wire serial interface to send the grayscale data, control command including 16/14/12/8-bit grayscale selection, grayscale clock frequency division selection, output polarity selection for high power LED driving, output Tr/Tf timing selection, current output waveform selection, and to realize the internal-latch function. MY9221 provides adaptive pulse density modulation method to increase the visual refresh rate up to 1000 Hz @ 16-bit grayscale and reduce the flickers, and it also provides output current bilateral processing for EMI reduction. Moreover MY9221 utilizes clock duty recovery technique and pulse re-timing to help long distance and multiple cascading applications. MY9221 provides typical ±1% channel-to-channel LED current accuracy. Additional features include a ±0.1% regulated output current capability and fast output transient response. MY9221 is available in a 20-pin QFN or 24-pin SSOP/TSSOP package and specified over the -40°C to +85°C ambient temperature range.

Features

- 3.3 ~ 5V Operating supply voltage (±10%)
- R/G/B x4 Output Channels
- 3~60mA@5V Constant current output range
- 3~35mA@3.3V Constant current output range
- Current setting by 3 external resistors
- 24V Rated output channels for long LED strings
- ±1%(typ.) LED Current accuracy between channels
- ±2%(typ.) LED Current accuracy between chips
- 20Mbps(max.) ~ 140 Kbps(min.) data rate for EMI reduction data transfer [patent pending]
- 16 / 14 / 12 / 8 bit grayscale selection
- Built-in internal grayscale clock supports refresh rate >1000Hz@16-bit grayscale, >256KHz@8-bit grayscale
- Internal Grayscale clock frequency selection for High Power LED driving application (min. 33.6KHz)
- Grayscale clock source selection (SSOP & TSSOP only): internal or external
- PWM or APDM control selection [patent pending]
- Clock duty recovery for cascading application
- Schmitt trigger input
- Output Current Tr / Tf programmable
- Output Current Bilateral Processing for EMI reduction
- -40°C to +85°C Ambient temperature range

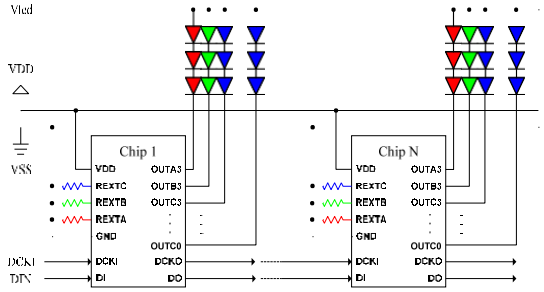
Applications

- Indoor and Outdoor LED Video Displays
- Full Color Mesh Display
- Full Color Dot Matrix Module
- Architectural and Decorative Lighting
- LCD Display Backlighting

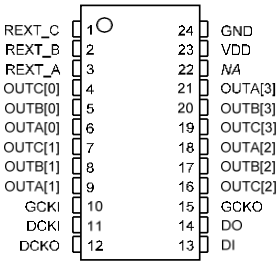
Order information

Part	Package Information	
MY9221SA	SOP24-236mil-1.0mm	2000 pcs/Reel
MY9221SS	SSOP24-150mil-0.635mm	2500 pcs/Reel
MY9221QD	QFN20-4mmx4mm-0.5mm	3000 pcs/Reel
MY9221TE	TSSOP24-173mil-0.65mm (Exposed Pad)	2500 pcs/Reel

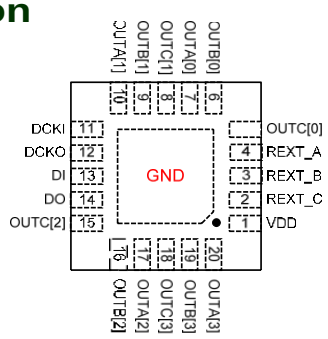
Typical Operating Circuits



Pin Configuration



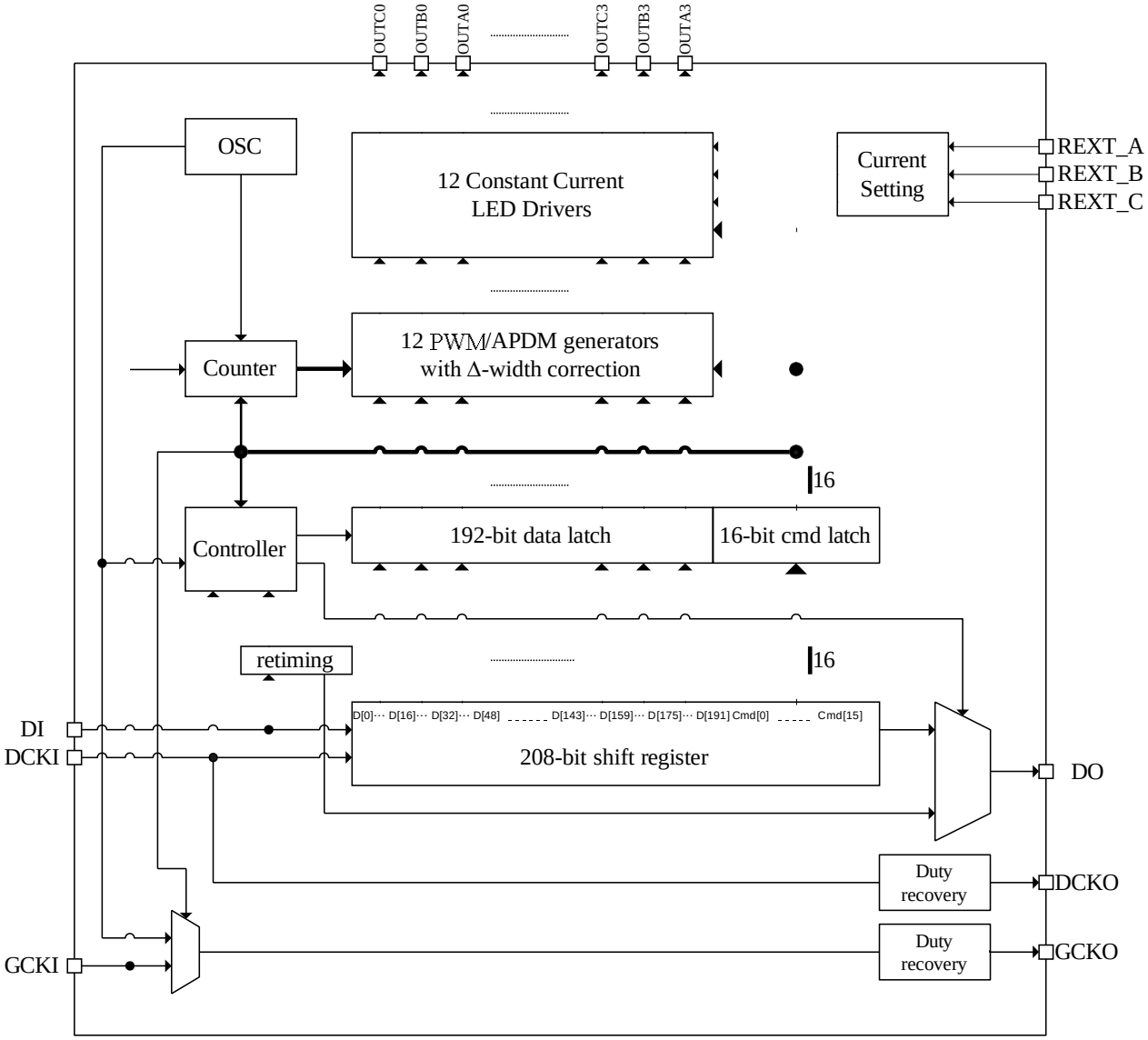
SA / SS / TE



QD

For pricing, delivery, and ordering information, please contact MY-Semi Inc. at +886-3-560-1668, or email to .tw or visit MY-Semi's website .tw

Block Diagram

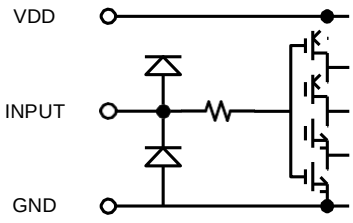


Pin Description

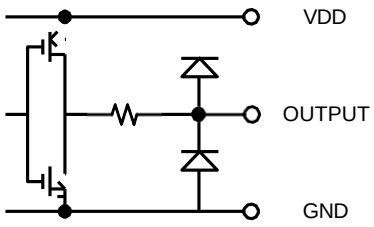
PIN No.		PIN NAME	FUNCTION
SOP24 SSOP24 TSSOP24	QFN20		
1,2,3	2,3,4	REXT_C,B,A	External resistors connected between REXT and GND for individual output current value setting.
19,16,7,4	18,15,8,5	OUTC[3:0]	Constant current outputs.
20,17,8,5	19,16,9,6	OUTB[3:0]	
21,18,9,6	20,17,10,7	OUTA[3:0]	
10	---	GCKI	External grayscale clock input for PWM/APDM operation.
11	11	DCKI	Clock input terminal for serial data transfer. Data is sampled at both rising edge and falling edge of DCKI.
12	12	DCKO	Clock output terminal for serial data transfer.
13	13	DI	Serial data input terminal.
14	14	DO	Serial data output terminal.
15	---	GCKO	Grayscale clock output When command data “osc” = ‘L’, GCKO comes from internal osc When command data “osc” = ‘H’, GCKO comes from GCKI
23	1	VDD	Supply voltage terminal.
24	Thermal pad	GND	Ground terminal.
22	---	NA	Not used

Equivalent Circuit of Inputs and Outputs

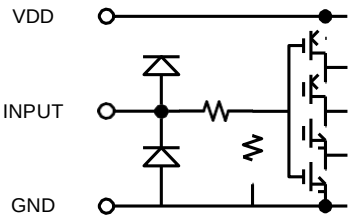
1. DI, DCKI terminals



2. DO, DCKO, GCKO terminals



3. GCKI terminal



Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	60	mA
Output Voltage	VOUT	-0.3 ~ 24	V
Input Data Clock Frequency	FDCK	0.07 ~ 10	MHz
Input Grayscale Clock Frequency	FGCK	10	MHz
GND Terminal Current	IGND	750	mA
Thermal Resistance (4 Layer PCB)	Rth(j-a)	53.2 (SA:SOP-236mil-1.0mm) 70.5 (SS:SSOP24-150mil-0.635mm) 36.9 (QD:QFN20-4mmx4mm) 31 (TE:TSSOP24-173mil-0.65mm (EP))	°C/W
Operating Supply Voltage	VDD	3.0 ~ 5.5	V
Operating Ambient Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.

(2) All voltage values are with respect to ground terminal.

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 24 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 4.8 mA	—	—	0.4	V
	VOH	IOH= 5.3 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 2340 Ω	—	±1	±3	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±2	±6	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 19.5 KΩ	—	±1	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4		—	±2	±6	%
Output Voltage Regulation*3	% / VOUT	Rrext = 2340 Ω VOUT = 1 V ~ 3 V	—	±.0.1	—	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 2340 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current *5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	2.40	—	mA
	$I_{DD2(off)}$	input signal is static Rrext = 2340 Ω all outputs turn off	—	5.73	—	
	$I_{DD3(on)}$	input signal is static Rrext = 2340 Ω all outputs turn on	—	5.85	—	
	$I_{DD4(off)}$	input signal is static Rrext = 19.5 KΩ all outputs turn off	—	2.84	—	
	$I_{DD5(on)}$	input signal is static Rrext = 19.5 KΩ all outputs turn on	—	2.84	—	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + ... + Iout_3)}{4}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + ... + Iout_3)}{4} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right) \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@Vcc = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

*5 IO excluded.

Electrical Characteristics (VDD = 3.3 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 24 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 3.9 mA	—	—	0.4	V
	VOH	IOH= 3.8 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel)*1	dIOUT1	VOUT = 1.0 V Rrext = 2340 Ω	—	±1	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT2		—	±2	±6	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 19.5 KΩ	—	±1	±3	%
Output Current Skew (Channel-to-Channel)*2	dIOUT4			±2	±6	%
Output Voltage Regulation*3	% / VOUT	Rrext = 2340 Ω VOUT = 1 V ~ 3 V	—	±0.1	—	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 2340 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current*5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	1.97	—	mA
	$I_{DD2(off)}$	input signal is static Rrext = 2340 Ω all outputs turn off	—	5.22	—	
	$I_{DD3(on)}$	input signal is static Rrext = 2340 Ω all outputs turn on	—	5.22	—	
	$I_{DD4(off)}$	input signal is static Rrext = 19.5 KΩ all outputs turn off	—	2.74	—	
	$I_{DD5(on)}$	input signal is static Rrext = 19.5 KΩ all outputs turn on	—	2.79	—	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + ... + Iout_3)}{4}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{\frac{(Iout_0 + Iout_1 + ... + Iout_3)}{4} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@Vcc = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

*5 IO excluded.

Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	DCKI-to-DO	tpLH1	VIH = VDD VIL = GND Rrext = 2340 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	29	39	ns
	DCKI-to-DCKO	tpLH2		—	6.3	19	
	GCKI-to-GCKO	tpLH3		—	10.5	19	
	DI-to-DO @ Internal-latch control cycle	tpLH4		—	12	—	
Propagation Delay ('H' to 'L')	DCKI-to-DO	tpHL1		—	39	59	
	DCKI-to-DCKO	tpHL2		—	6.3	19	
	GCKI-to-GCKO	tpHL3		—	9	19	
Pulse Duration	DCKI	$tw_{(DCK)}$		50	—	7200	
	GCKI	$tw_{(GCK)}$		50	—	—	
	DI @ Internal-latch control cycle	$twH_{(DI)}$		70	—	—	
	DI @ Internal-latch control cycle	$twL_{(DI)}$		230	—	—	
Setup Time	DI	$tsu_{(D)}$		10	—	—	
Hold Time	DI	$th_{(D)}$		10	—	—	
DO/DCKO/GCKO Rise Time		$tr_{(DO)}$		—	5	—	
DO/DCKO/GCKO Fall Time		$tf_{(DO)}$		—	5	—	
Output Current Rise Time (fast)		Tor_f		—	10	—	
Output Current Fall Time (fast)		Tof_f		—	4	—	
Output Current Rise Time (slow)		Tor_s		—	90	—	
Output Current Fall Time (slow)		Tof_s		—	66	—	
DI Retiming @ Internal-latch control cycle		Tw_re		70	90	110	
Internal-latch Start Time		Tstart		220	—	—	us
Internal-latch Stop Time*		Tstop		200	—	—	ns
DCKI Freq.		F(DCKI)		0.07	—	10	MHz
Internal OSC Freq.		F(OSC)		6.9	8.6	10.3	MHz
GCKI Freq.		F(GCKI)		—	—	10	MHz

* Tstop (min.) for cascade application must > "200ns + N*10ns" (N is the cascade number of drivers)

Switching Characteristics (VDD = 3.3V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	DCKI-to-DO	tpLH1	VIH = VDD VIL = GND Rrext = 2340 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	34	39	ns
	DCKI-to-DCKO	tpLH2		—	7.9	19	
	GCKI-to-GCKO	tpLH3		—	12	19	
	DI-to-DO @ Internal-latch control cycle	tpLH4		—	18	—	
Propagation Delay ('H' to 'L')	DCKI-to-DO	tpHL1		—	40	59	
	DCKI-to-DCKO	tpHL2		—	8.2	19	
	GCKI-to-GCKO	tpHL3		—	10.5	19	
Pulse Duration	DCKI	$tw_{(DCK)}$		50	—	7200	
	GCKI	$tw_{(GCK)}$		50	—	—	
	DI @ Internal-latch control cycle	$twH_{(DI)}$		70	—	—	
	DI @ Internal-latch control cycle	$twL_{(DI)}$		230	—	—	
Setup Time	DI	$tsu_{(D)}$		10	—	—	
Hold Time	DI	$th_{(D)}$		10	—	—	
DO/DCKO/GCKO Rise Time		$tr_{(DO)}$		—	8.5	—	
DO/DCKO/GCKO Fall Time		$tf_{(DO)}$		—	8.5	—	
Output Current Rise Time (fast)		Tor_f		—	13.4	—	
Output Current Fall Time (fast)		Tof_f		—	7.5	—	
Output Current Rise Time (slow)		Tor_s		—	153	—	
Output Current Fall Time (slow)		Tof_s		—	77	—	
DI Retiming @ Internal-latch control cycle		Tw_re		90	110	130	
Internal-latch Start Time		Tstart		220	—	—	us
Internal-latch Stop Time*		Tstop		200	—	—	ns
DCKI Freq.		F(DCKI)		0.07	—	10	MHz
Internal OSC Freq.		F(OSC)		6.7	8.4	10.1	MHz
GCKI Freq.		F(GCKI)		—	—	10	MHz

* Tstop (min.) for cascade application must > "200ns + N*10ns" (N is the cascade number of drivers)