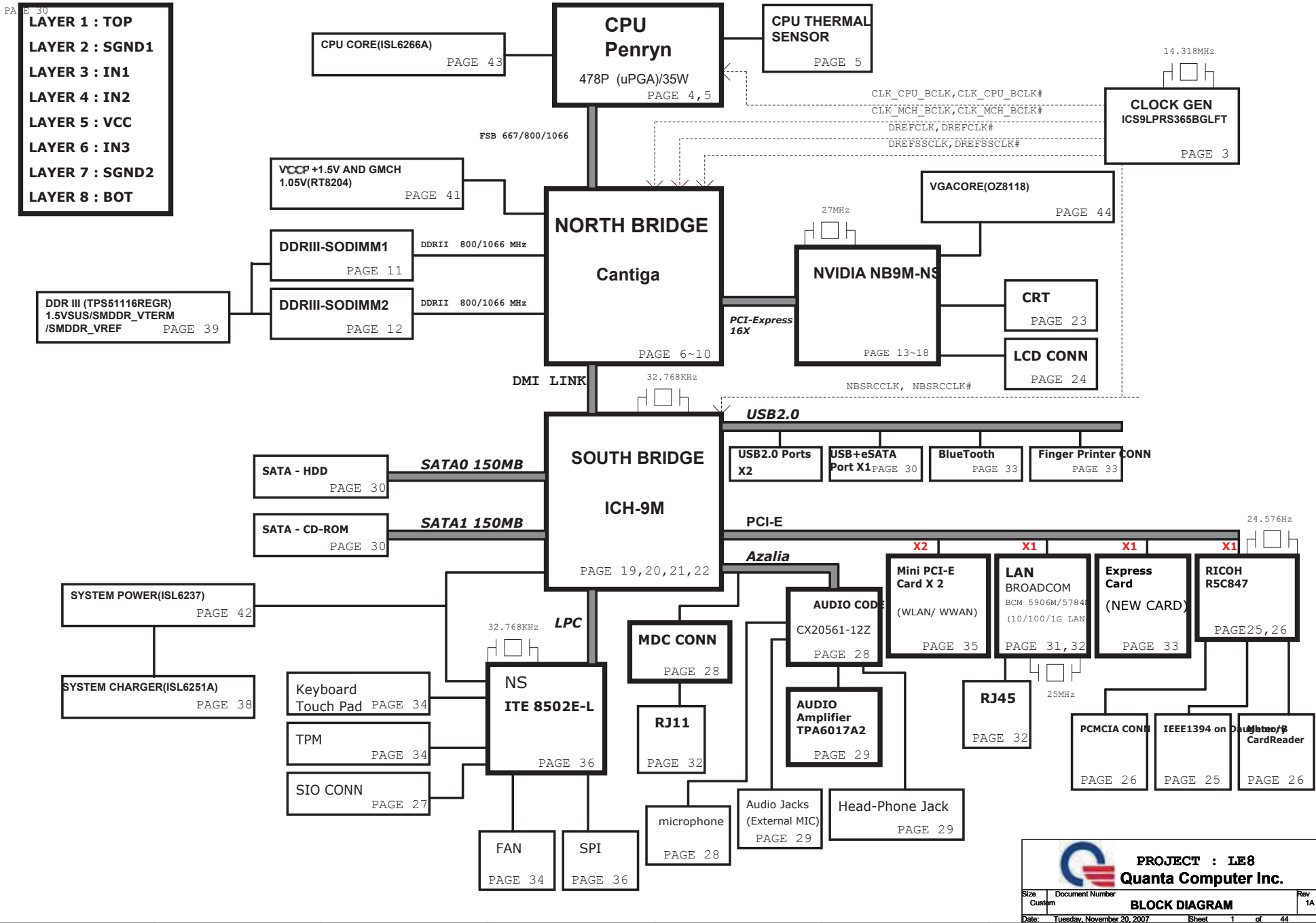


**PCB STACK UP  
8L**

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

# LE8(K43) BLOCK DIAGRAM

01










**PROJECT : LE8**  
**Quanta Computer Inc.**

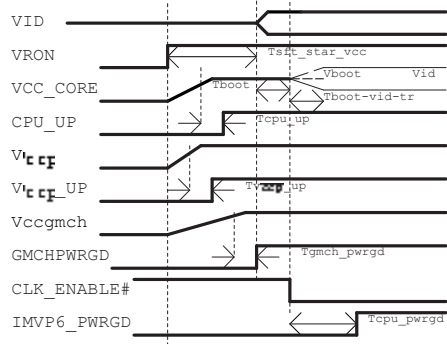
Size	Document Number	Rev	
Custom	<b>BLOCK DIAGRAM</b>	1A	
Date: Tuesday, November 20, 2007		Sheet	1 of 44

# Board Stack up Description

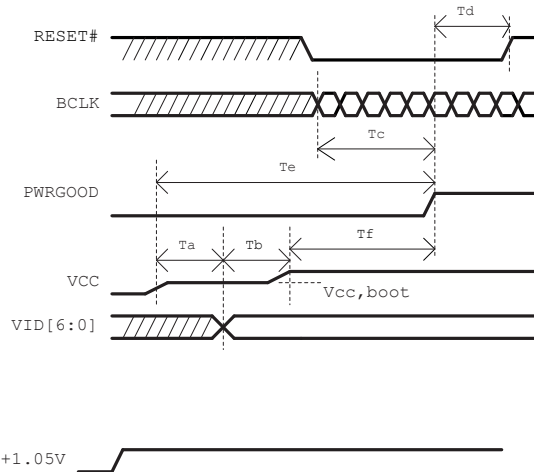
## PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



MEROM Power-up Timing Specifications

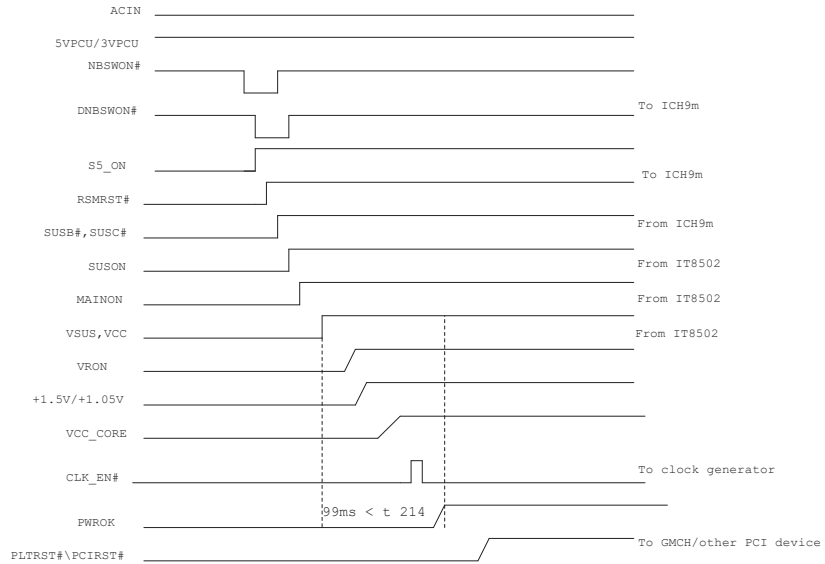


Ta=VCC and V<sub>cc</sub> assertion to VID[6:0] valid  
 Tb=VID[6:0] stable to VCC valid  
 Tc=BCLK stable to PWRGOOD assertion  
 Td=PWRGOOD to RESET# de-assertion time  
 Te=Vcc,boot valid to PWRGOOD assertion time

## Voltage Rails

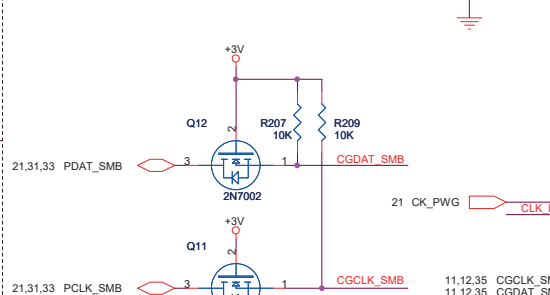
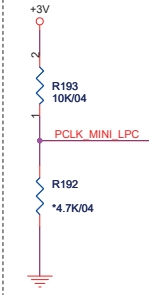
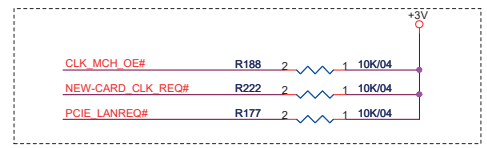
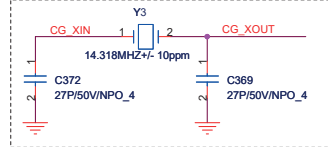
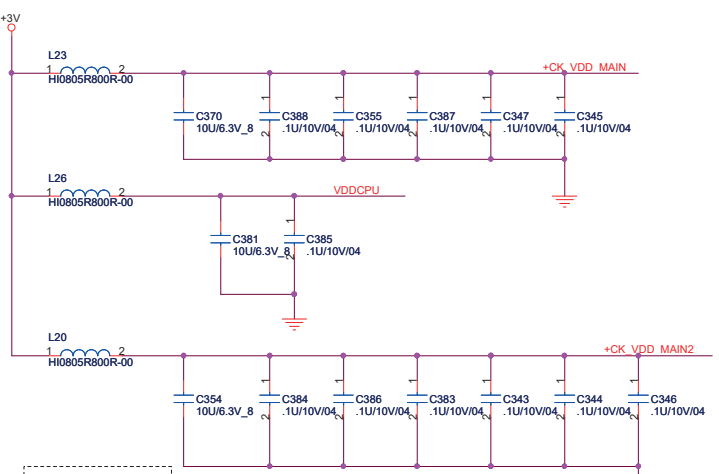
Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.5VSUS	X	X			SUSON
SMDRR_VTERM/+3V/+5V/+15V/+1.8V	X				MAINON
+VGACORE/+VGA1.1V	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3V/PCII	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING

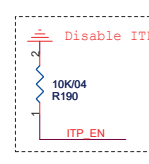
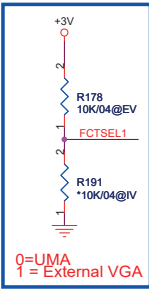


**PROJECT : LE8**  
**Quanta Computer Inc.**

Size: Custom Document Number: SYSTEM INFORMATION Rev: 1A  
 Date: Tuesday, November 20, 2007 Sheet: 2 of 44



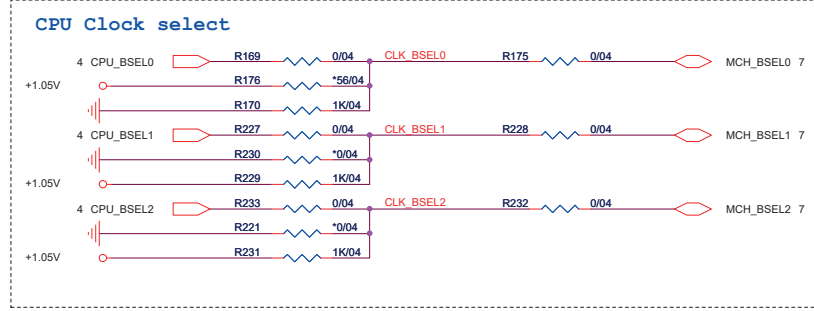
0=overclocking of CPU and SRC Allowed  
1 = overclocking of CPU and SRC not Allowed



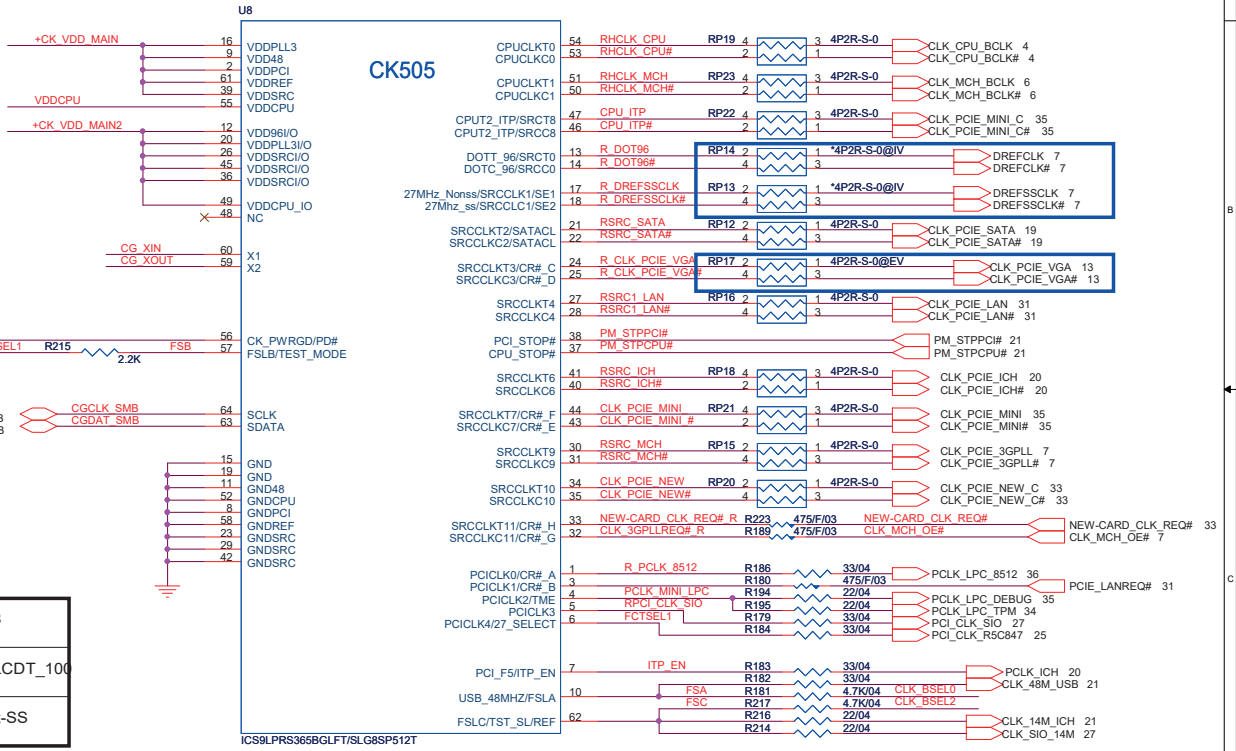
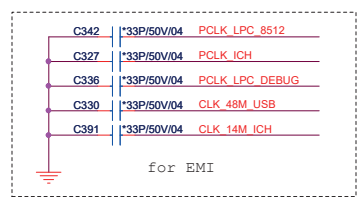
0=UMA  
1 = External VGA

**GCLK\_SEL = FCTSEL1**

FCTSEL1 (PIN13)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS



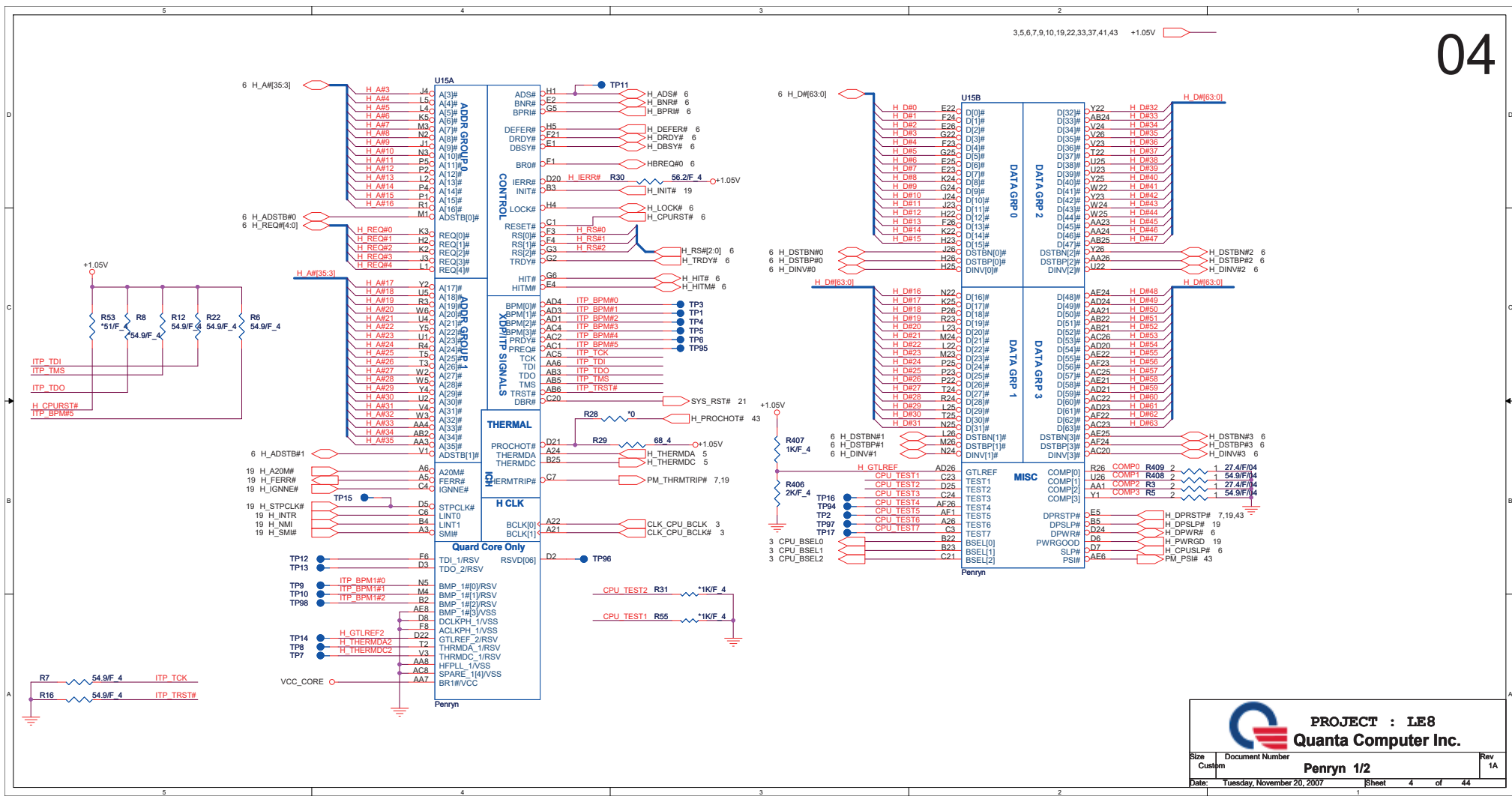
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33




**CPU Clock select**

**PROJECT : LE8**  
**QUANTA Computer Inc.**

Size	Document Number	Rev
Custom	<b>CLOCK GENERATOR</b>	1A
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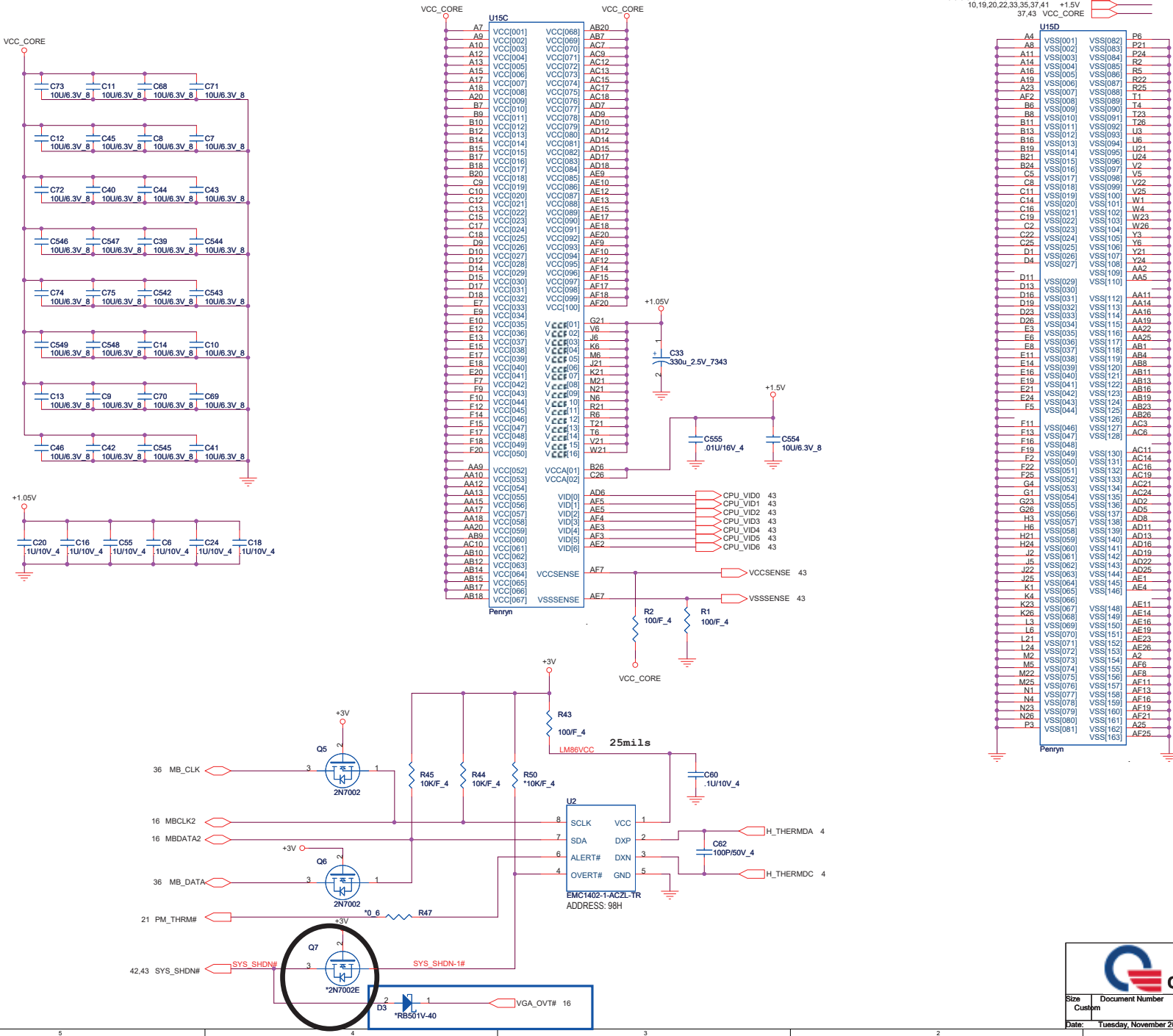


**PROJECT : IE8**  
**Quanta Computer Inc.**

Size: Custom    Document Number: **Penryn 1/2**    Rev: 1A

Date: Tuesday, November 20, 2007    Sheet: 4 of 44

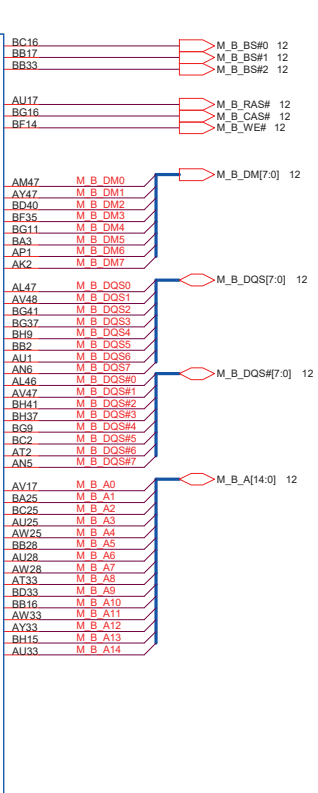
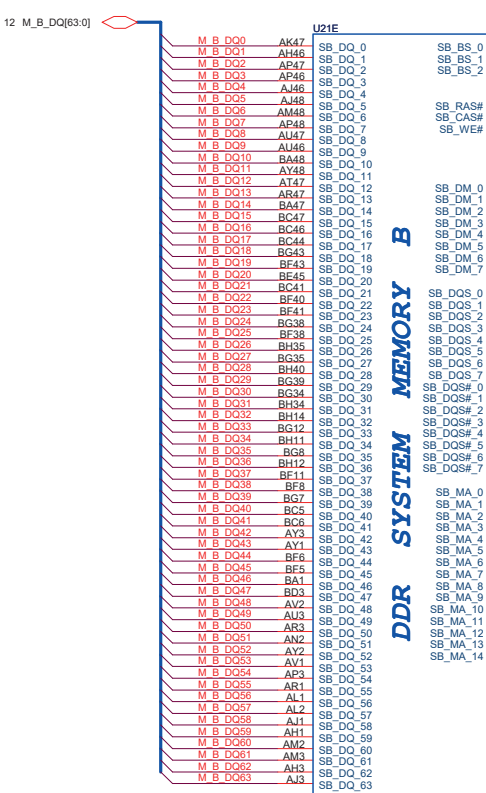
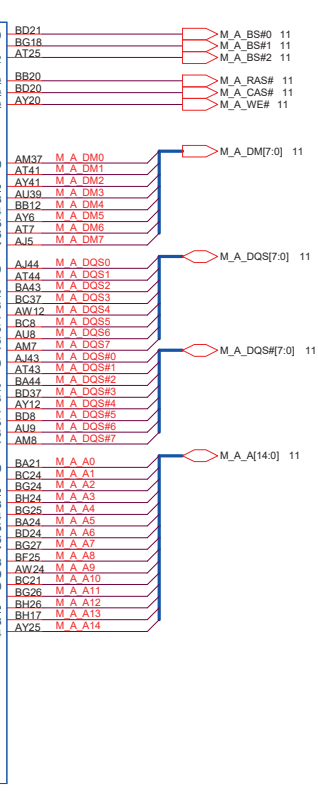
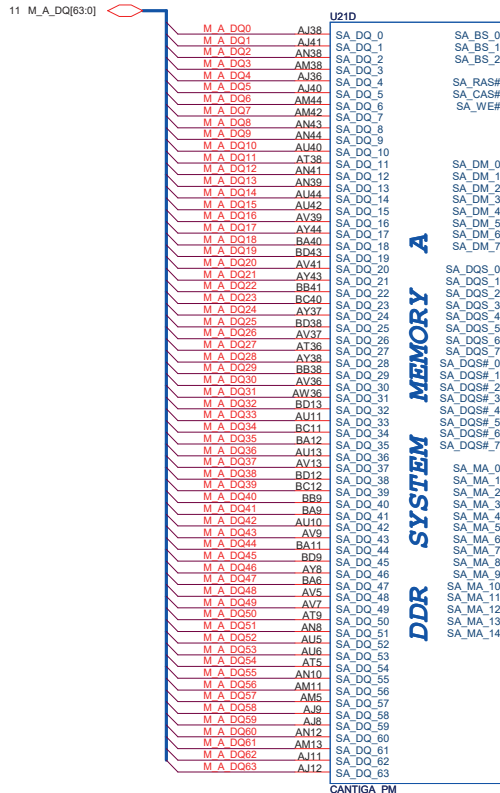
3,7,10,11,12,13,15,16,19,20,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44 +3V  
3,4,6,7,9,10,19,22,33,37,41,43 +1.05V  
10,19,20,22,33,35,37,41 +1.5V  
37,43 VCC\_CORE



**PROJECT : LE8**  
**Quanta Computer Inc.**  
 Size Custom Document Number  
**Penryn & TH Monitor 2/2** Rev 1A  
 Date: Tuesday, November 20, 2007 Sheet 5 of 44

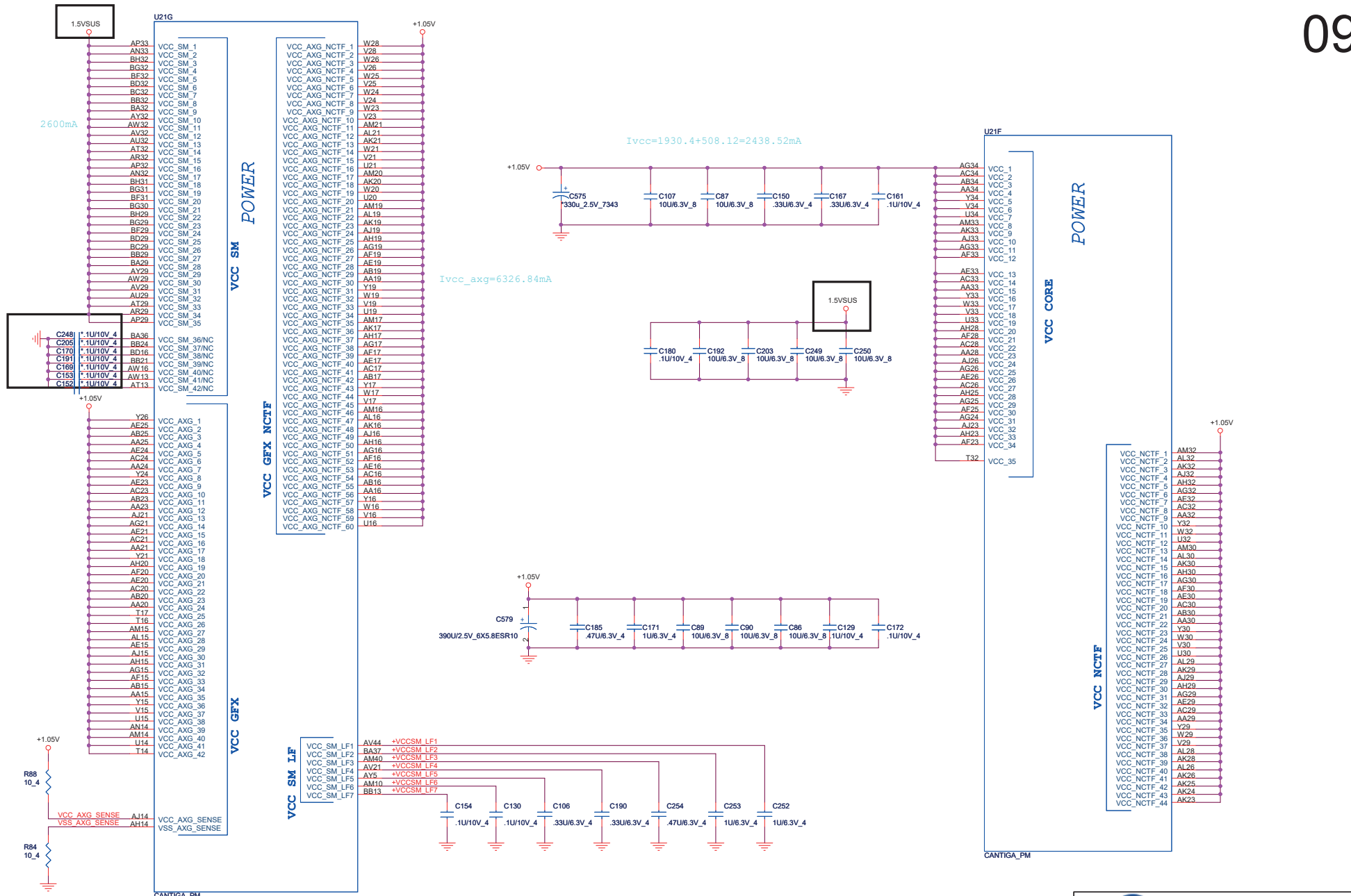






**PROJECT : LE8**  
**Quanta Computer Inc.**

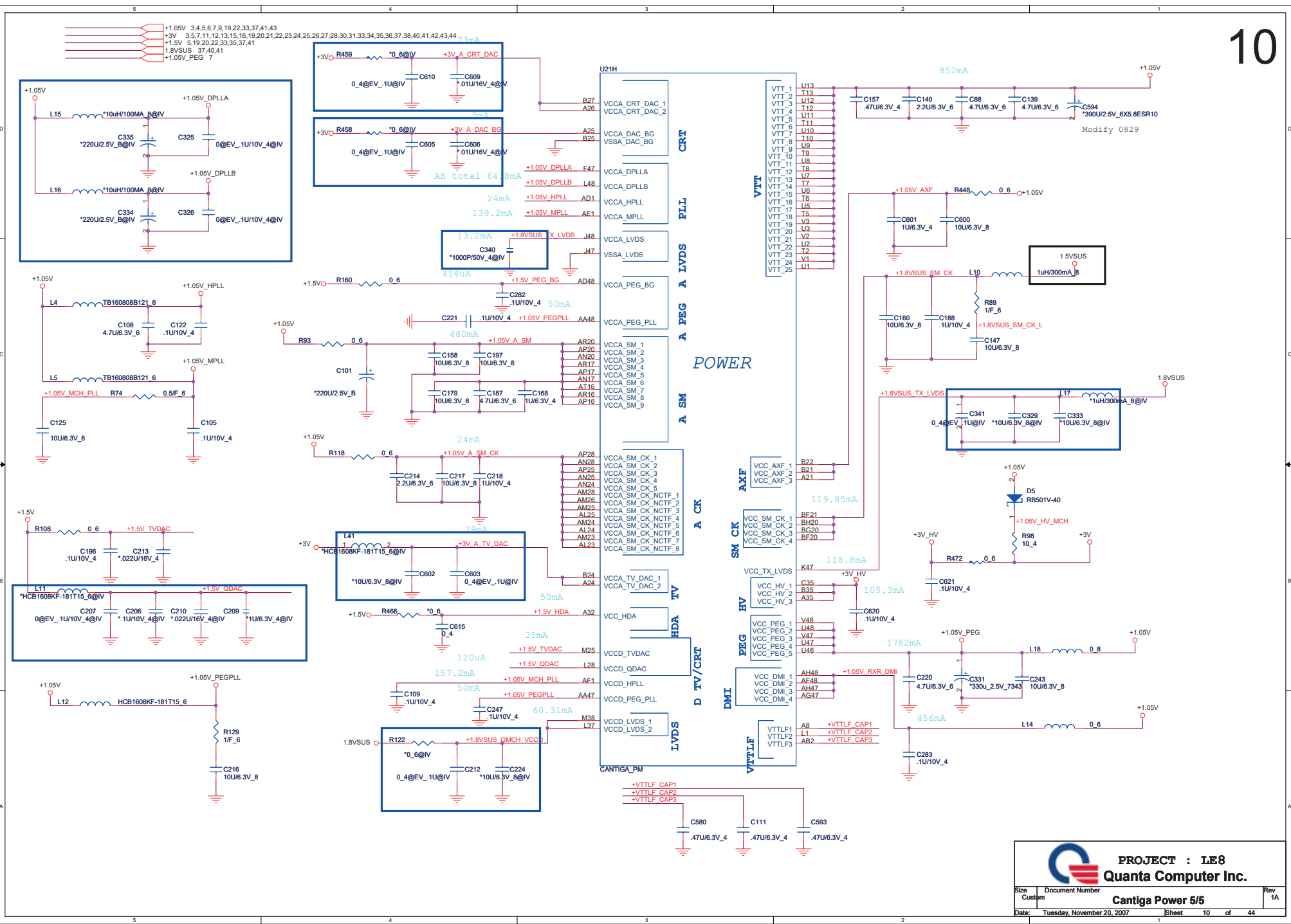
Size: Custom Document Number  
**Cantiga DDR3 3/5**  
 Date: Tuesday, November 20, 2007 Sheet 8 of 44 Rev 1A



7,10,11,12,33,37,39,44 1.5VSUS  
 3,4,5,6,7,10,19,22,33,37,41,43 +1.05V

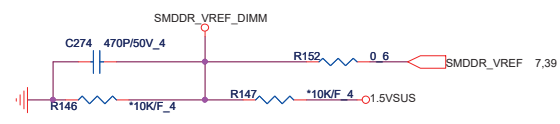
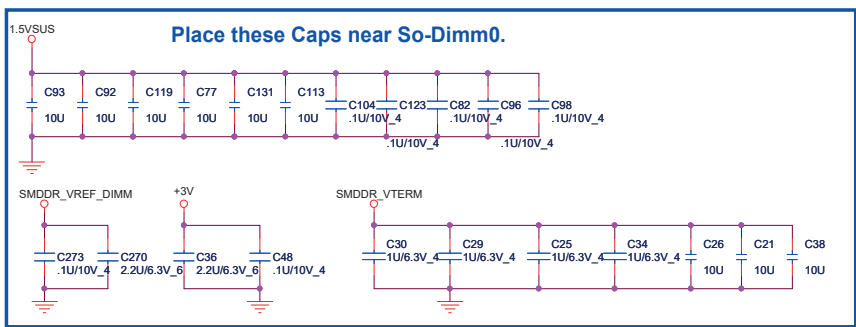
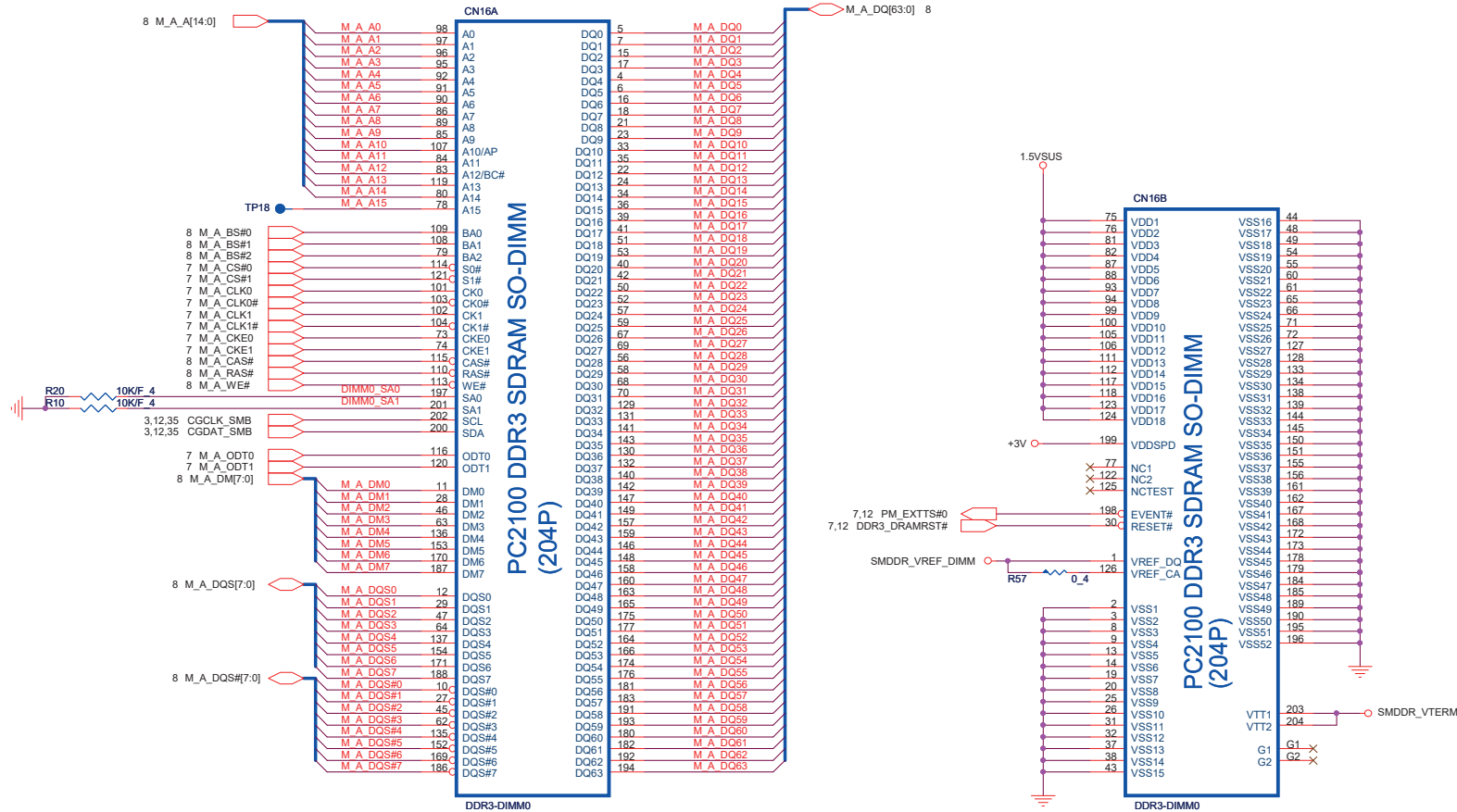
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**Quanta Computer Inc.**

Size: Custom Document Number: Cantiga Vcc 4/5 Rev 1A  
 Date: Tuesday, November 20, 2007 Sheet 9 of 44



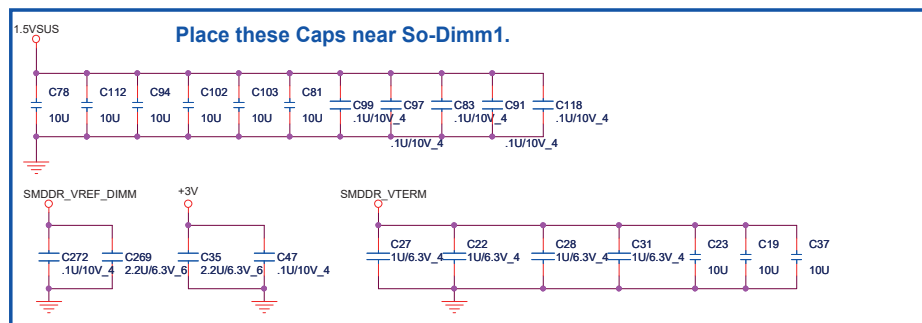
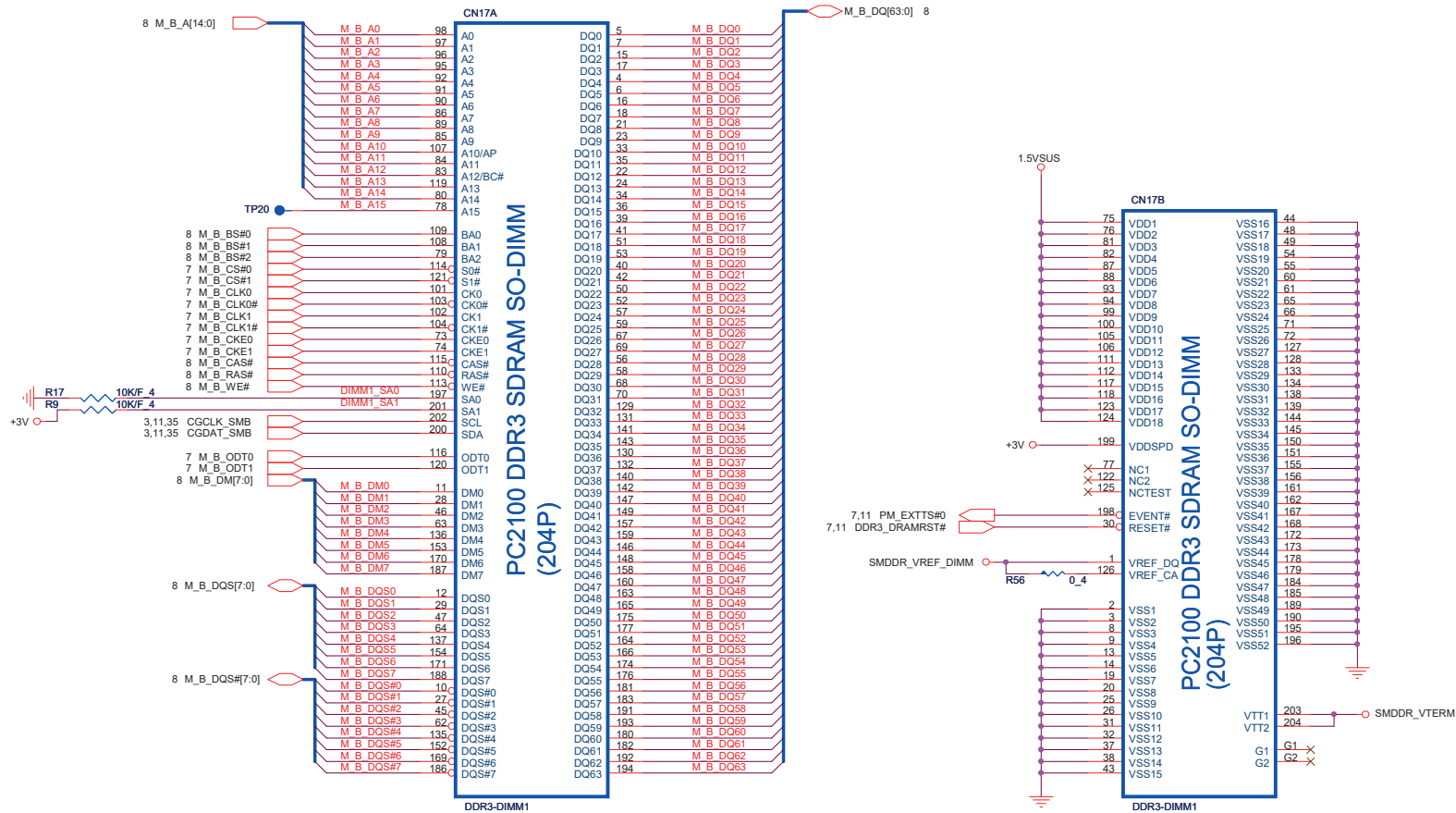
**PROJECT : IE8**  
**Quanta Computer Inc.**

Size: Custom Document Number: Cantiga Power 5/5 Rev 1A  
 Date: Tuesday, November 20, 2007 Sheet 10 of 44



**PROJECT : LE8**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>DDR3 DIMM-0(H=5.2)</b>	Rev 1A
Date: Tuesday, November 20, 2007		
Sheet 11 of 44		



**PROJECT : LE8**  
**Quanta Computer Inc.**

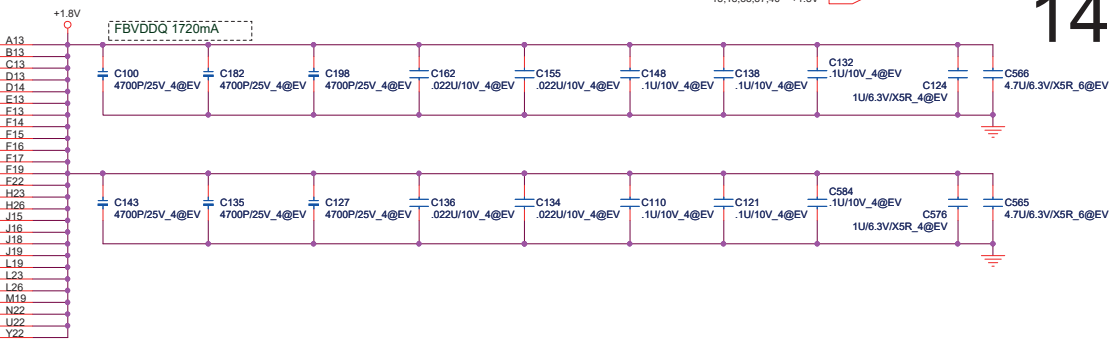
Size Custom	Document Number <b>DDR3 DIMM-1(H=9.2)</b>	Rev 1A
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- 18 VMA\_DQ[83..0]
- 18 VMA\_DM[7..0]
- 18 VMA\_WDQS[7..0]
- 18 VMA\_RDQS[7..0]

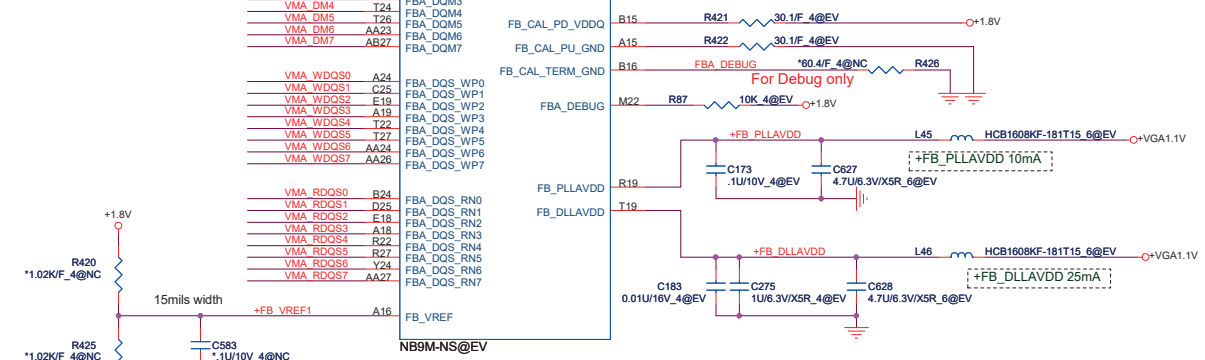
**U20B**

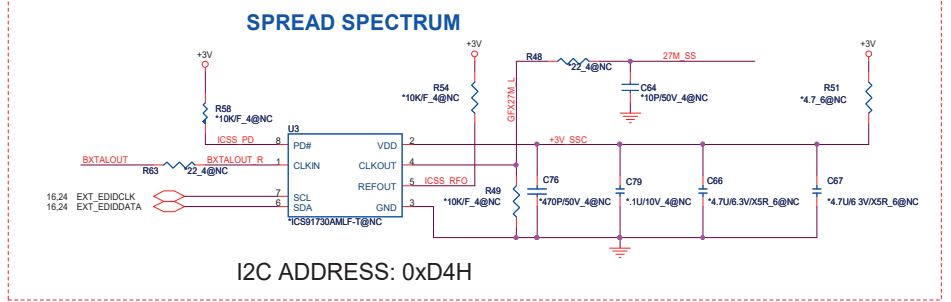
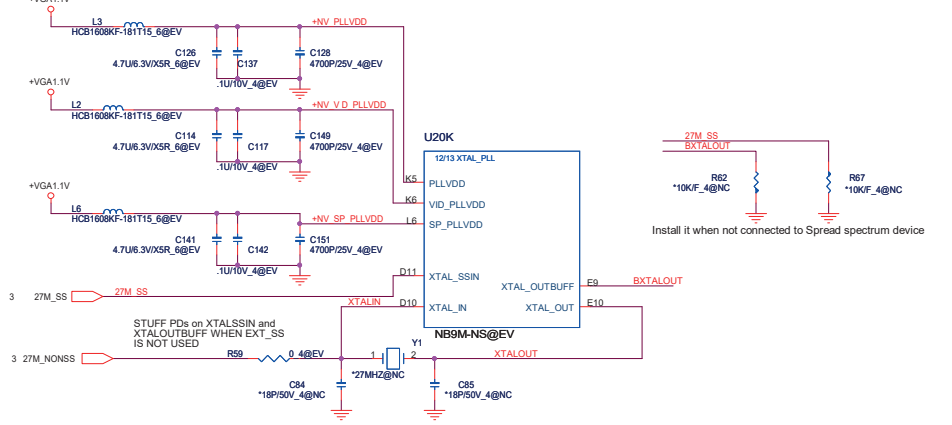
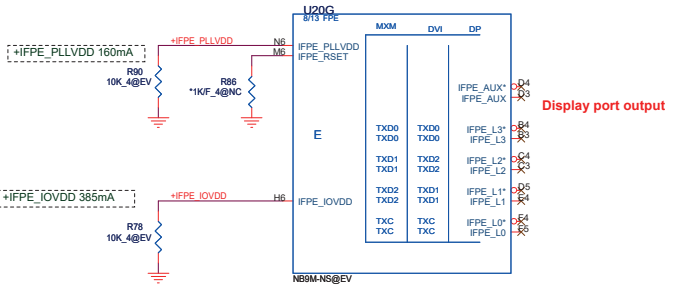
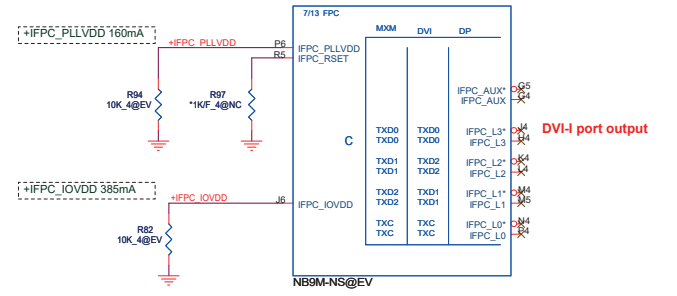
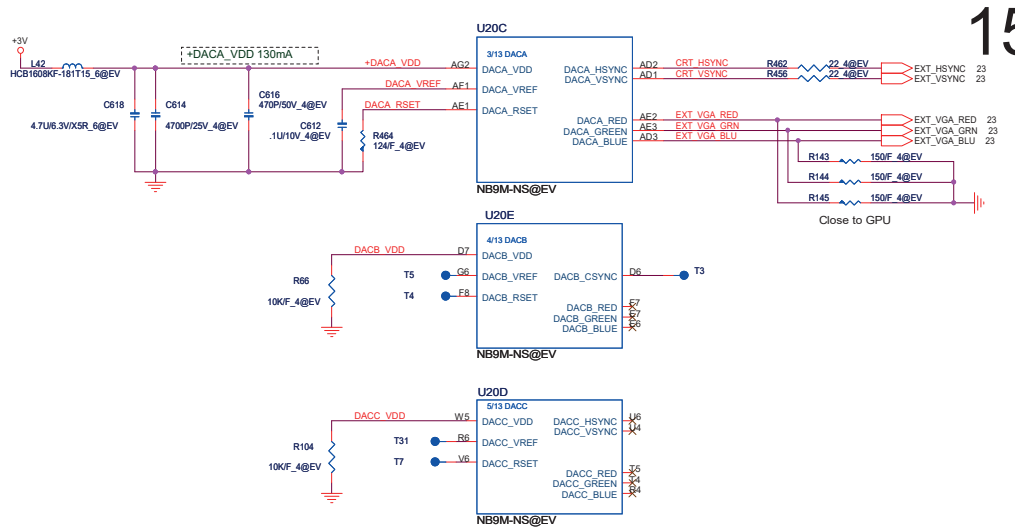
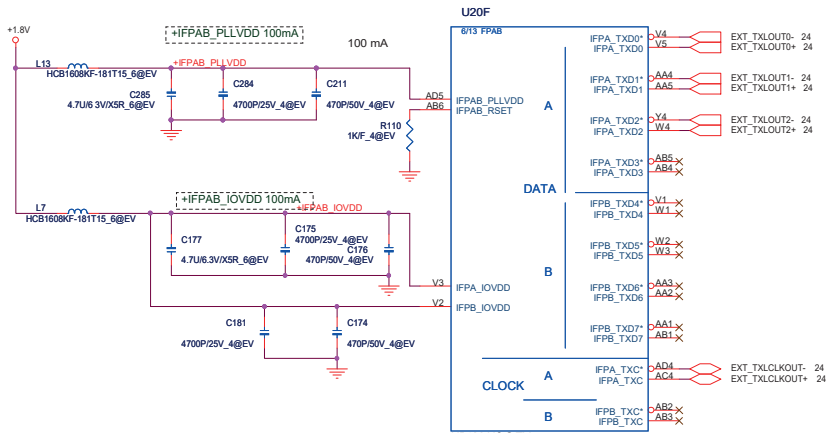
VMA_DQ0	D21	2/13 FRAME_BUFFER	FBVDDQ_01	A13
VMA_DQ1	C22	FBA_D0	FBVDDQ_02	B13
VMA_DQ2	B22	FBA_D1	FBVDDQ_03	C13
VMA_DQ3	A22	FBA_D2	FBVDDQ_04	D13
VMA_DQ4	C24	FBA_D3	FBVDDQ_05	D14
VMA_DQ5	B25	FBA_D4	FBVDDQ_06	E13
VMA_DQ6	A25	FBA_D5	FBVDDQ_07	F13
VMA_DQ7	A26	FBA_D6	FBVDDQ_08	F14
VMA_DQ8	D22	FBA_D7	FBVDDQ_09	F15
VMA_DQ9	E22	FBA_D8	FBVDDQ_10	F16
VMA_DQ10	E24	FBA_D9	FBVDDQ_11	F17
VMA_DQ11	D24	FBA_D10	FBVDDQ_12	F19
VMA_DQ12	D26	FBA_D11	FBVDDQ_13	F22
VMA_DQ13	C27	FBA_D12	FBVDDQ_14	H23
VMA_DQ14	C27	FBA_D13	FBVDDQ_15	H26
VMA_DQ15	B27	FBA_D14	FBVDDQ_16	J15
VMA_DQ16	E16	FBA_D15	FBVDDQ_17	J16
VMA_DQ17	E16	FBA_D16	FBVDDQ_18	J18
VMA_DQ18	D17	FBA_D17	FBVDDQ_19	J19
VMA_DQ19	F18	FBA_D18	FBVDDQ_20	L19
VMA_DQ20	D20	FBA_D19	FBVDDQ_21	L23
VMA_DQ21	F20	FBA_D20	FBVDDQ_22	L26
VMA_DQ22	E21	FBA_D21	FBVDDQ_23	M19
VMA_DQ23	F21	FBA_D22	FBVDDQ_24	N22
VMA_DQ24	C16	FBA_D23	FBVDDQ_25	U22
VMA_DQ25	B18	FBA_D24	FBVDDQ_26	Y22
VMA_DQ26	C18	FBA_D25		
VMA_DQ27	D18	FBA_D26		
VMA_DQ28	C19	FBA_D27		
VMA_DQ29	C21	FBA_D28		
VMA_DQ30	B21	FBA_D29		
VMA_DQ31	A21	FBA_D30		
VMA_DQ32	P22	FBA_D31		
VMA_DQ33	P24	FBA_D32		
VMA_DQ34	R23	FBA_D33		
VMA_DQ35	R24	FBA_D34		
VMA_DQ36	T23	FBA_D35		
VMA_DQ37	U24	FBA_D36		
VMA_DQ38	V23	FBA_D37		
VMA_DQ39	V24	FBA_D38		
VMA_DQ40	N25	FBA_D39		
VMA_DQ41	N26	FBA_D40		
VMA_DQ42	R25	FBA_D41		
VMA_DQ43	R26	FBA_D42		
VMA_DQ44	T25	FBA_D43		
VMA_DQ45	V26	FBA_D44		
VMA_DQ46	V25	FBA_D45		
VMA_DQ47	V27	FBA_D46		
VMA_DQ48	V22	FBA_D47		
VMA_DQ49	W22	FBA_D48		
VMA_DQ50	W23	FBA_D49		
VMA_DQ51	W24	FBA_D50		
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VMA_DQ53	AB23	FBA_D52		
VMA_DQ54	AB24	FBA_D53		
VMA_DQ55	AC24	FBA_D54		
VMA_DQ56	AD24	FBA_D55		
VMA_DQ57	AD25	FBA_D56		
VMA_DQ58	W25	FBA_D57		
VMA_DQ59	AA25	FBA_D58		
VMA_DQ60	AB25	FBA_D59		
VMA_DQ61	AB26	FBA_D60		
VMA_DQ62	AD26	FBA_D61		
VMA_DQ63	AD27	FBA_D62		
		FBA_D63		



- F26 VMA\_MA3 18
- J24 VMA\_MA0 18
- F25 VMA\_MA2 18
- M23 VMA\_MA1 18
- N27 VMA\_MASH 18
- M27 VMA\_M4H 18
- K26 VMA\_MAS 18
- J25 VMA\_CS0# 18
- J27 VMA\_WE# 18
- G23 VMA\_BA0 18
- G26 VMA\_CKE 18
- J23 VMA\_MASH 18
- M25 VMA\_MA2H 18
- K27 VMA\_MA12 18
- G25 VMA\_RAS# 18
- L24 VMA\_MA11 18
- K23 VMA\_MA10 18
- K24 VMA\_BA1 18
- G22 VMA\_MAS 18
- K25 VMA\_MAS 18
- H22 VMA\_MA9 18
- M26 VMA\_MA6 18
- H24 VMA\_MA5 18
- F27 VMA\_MA7 18
- J26 VMA\_MA4 18
- G24 VMA\_CAS# 18
- G27 VMA\_CMD27 18
- M24
- K22
- RFU\_3
- RFU\_4
- RFU\_4
- F24 VMA\_CLK0
- E23 VMA\_CLK0#
- N24 VMA\_CLK1#
- N23 VMA\_CLK1#

for DDR2 need use  
CMD11(CKE) and  
CMD12(ODT)



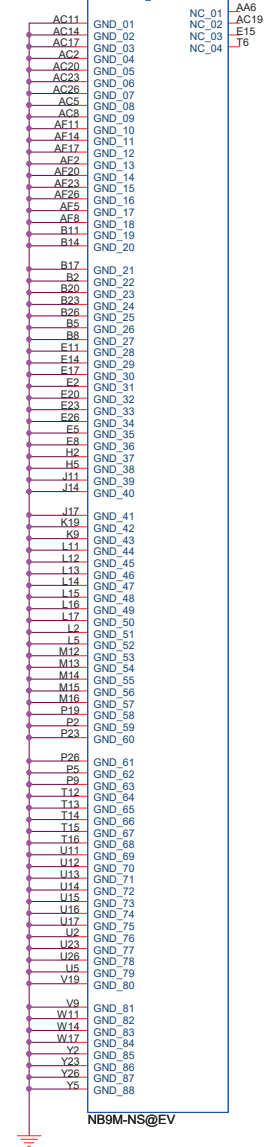


14,18,33,37,40 +1.8V  
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 13,14,33,37,44 +VGA1.1V

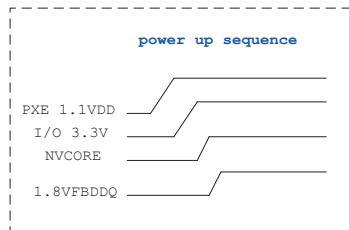


U20J

19/13 GND\_NC

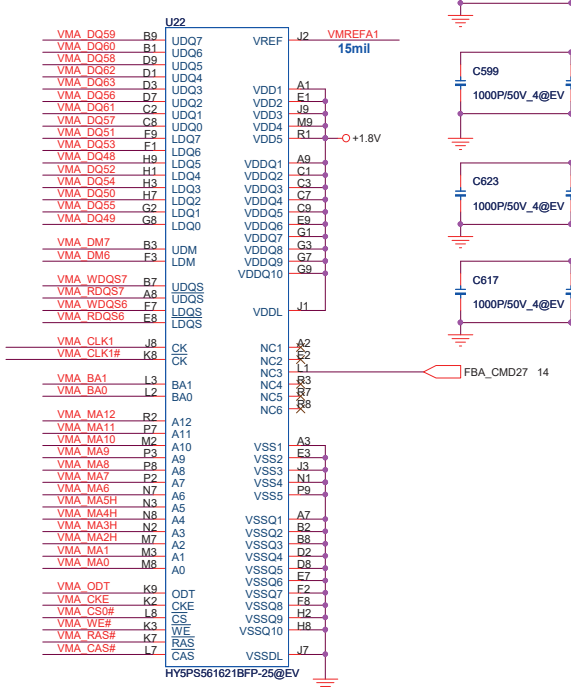
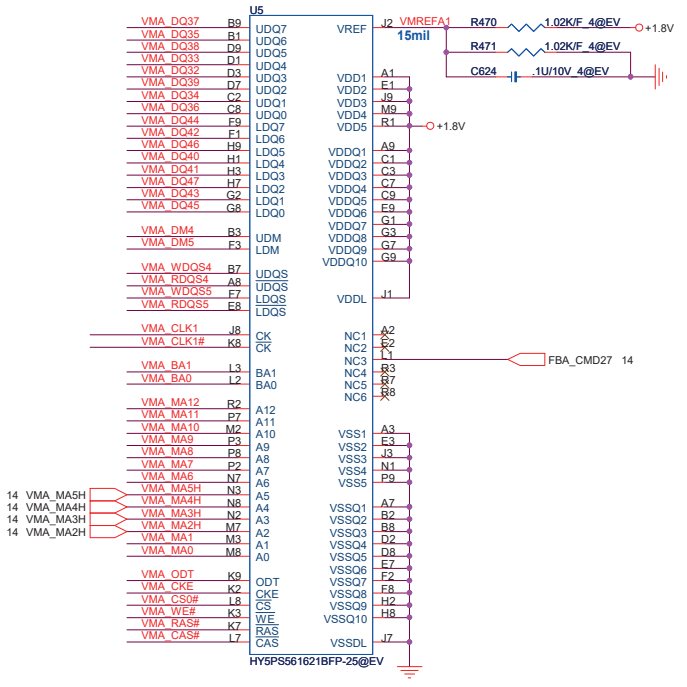
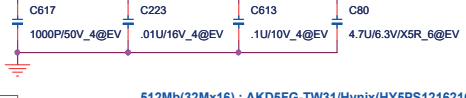
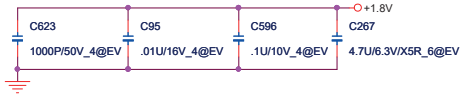
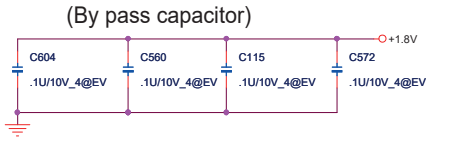
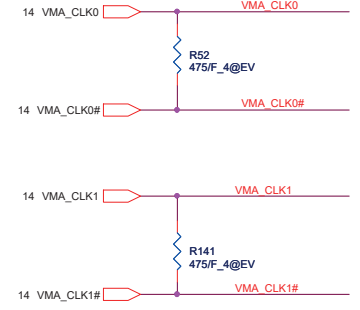
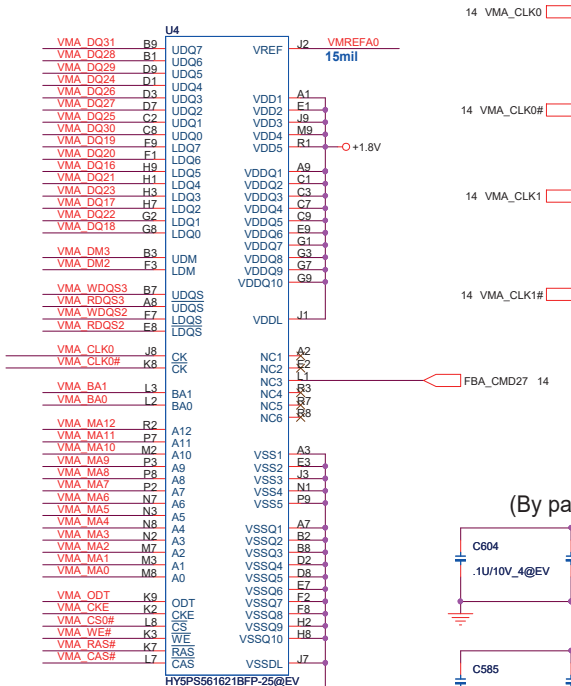
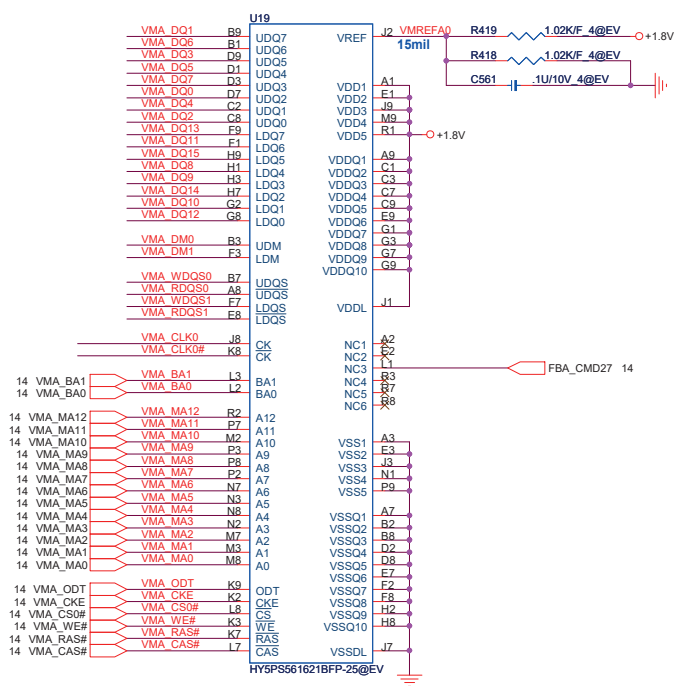


NB9M: VGACORE +0.9V ~ +1.0V

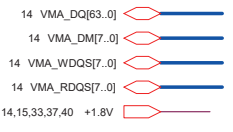


PROJECT : LE8  
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X GND 5/5	1A
Date:	Tuesday, November 20, 2007	Sheet 17 of 44

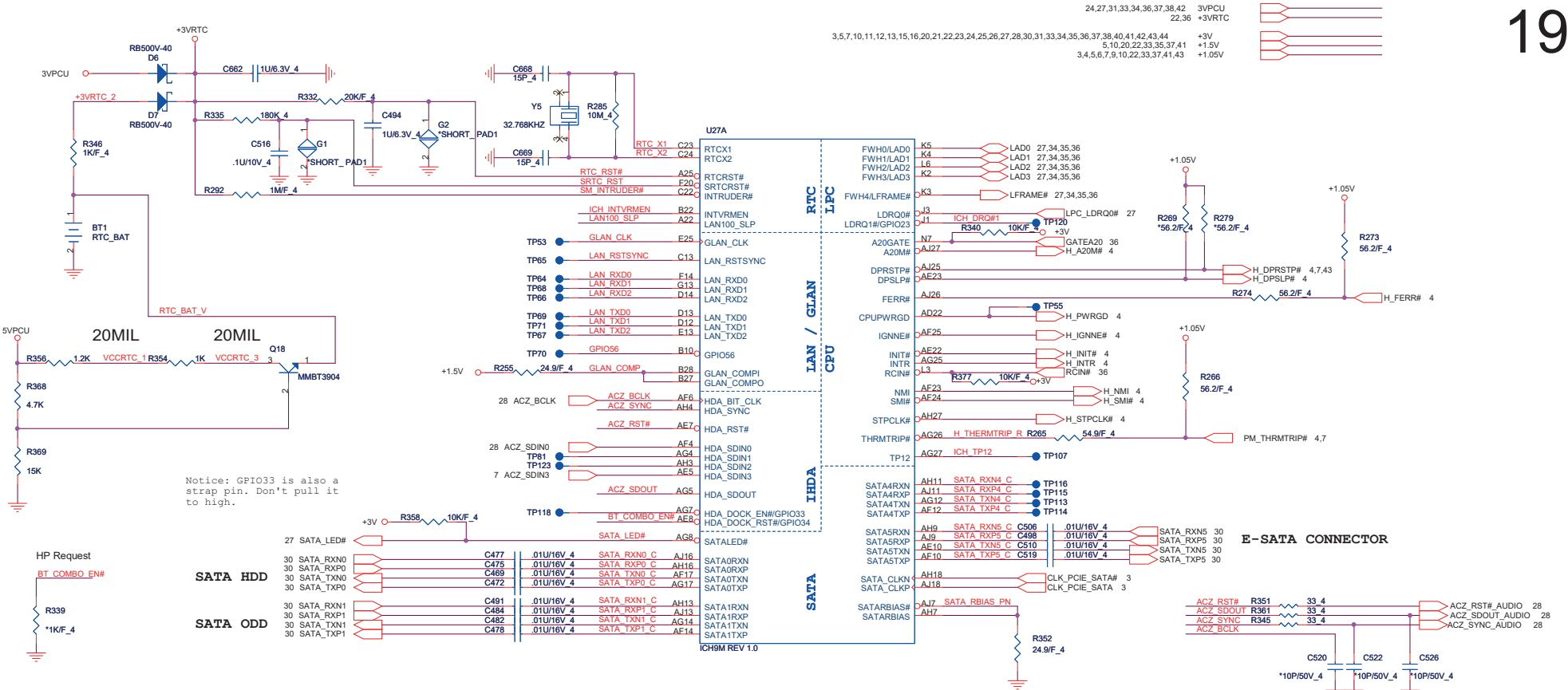


512Mb(32Mx16) : AKD5FG-TW31/Hynix(HYSP5121621CFP-25)  
 AKD5FG-T\*04/Quimonda(HYB18T512161B2F-20)



**PROJECT : LE8**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	NV9X VRAM-1(GDDR2 BGA84)	1A
Date:	Tuesday, November 20, 2007	Sheet 18 of 44



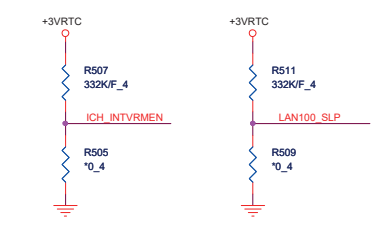
SB Strap

ICH9-M Internal VR Enable strap (Internal VR for VccSus1\_05, VccSus1\_5 and VccCL1\_5)

ICH9-M LAN100\_SLP Strap (Internal VR for VccLAN1\_05 and VccCL1\_05)

INTVRMEN Low = Internal VR disable High = Internal VR enable(Default)

LAN100\_SLP Low = Internal VR disable High = Internal VR enable(Default)



XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1	(default)
SPI	0	1	
PCI	1	0	
LPC	1	1	(default)



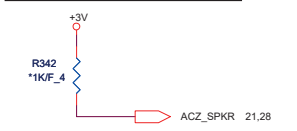
A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled	Hi = Default



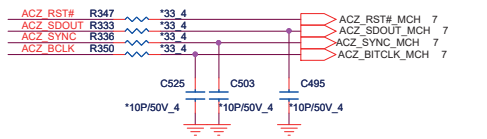
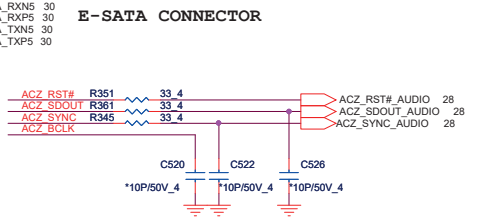
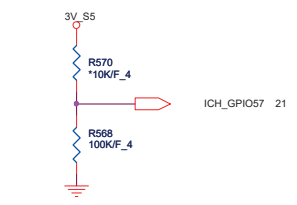
No Reboot Strap

ACZ_SPKR	Low: Default	Hi: No reboot



TPM physical presence

ICH_GPIO57	Low: Default



PROJECT : LE8  
Quanta Computer Inc.

Size Custom Document Number ICH9-M Host 1/4 Rev 1A

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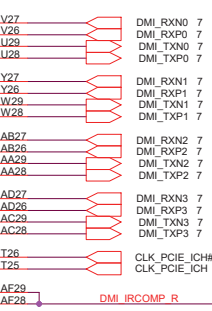
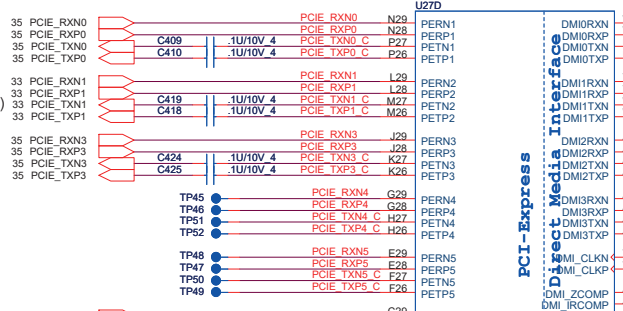
3,5,7,10,11,12,13,15,16,19,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44  
6,10,19,22,33,35,37,41 +1.5V  
+3V  
21,25,26,28,33,34,35,37,39,43 3V5US



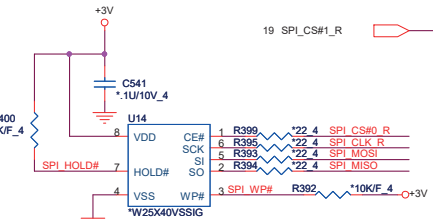
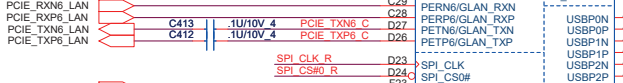
MINI CARD PCI-E (WLAN)

EXPRESS CARD (NEW CARD)

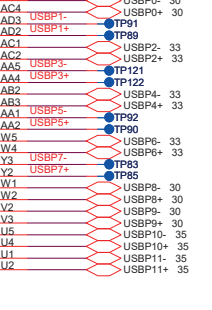
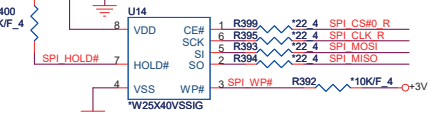
MINI CARD PCI-E (WWAN)



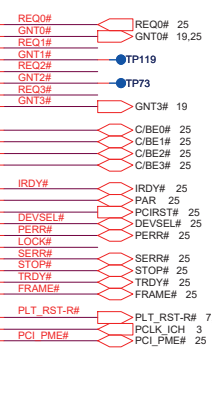
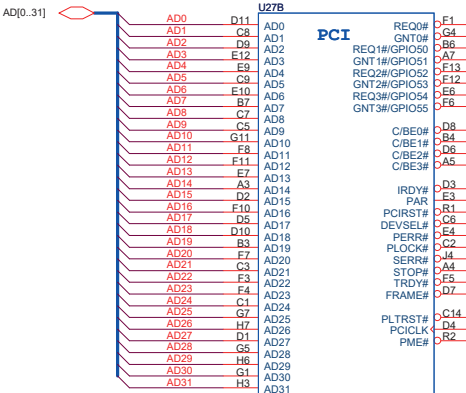
PCIE-LAN



512K byte SPI ROM For HDCP only



ICH9M REV 1.0



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTE#, F#, G#	RICOH R5C847

USB Connector

Finger Printer

BLUETOOTH

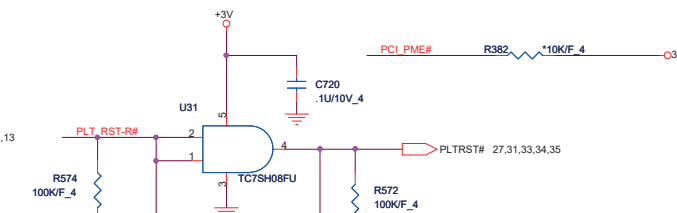
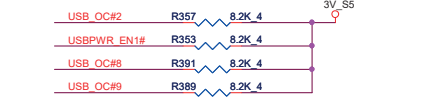
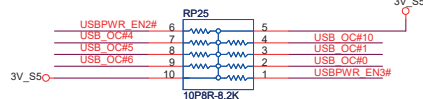
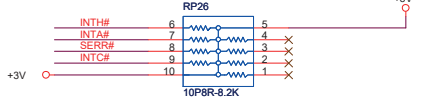
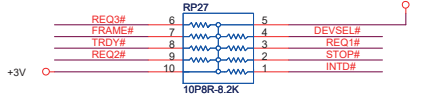
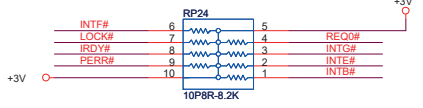
NEW CARD

USB Connector

USB Connector

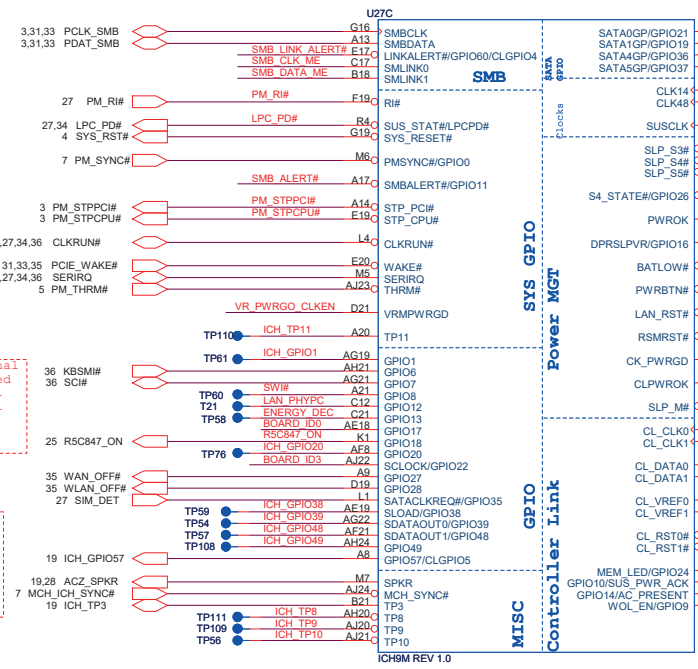
WWAN Min-Card

WLAN Min-Card



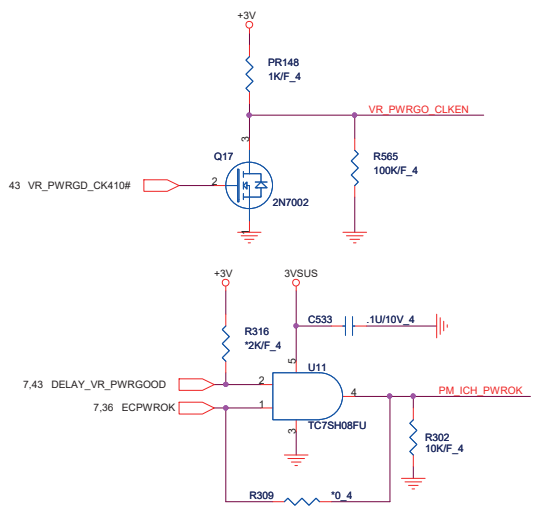
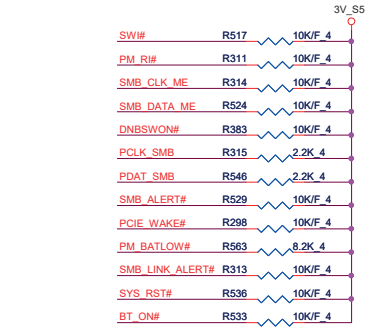
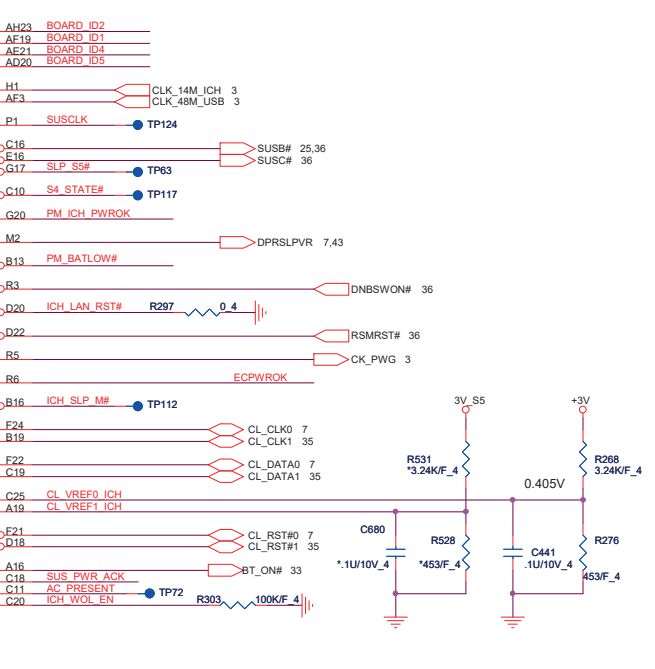
**PROJECT : IE8**  
**Quanta Computer Inc.**  
 Size: Custom Document Number: ICH9-M PCIE 2/4 Rev 1A  
 Date: Tuesday, November 20, 2007 Sheet 20 of 44

5,10,19,20,22,33,35,37,41 +1.5V  
 3,5,7,10,11,12,13,15,16,19,20,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44 +3V  
 19,20,22,37 3V\_S5  
 25,26,28,33,34,35,37,39,43 3VSUS



Notice: GPIO20 signal should not be pulled high for functional strap (internal pull down 20k).

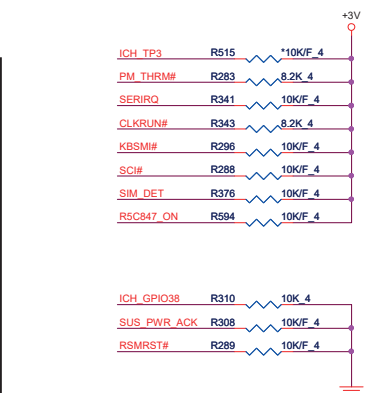
Notice: GPIO49 is also a strap pin (internal pull up 20k). Don't pull-down.



Board ID For Function	ID3 GPIO22	ID2 GPIO21	ID1 GPIO19	ID0 GPIO17
Default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

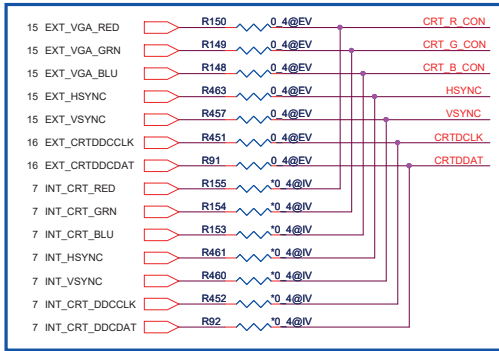
  

Board ID For Model	ID5 GPIO37	ID4 GPIO36
LE6	0	0
LE7	0	1
LE8	1	0
LE9	1	1





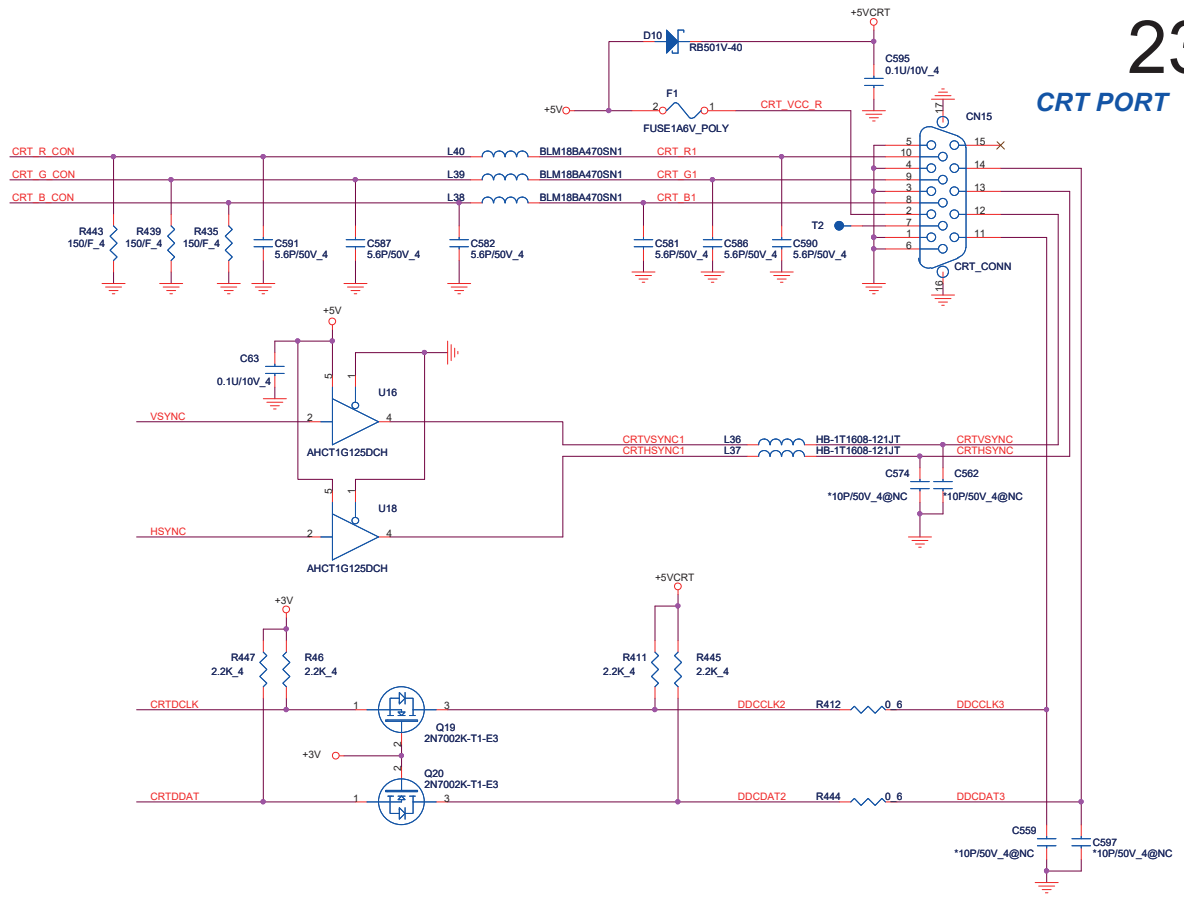
CRT SWITCH



UMA & Discrete setting

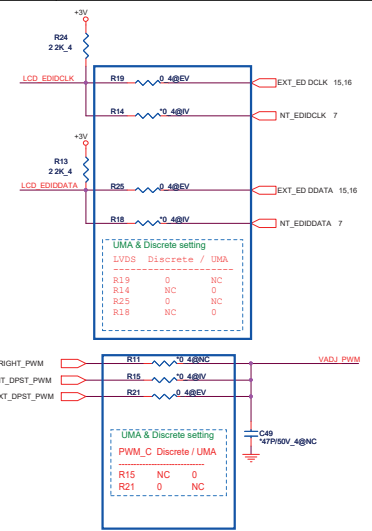
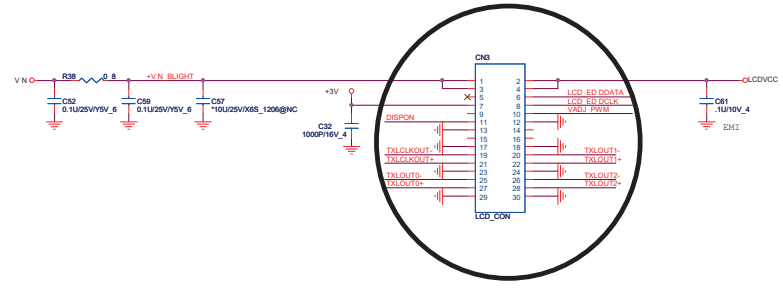
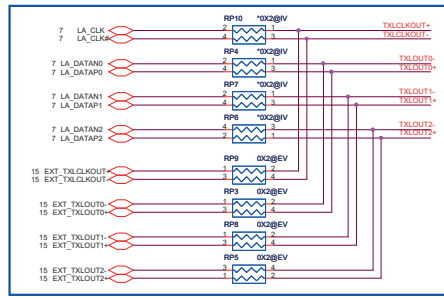
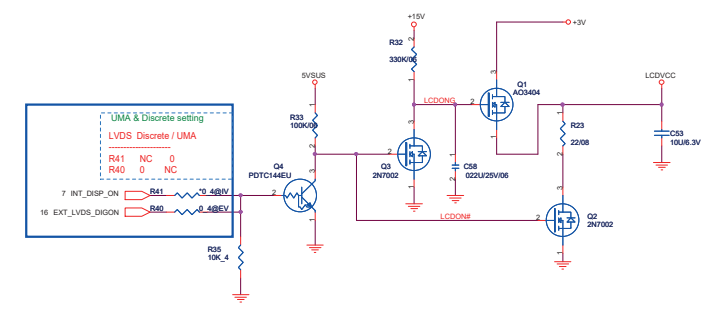
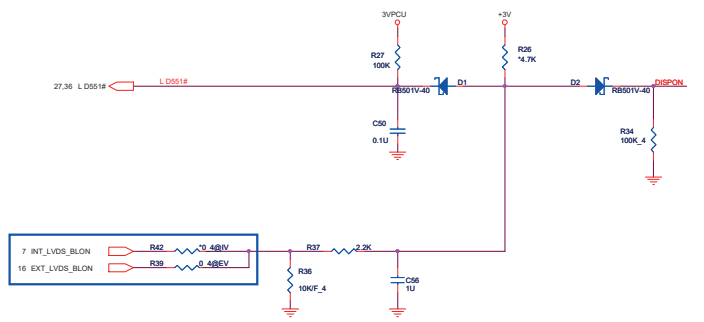
LVDS Discrete / UMA

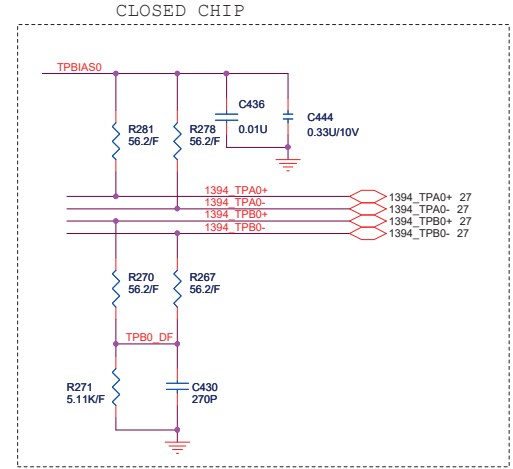
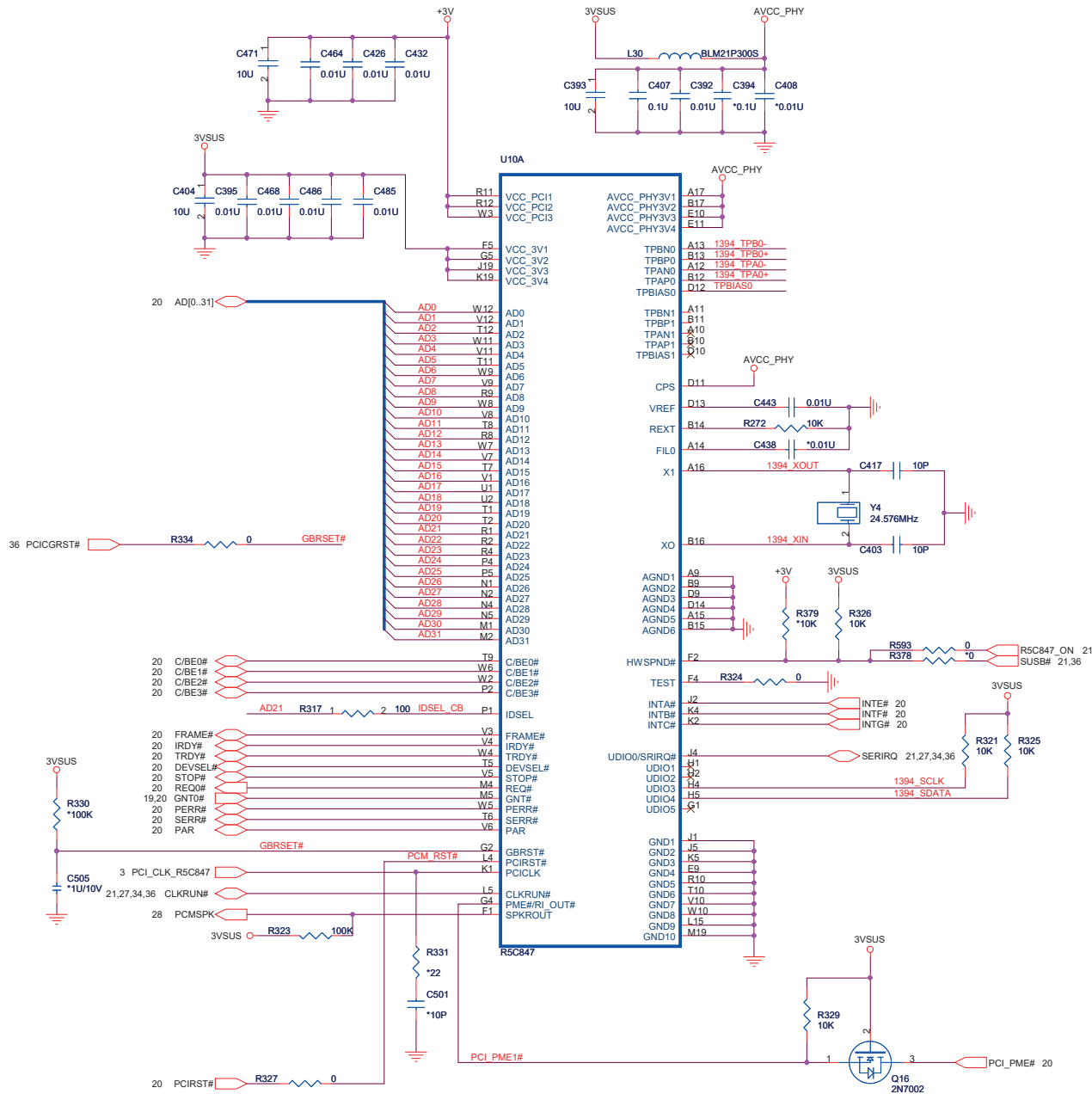
R150	0	NC
R149	0	NC
R148	0	NC
R463	0	NC
R457	0	NC
R451	0	NC
R91	0	NC
R155	NC	0
R154	NC	0
R153	NC	0
R461	NC	0
R460	NC	0
R452	NC	0
R92	NC	0



**PROJECT : LE8**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>CRT CON</b>	Rev 1A
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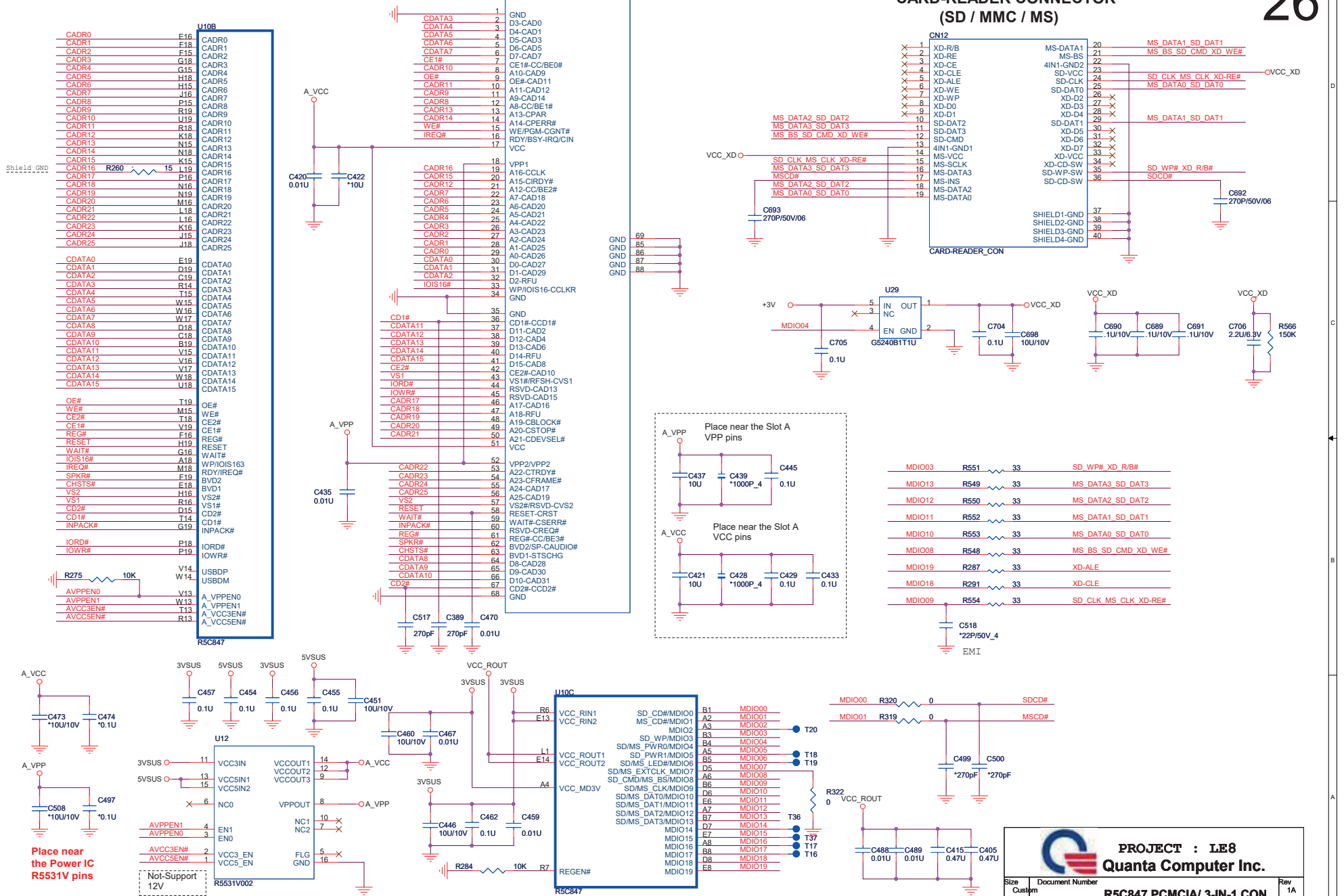


R5C847 pin to pin compatible with R5C843/R5C841

		<b>PROJECT : LE8</b>	
		<b>Quanta Computer Inc.</b>	
Size Custom	Document Number <b>R5C847 PCI/1394</b>	Rev 1A	
Date: Tuesday, November 20, 2007	Sheet 25	of 44	

# PCMCIA CONNECTOR

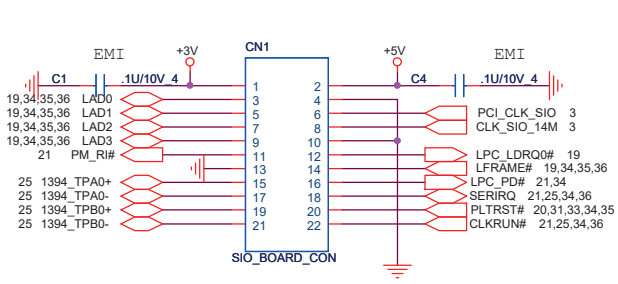
# CARD-READER CONNECTOR (SD / MMC / MS)



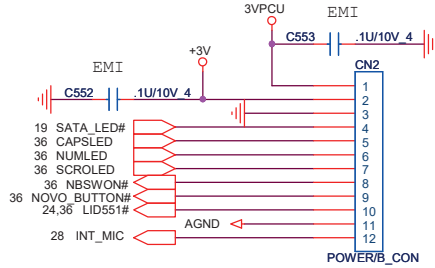
**PROJECT : LE8**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>R5C847 PCMCIA/ 3-IN-1 CON</b>	1A
Date:	Tuesday, November 20, 2007	Sheet 26 of 44

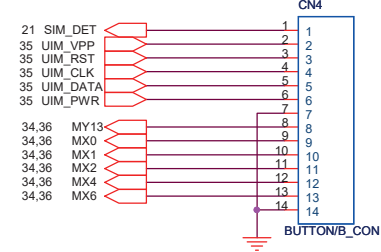
SIO BOARD



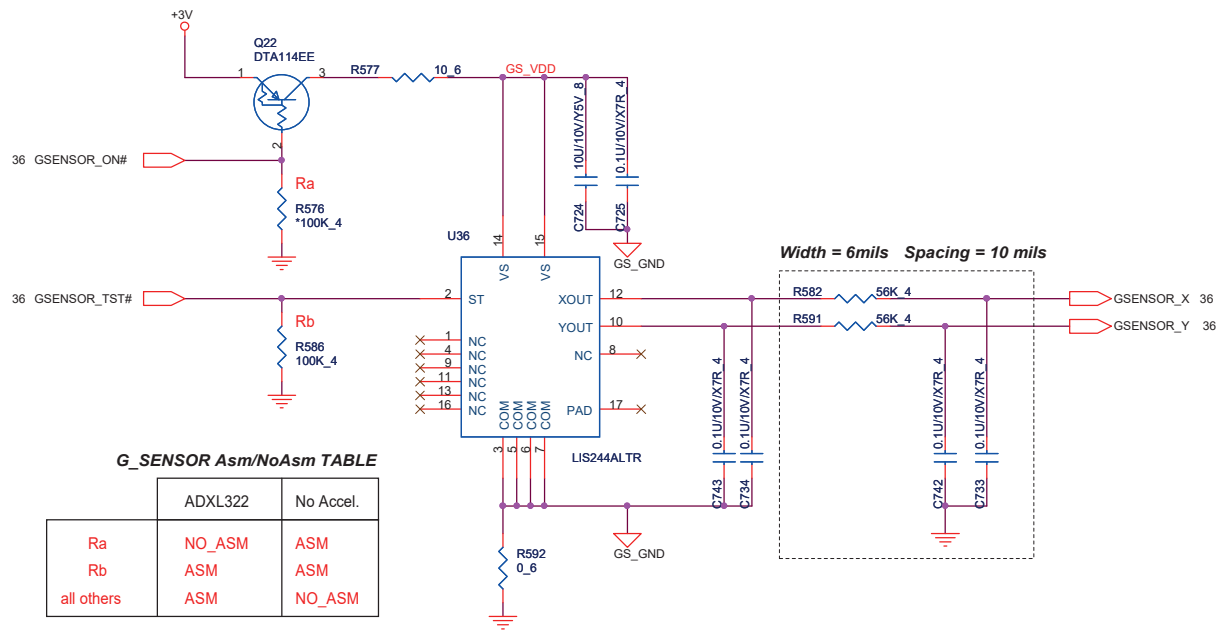
POWER BOARD



BUTTON BOARD

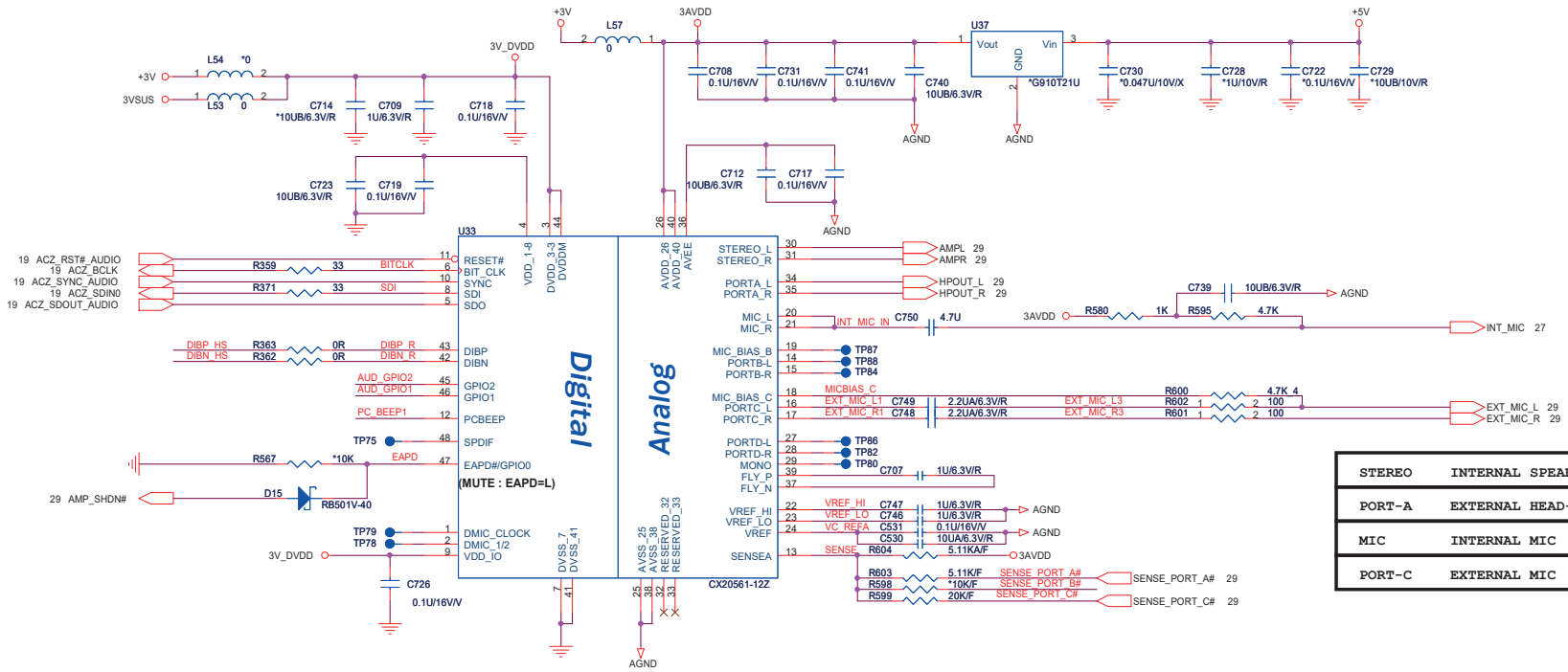


G-SENSOR



**PROJECT : LE8**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>T/Bs &amp; G-SENSOR</b>	Rev 1A
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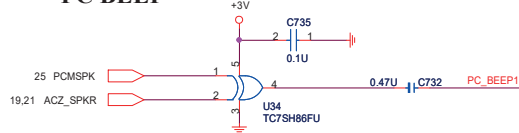
STEREO	INTERNAL SPEAKERS
PORT-A	EXTERNAL HEAD-PHONE
MIC	INTERNAL MIC
PORT-C	EXTERNAL MIC

GAIN	10K GPIO RESISTORS	
	GPIO1	GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

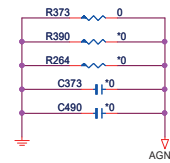
Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2



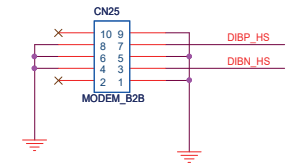
**PC BEEP**



**FOR EMI SOLUTION**

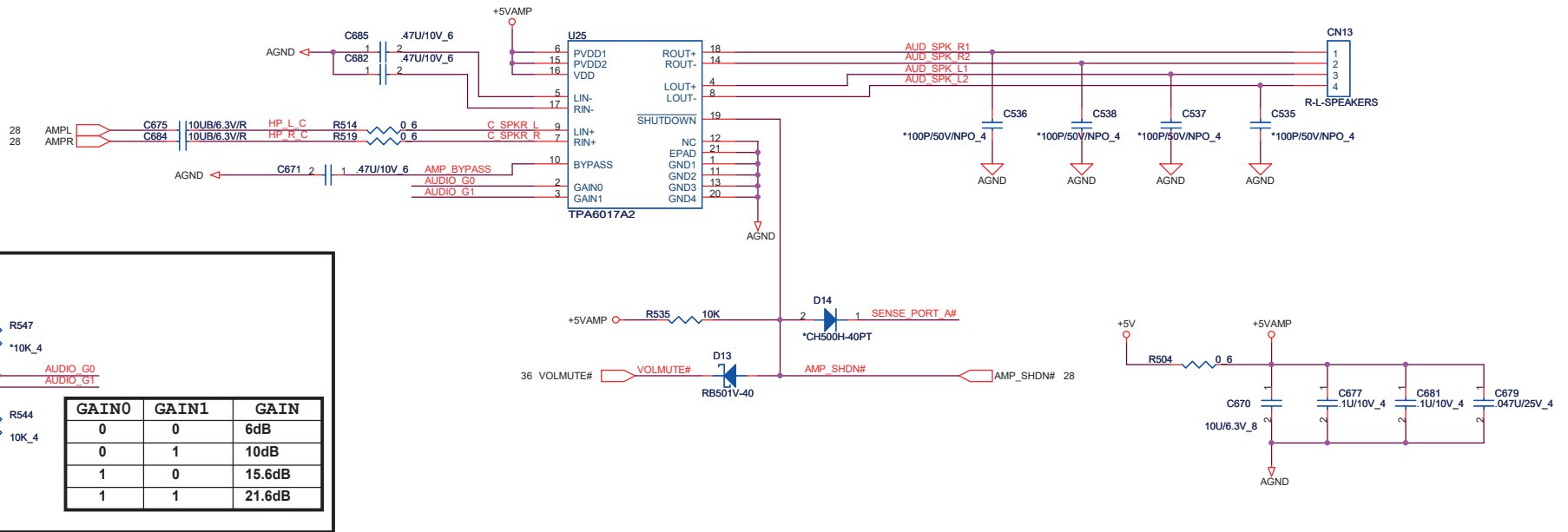


**MODEM/B CONN.**

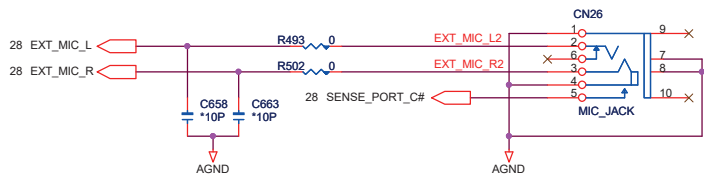


**PROJECT : LE8**  
**Quanta Computer Inc.**

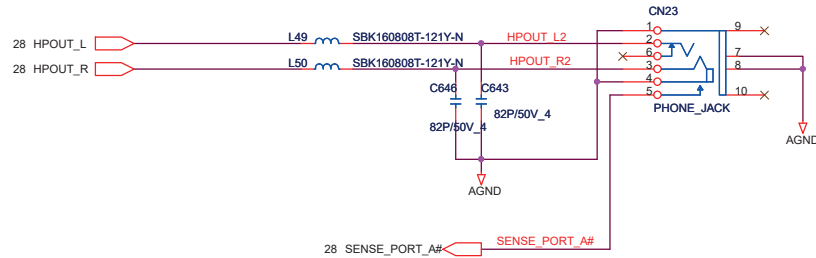
# INTERNAL SPEAKER AMPLIFIER




## MIC-IN JACK



## HEADPHONE





**PROJECT : LE8**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>AMP_TPA6017 &amp; JACKS</b>	Rev 1A
Date: Tuesday, November 20, 2007		Sheet 29 of 44

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